Chrontel

CH7303

Preliminary Advanced Information

Chrontel CH7303 HDTV / DVI Encoder

Features

- Digital Visual Interface (DVI) Transmitter up to 165M pixels/second
- DVI low jitter PLL
- DVI hot plug detection
- Analog YPrPb outputs for HDTV
- HDTV support for 480p, 576p, 720p, 1080i and 1080p
- Macrovision™ copy protection support for HDTV
- Programmable digital input interface supporting RGB (15, 16, 24 or 30 bit) and YCrCb input data formats
- Can output either RGB or YPrPb
- TV / Monitor connection detect
- Programmable power management
- Three 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device
- Offered in a 64-pin LQFP package
- Backward pin compatible with CH7301 or CH7009/11
- Support three additional 15 bit multiplexed RGB Input Data Format (IDF 6,7.8)

† Patent number 5,781,241
¥ Patent number 5,914,753

Note: Other names and brands may be claimed as property by others.

General Description

The CH7303 is a Display Controller device which accepts a digital graphics input signal, and encodes and transmits data through a DVI link (DFP can also be supported), VGA ports (analog RGB) or a HDTV port (YPrPb). The device is able to encode the video signals and generate synchronization signals for analog HDTV interface standards and graphics standards up to UXGA. The device accepts data over one 15-bit wide variable voltage data port which supports 9 different data formats including RGB and YCrCb.

The DVI processor includes a low jitter PLL for generation of the high frequency serialized clock, and all circuitry required to encode, serialize and transmit data. The CH7303 is able to drive a DFP display at a pixel rate of up to 165MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

In addition to DVI encoder modes, bypass modes are included which perform color space conversion to HDTV standards and generate and insert HDTV sync signals, or output VGA style analog RGB for use as a CRT DAC.

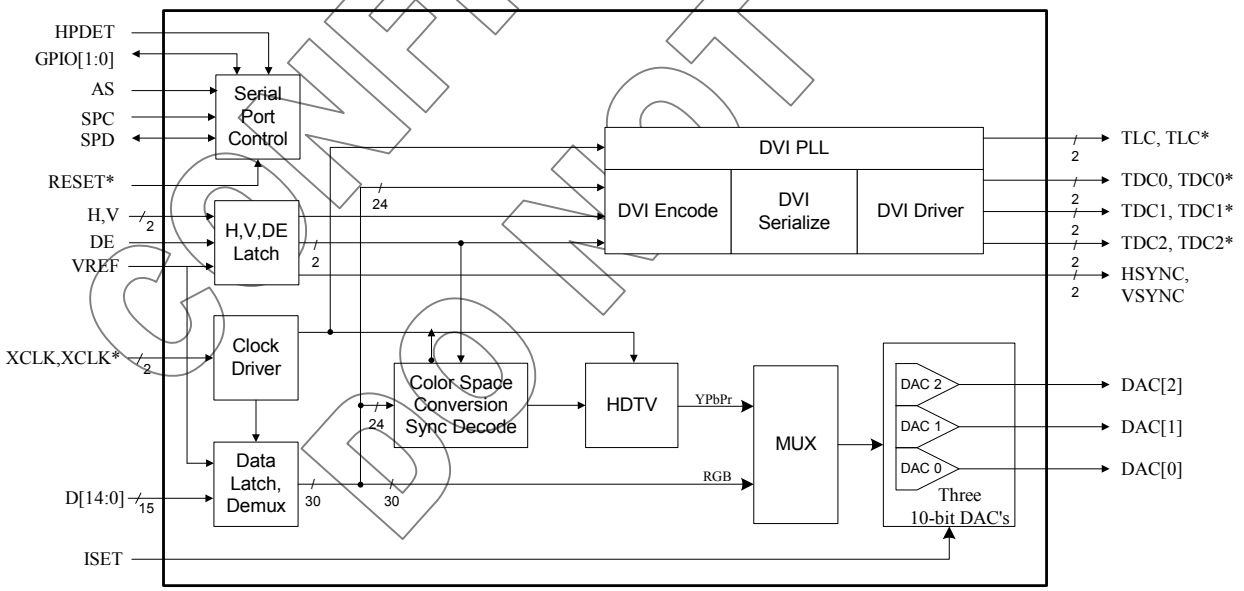

Figure 1: Functional Block Diagram

1.0 Pin-Out

1.1 Package Diagram

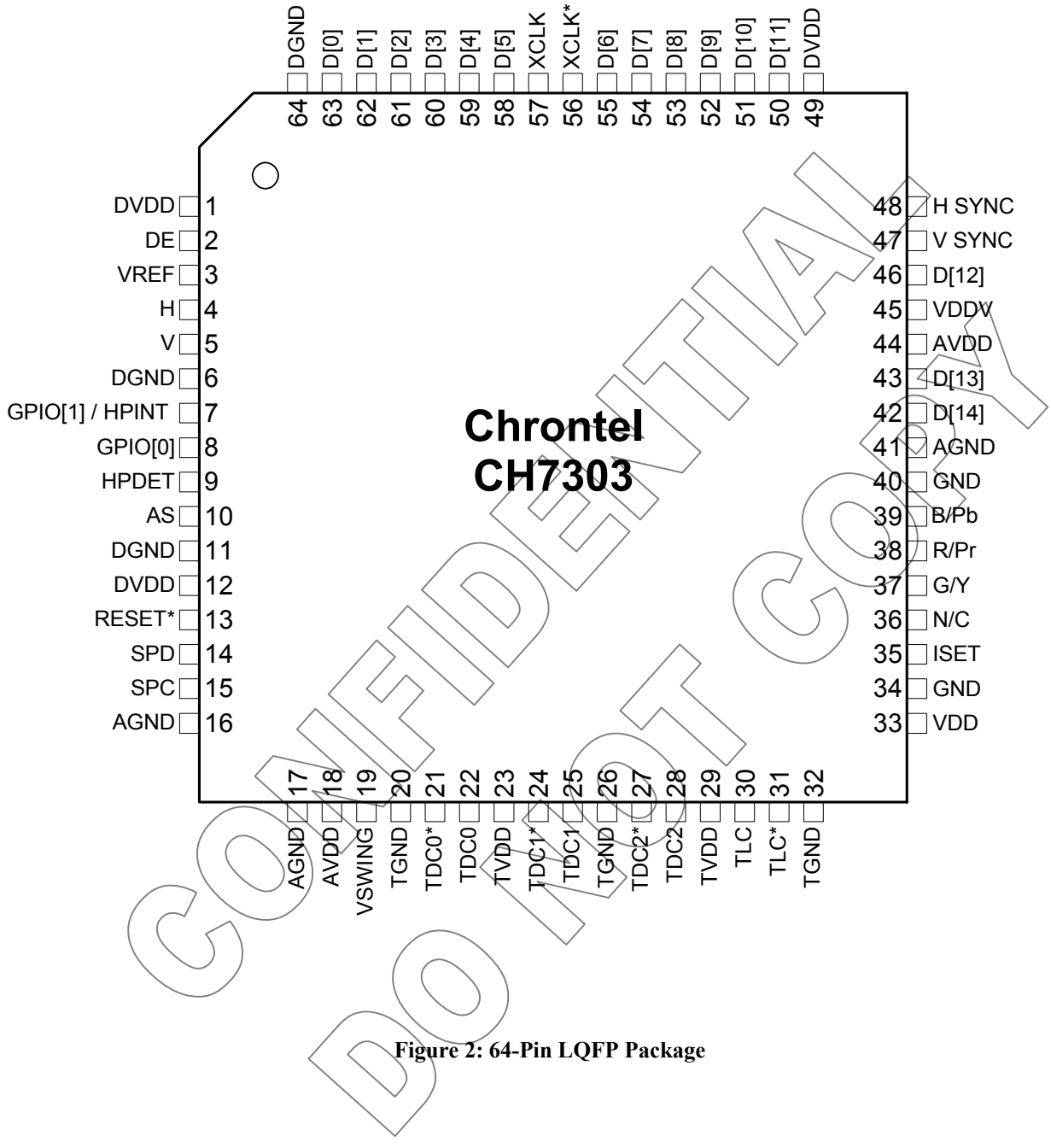

Figure 2: 64-Pin LQFP Package

1.2 Pin Description

Table 1: Pin Description

Pin #	# Pins	Type	Symbol	Description
2	1	In	DE	**Data Enable** This pin accepts a data enable signal which is high when active video data is input to the device, and low all other times. The levels are 0 to VDDV, and the VREF signal is used as the threshold level. This input is used by the DVI.
3	1	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync, data enable and clock inputs.
4	1	In	H	**Horizontal Sync Input** This pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDV and the VREF signal is used as the threshold level.
5	1	In	V	**Vertical Sync Input** This pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDV and the VREF signal is used as the threshold level.
7	2	In/Out	GPIO[1] / HPINT	**DVI Link Detect Output** When the GPIO[1] pin is configured as an output, this pin can be used to output the DVI detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. The output is released through serial port control.
8	2	In/Out	GPIO[0]	**General Purpose Input - Output[0]** (Weak internal pull-up) This pin provides a general-purpose I/O controlled via the serial port. The internal pull-up will be to the DVDD supply.
9	1	In	HPDET	**Hot Plug Detect** (internal pull-down) This input pin determines whether the DVI is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via GPIO[1]/TLDET* pin pulling low.
10	1	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (1,1,1,0,1,AS*,AS).
13	1	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
14	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to VDDV. Outputs are driven from 0 to VDDV.
15	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and operates with inputs from 0 to VDDV.
19	1	In	VSWING	**DVI Swing Control** This pin sets the swing level of the DVI outputs. A 2.4K ohm resistor should be connected between this pin and TGND using short and wide traces.
22, 21	2	Out	TDC0, TDC0*	**DVI Data Channel 0 Outputs** These pins provide the DVI differential outputs for data channel 0 (blue).
25, 24	2	Out	TDC1, TDC1*	**DVI Data Channel 1 Outputs** These pins provide the DVI differential outputs for data channel 1 (green).

Table 1: Pin Description (contd.)

Pin #	# Pins	Type	Symbol	Description
28, 27	2	Out	TDC2, TDC2*	**DVI Data Channel 2 Outputs** These pins provide the DVI differential outputs for data channel 2 (red).
30, 31	2	Out	TLC, TLC*	**DVI Clock Outputs** These pins provide the differential clock output for the DVI interface corresponding to data on the TDC[0:2] outputs.
35	1	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and DAC ground (pins 34 and 40) using short and wide traces.
37	1	Out	Y/G (DAC1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75ohm doubly terminated load. The output can be selected to be the luminance component of YprPb or Green.
38	1	Out	R/Pr (DAC2)	**Red / Pr Output** This pin outputs a selectable video signal. The output is designed to drive a 75ohm doubly terminated load. The output can be selected to be the Pr component of YPrPb or red.
39	1	Out	B/Pb (DAC0)	**Blue / Pb Output** This pin outputs a selectable video signal. The output is designed to drive a 75ohm doubly terminated load. The output can be selected to be the Pb component of YPrPb or blue.
47	1	Out	VSYNC	**VSYNC** By programming BCO register, a buffered version of VGA vertical sync can be acquired from this pin . This output pin can also provide a buffered clock output, driven by the DVDD supply.
48	1	Out	HSYNC	**Horizontal Sync Output** A buffered version of VGA horizontal sync can be acquired from this pin via DC register)
50 -55, 58 –63, 42, 43, 46	15	In/Out	D[14] - D[0]	**Data[14] through Data[0] Inputs** These pins accept the 15 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV, and the VREF signal is used as the threshold level.
57, 56	2	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the CH7303 for use with the H, V, DE and D[14:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The clock polarity used can be selected using the MCP control bit.
1, 12, 49	3	Power	DVDD	**Digital Supply Voltage** (3.3V)
6, 11, 64	3	Power	DGND	**Digital Ground**
45	1	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
23, 29	2	Power	TVDD	**DVI Transmitter Supply Voltage** (3.3V)
20, 26, 32	3	Power	TGND	**DVI Transmitter Ground**
18, 44	2	Power	AVDD	**PLL Supply Voltage** (3.3V)
16, 17, 41	3	Power	AGND	**PLL Ground**
33	1	Power	VDD	**DAC Supply Voltage** (3.3V)
34, 40	2	Power	GND	**DAC Ground**

2.0 Functional Description

2.1 TV Output Operation

The CH7303 is capable of being operated as in one of several bypass modes for driving monitors requiring component video signals (HDTV, multi-sync monitors, etc.). All modes make use of the same set of DAC's, and therefore cannot be used simultaneously. Table 2 describes the possible operating modes. A 'p' following a number in the Input Scan Type column indicates a progressive scan (non-interlaced) input where the number indicates the active number of lines per frame. An 'i' following a number in the Input Scan Type column indicates an interlaced input where the number indicates the active number of lines per frame. Detailed descriptions of each of the operating modes follows Table 2.

Table 2: Operating Modes

Input Scan Type	Input Data Format	Output scan Type	Output Format	Operating Mode
non-interlaced	RGB	non-interlaced	RGB	RGB bypass
non-interlaced (480p, 576p, 720p)	RGB / YCrCb[1]	non-interlaced	YpbPr[2,3]	HDTV/EDTV bypass
Interlaced (1080i)	RGB / YCrCb[1]	interlaced	YpbPr[3]	HDTV/EDTV bypass (1080i)
non-interlaced (1080p)	RGB / YCrCb[1]	non-interlaced	YpbPr[3]	HDTV/EDTV bypass (1080p)

2.1.1 HDTV / EDTV Bypass

In HDTV / EDTV Bypass mode, data, sync and clock signals are input to the CH7303 from a graphics device in the scanning method that matches the display device (interlaced data is sent to the CH7303 to drive an interlaced display, non-interlaced data is sent to the CH7303 to drive a non-interlaced display). The input data format can be YCrCb or RGB. Horizontal and vertical sync signals must either be sent to the CH7303 from the graphics device or embedded in the data stream according to SMPTE standards. Data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. Input data is color space converted to the selected video format, has sync signals generated and is output from the video DAC's. The output format is YPbPr. The graphics resolutions supported for HDTV Bypass mode are shown in Table 3 below. The resolutions supported for EDTV Bypass mode are shown in Table 3 below.

Table 3: HDTV Bypass

Active Resolution	Total Resolution	Scan Type	Pixel Clock (MHz)	Frame Rate (Hz)	Standard
1280x720	1650x750	Non-Interlaced	74.25 74.25/1.001	60 60/1.001	SMPTE 296M
1280x720	1648x750	Non-Interlaced	74.160	60	
1920x1080	2200x1125	Interlaced	74.25 74.25/1.001	30 30/1.001	SMPTE 274M
1920x1080	2640x1125	Interlaced	74.25	25	SMPTE 274M
1920x1080	2376x1250	Interlaced	74.25	25	SMPTE 295M
1920x1080	2200x1125	Non-Interlaced	148.5 148.5/1.001 74.25 74.25/1.001	60 60/1.001 30 30/1.001	SMPTE 274M
1920x1080	2640x1125	Non-Interlaced	148.5 74.25	50 25	SMPTE 274M
1920x1080	2750x1125	Non-Interlaced	74.25 74.25/1.001	24 24/1.001	SMPTE 274M
1920x1080	2752x1125	Non-Interlaced	74.304	24	
1920x1080	2376x1250	Non-Interlaced	148.5	50	SMPTE 295M

Table 4: EDTV Bypass

Active Resolution	Total Resolution	Scan Type	Pixel Clock (MHz)	Frame Rate (Hz)	Standard
720x480	858x525	Non-Interlaced	27.0	60/1.001	EIA-770.2-A
720x483	858x525	Non-Interlaced	27.027	60	SMPTE 293M
720x480	856x525	Non-Interlaced	26.937	60/1.001	
720x483	856x525	Non-Interlaced	26.964	60	
720x576	864x625	Non-interlaced	27.0	50	ITU-R BT.1358

2.1.2 RGB Bypass

In RGB Bypass mode, data, sync and clock signals are input to the CH7303 from a graphics device, and bypassed directly to the D/A converters to implement a second CRT DAC function. External sync signals must be supplied from the graphics device. These sync signals are buffered internally, and can be output to drive the CRT. The input data format must be RGB in this operating mode. Input data is 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The CH7303 can support a pixel rate of 165MHz. This operating mode uses all 8 bits of the DAC's 10-bit range, and provides a nominal signal swing of 0.661V (or 0.7V depending on DAC Gain setting in control registers) when driving a 75Ω doubly terminated load. No scaling, scan conversion or flicker filtering is applied in Bypass modes.

2.2 DVI Output

2.2.1 DVI Transmitter

In DVI Output mode, multiplexed input data, sync and clock signals are input to the CH7303 from the graphics controller's digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. Some examples of modes supported are shown in the table. For the table below, clock frequencies for given modes were taken from VESA DISPLAY MONITOR TIMING SPECIFICATIONS if they were detailed there, not VESA TIMING DEFINITION FOR FLAT PANEL MONITORS. The device is not dependent upon this set of timing specifications. Any values of pixels/line, lines/frame and clock rate are acceptable, as long as the pixel rate remains below 165MHz. The input format can be any RGB format or YCrCb (see Input Data Formats section).

Table 9: DVI Output

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	Refresh Rate (Hz)	XCLK Frequency (MHz)	DVI Frequency (MHz)
720x400	4:3	1.35:1.00	<85	<35.5	<355
640x400	8:5	1:1	<85	<31.5	<315
640x480	4:3	1:1	<85	<36	<360
720x480	4:3	9:8	59.94	27	270
720x576	4:3	15:12	50	27	270
800x600	4:3	1:1	<85	<57	<570
1024x768	4:3	1:1	<85	<95	<950
1280x720	16:9	1:1	<60	<67	<670

2.3 Input Interface

2.3.1 Overview

Two distinct methods of transferring data to the CH7303 are described. They are:

- Multiplexed data, clock input at 1X the pixel rate
- Multiplexed data, clock input at 2X the pixel rate

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7303 is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X pixel rate the data applied to the CH7303 is latched with one edge of the clock (also known as single edge transfer mode or SDR). The polarity of the pixel clock can be reversed under serial port control. In single edge transfer modes, the clock edge used to latch data is programmable. In dual edge transfer modes, the clock edge used to latch the first half of each pixel is programmable.

2.3.2 Interface Voltage Levels

The graphics controller interface can operate at a variable voltage level controlled by the voltage on the **VDDV** pin. This should be set to the maximum voltage of the interface (typically 3.3V or adjustable between 1.1 and 1.8V). The VREF pin is the voltage reference for the data, date enable, clock and sync inputs and must be tied to VDDV/2. This is typically done using a resistor divider.

2.3.3 Input Clock and Data Timing Diagram

Figure 3 below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK/XCLK* waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in section **Error! Reference source not found.**.

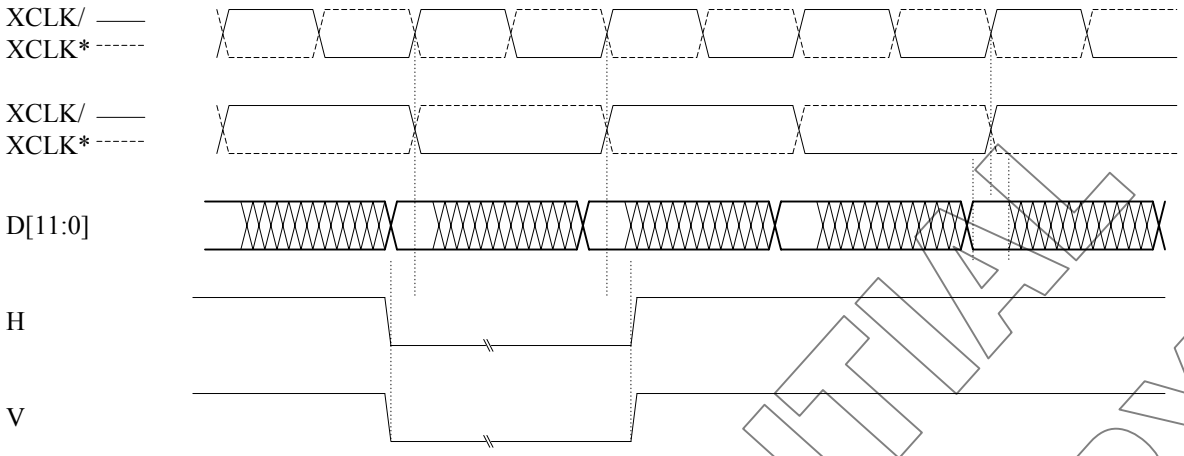

Figure 3: Clock, Data and Interface Timing

2.3.4 Data De-skew Feature

The de-skew feature allows adjustment of the input setup and hold time. The input data D[14:0] can be latched slightly before or after the latching edge of XCLK depending on the amount of the de-skew. Note that the XCLK is not changed, only the time at which the data is latch relative to XCLK. .The de-skew is controlled using the XCMD[3:0] bits located in CH7303 register. The delay t_{CD} between clock and data is given by the following formula:

t_{CD} = - XCMD[3:0] * t_{STEP} for $0 \le$ XCMD[3:0] ≤ 7
t_{CD} = (XCMD[3:0] – 8) * t_{STEP} for $8 \le$ XCMD[3:0] ≤ 15

where XCMD is a number between 0 and 15 represented as a binary code
t_{STEP} is the adjustment increment

2.3.5 Input Data Formats

The CH7303 supports 9 different multiplexed data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge (rising or falling depending on the value of the MCP bit – rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal). The input data formats are (IDF[2:0]):

IDF	Description
0	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 1)
1	12-bit multiplexed RGB input (24-bit color), (multiplex scheme 2)
2	8-bit multiplexed RGB input (16-bit color, 565)
3	8-bit multiplexed RGB input (15-bit color, 555)
4	8-bit multiplexed YCrCb input (24-bit color), (Y, Cr and Cb are multiplexed)
5	12-bit multiplexed RGB input (24-bit color), (multiplex scheme A3 - edge-pair)
6	15-bit multiplexed RGB input (30-bit color), (multiplex scheme B1 - half-half mode)
7	15-bit multiplexed RGB input (30-bit color), (multiplex scheme B2 - half-color mode)
8	15-bit multiplexed RGB input (30-bit color), (multiplex scheme B3 - edge pair mode)

The input data format is shown in Figure 4 below. The Pixel Data bus represents a 15-bit, 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; P0a and P0b) will contain a complete pixel encoded as shown in Table 9 through Table 8.

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

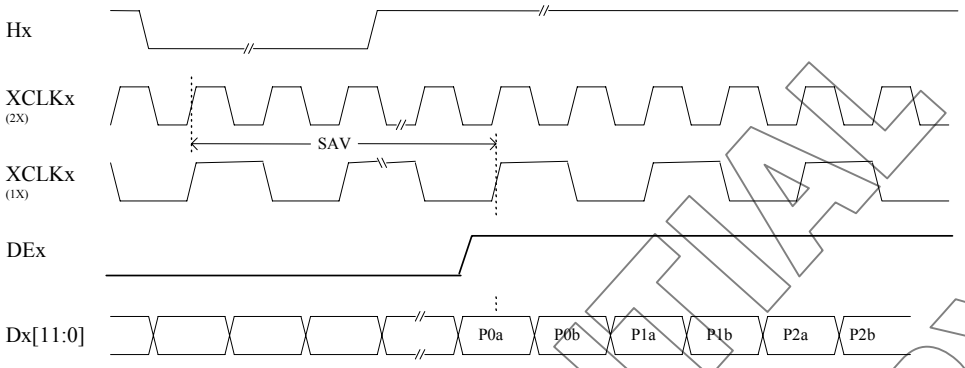

Figure 4: 12-bit Multiplexed Input Data Formats (IDFx = 0,1,2,3,4)

Table 5: Multiplexed Input Data Formats (IDF = 0, 1)

IDF = Format =		0 12-bit RGB				1 12-bit RGB			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	D[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	D[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	D[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	D[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	D[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	D[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	D[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	D[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	D[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	D[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	D[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 6: Multiplexed Input Data Formats (IDF = 2, 3)

IDF = Format =		2 RGB 5-6-5				3 RGB 5-5-5			
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P0a**	**P0b**	**P1a**	**P1b**
Bus Data	D[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	D[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	D[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	D[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	D[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	D[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	D[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	D[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 7: Multiplexed Input Data Formats (IDF = 4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

Table 8: Embedded Sync in Multiplexed Data Format (IDF=4)

IDF = Format =		4 YCrCb 8-bit							
Pixel #		**P0a**	**P0b**	**P1a**	**P1b**	**P2a**	**P2b**	**P3a**	**P3b**
Bus Data	D[7]	1	0	0	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	D[6]	1	0	0	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	D[5]	1	0	0	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	D[4]	1	0	0	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	D[3]	1	0	0	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	D[2]	1	0	0	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	D[1]	1	0	0	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	D[0]	1	0	0	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7:0] byte contains the following data:

S[6] = F = 1 during field 2, 0 during field 1
S[5] = V = 1 during field (frame) blank, 0 elsewhere
S[4] = H = 1 during EAV (synchronization reference at the end of active video)
0 during SAV (synchronization reference at the start of active video)

Bits S[7] and S[3:0] are ignored.

Table 9: Multiplexed Input Data Formats (IDF = 6, 7, 8)

IDF = Format =		6 15-bit RGB		7 15-bit RGB		8 15-bit RGB	
Pixel #		**P0a**	**P0b**	**P0a**	**P0b**	**P0a**	**P0b**
Bus Data	D[14]	G0[4]	R0[9]	R0[4]	R0[9]	R0[8]	R0[9]
	D[13]	G0[3]	R0[8]	R0[3]	R0[8]	R0[6]	R0[7]
	D[12]	G0[2]	R0[7]	R0[2]	R0[7]	R0[4]	R0[5]
Bus Data	D[11]	G0[1]	R0[6]	R0[1]	R0[6]	R0[2]	R0[3]
	D[10]	G0[0]	R0[5]	R0[0]	R0[5]	R0[0]	R0[1]
	D[9]	B0[9]	R0[4]	G0[4]	G0[9]	G0[8]	G0[9]
	D[8]	B0[8]	R0[3]	G0[3]	G0[8]	G0[6]	G0[7]
	D[7]	B0[7]	R0[2]	G0[2]	G0[7]	G0[4]	G0[5]
	D[6]	B0[6]	R0[1]	G0[1]	G0[6]	G0[2]	G0[3]
	D[5]	B0[5]	R0[0]	G0[0]	G0[5]	G0[0]	G0[1]
	D[4]	B0[4]	G0[9]	B0[4]	B0[9]	B0[8]	B0[9]
	D[3]	B0[3]	G0[8]	B0[3]	B0[8]	B0[6]	B0[7]
	D[2]	B0[2]	G0[7]	B0[2]	B0[7]	B0[4]	B0[5]
	D[1]	B0[1]	G0[6]	B0[1]	B0[6]	B0[2]	B0[3]
	D[0]	B0[0]	G0[5]	B0[0]	B0[5]	B0[0]	B0[1]

3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All power supplies relative to GND	-0.5		5.0	V
	Input voltage of all digital pins	GND – 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	0		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (1 minute)			220	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

3.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	PLL Power Supply Voltage	3.1	3.3	3.6	V
VDD	DAC Power Supply Voltage	3.1	3.3	3.6	V
DVDD	Digital Power Supply Voltage	3.1	3.3	3.6	V
VDDV	I/O Power Supply Voltage	1.1	1.8	3.6	V
R_L	Output load to DAC Outputs		37.5		Ω

3.3 Electrical Characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD =3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		33.9		mA
	Video level error			10	%
I_{VDD}	Total supply current		TBD		mA
I_{VDDV}	VDDV (1.8V) current (15pF load)		4		mA
I_{PD}	Total Power Down Current		0.06		mA

3.4 DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Inputs		0.25			V
V_{DATAIH}	D[0-14] Input High Voltage		Vref+0.25		DVDD+0.5	V
V_{DATAIL}	D[0-14] Input Low Voltage		GND-0.5		Vref-0.25	V
V_{MISCIH}	GPIOx, RESET*, AS, HPDET Input High Voltage	DVDD=3.3V	2.7		VDD + 0.5	V
V_{MISCIL}	GPIOx, RESET*, AS, HPDET Input Low Voltage	DVDD=3.3V	GND-0.5		0.6	V
I_{MISCPU}	Pull Up Current (GPIO, RESET*, AS)	V_{IN} = 0V	0.5		5.0	uA
I_{MISCPD}	Pull Down Current (HPDET)	V_{IN} = 3.3V	0.5		5.0	uA
V_{MISCOH}	GPIOx, VSYNC, HSYNC Output High Voltage	I_{OH} = -0.4mA	DVDD-0.2			V
V_{MISCOL}	GPIOx, VSYNC, HSYNC Output Low Voltage	I_{OL} = 3.2mA			0.2	V
V_H	DVI Single Ended Output High Voltage	TVDD = 3.3V ± 5% R_{TERM} = 50Ω ± 1% R_{SWING} = 2400Ω ± 1%	TVDD – 0.01		TVDD + 0.01	V
V_L	DVI Single Ended Output Low Voltage		TVDD – 0.6		TVDD – 0.4	V
V_{SWING}	DVI Single Ended Output Swing Voltage		400		600	mVp-p
V_{OFF}	DVI Single Ended Standby Output Voltage		TVDD – 0.01		TVDD + 0.01	V

Note :
V_{DATA} - refers to all digital data (D[14:0]), clock (XCLK, XCLK*), sync (H, V) and DE inputs. V_{MISC} - refers to GPIOx, RESET*, AS and HPDET inputs and GPIOx, VSYNC and HSYNC outputs.

3.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{XCLK}	Input (XCLK) frequency		25		165	MHz
t_{PIXEL}	Pixel time period		6.06		40	ns
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{XJIT}	XCLK clock jitter tolerance	f_{XCLK} = 75MHz		2		ns
t_{DVIR}	DVI Output Rise Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{DVIF}	DVI Output Fall Time (20% - 80%)	f_{XCLK} = 165MHz	75		242	ps
t_{SKDIFF}	DVI Output intra-pair skew	f_{XCLK} = 165MHz			90	ps
t_{SKCC}	DVI Output inter-pair skew	f_{XCLK} = 165MHz			1.2	ns
t_{DVIJIT}	DVI Output Clock Jitter	f_{XCLK} = 165MHz			150	ps
T_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	XCLK = XCLK* to D[11:0], H, V, DE = Vref	TBD			ns
T_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	D[11:0], H, V, DE = Vref to XCLK = XCLK*	TBD			ns
t_{STEP}	De-skew time increment		50		80	ps

3.6 Timing Information

3.6.1 Clock - Slave, Sync - Slave Mode

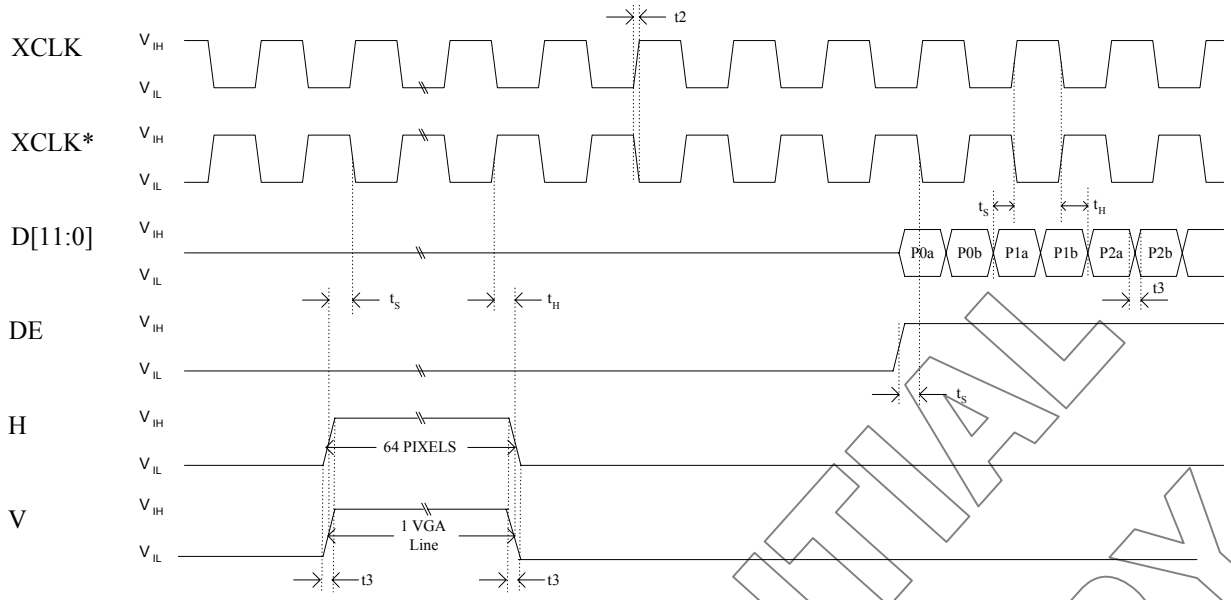

Figure 5: Timing for Clock - Slave, Sync - Slave Mode

Table 10: Timing for Clock - Slave, Sync - Slave Mode

Symbol	Parameter	Min	Typ	Max	Unit
t2	XCLK & XCLK* rise/fall time w/15pF load		3		ns
t3	D[11:0], H, V & DE rise/fall time w/ 15pF load		3		ns

4.0 Package Dimensions

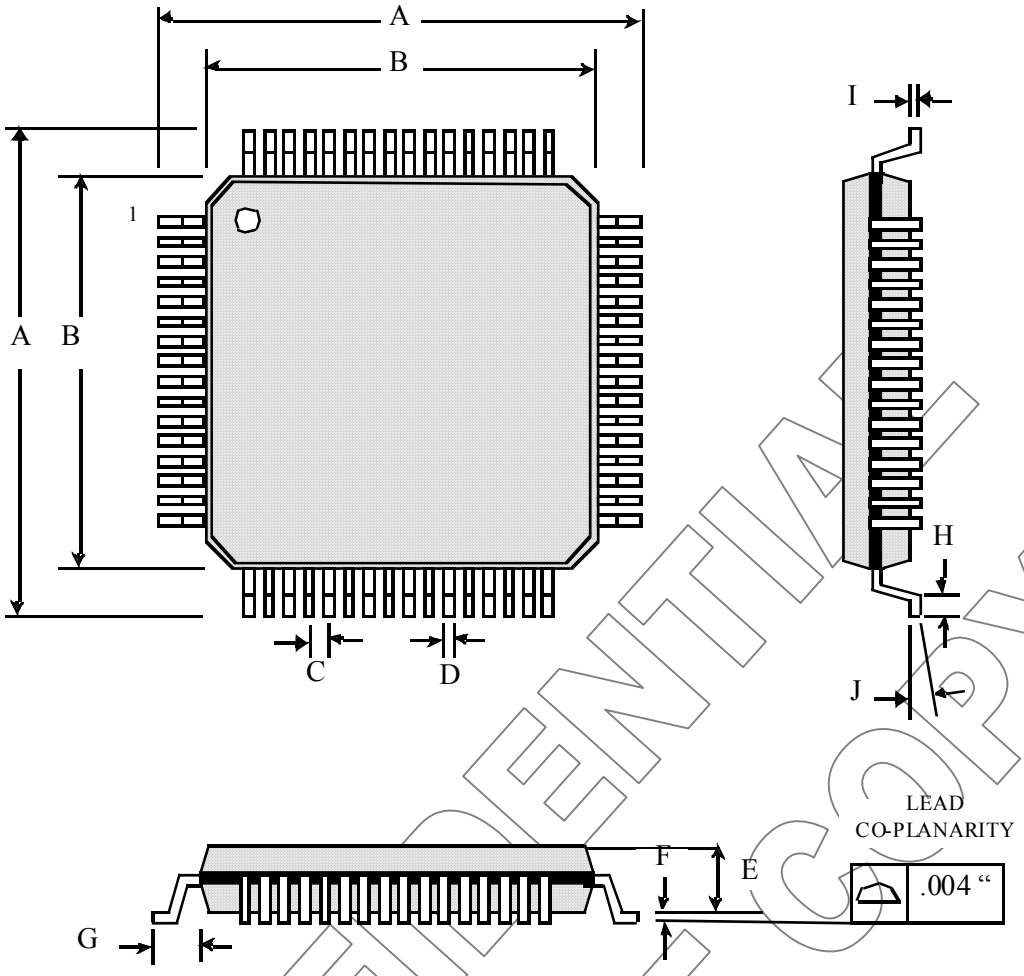

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Figure 6: 64 Pin LQFP Package

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