REVISIONS

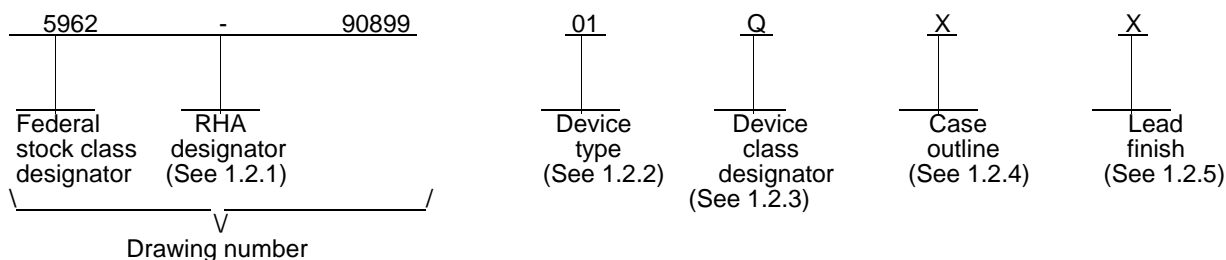| LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Added device types 09 - 13. Moved endurance and data retention testing requirements from Section 4 of drawing to Section 3 of drawing. Editorial changes throughout.	94-03-25	M. A. Frye
B	Updated boilerplate. Added vendor CAGE 01295 as a source of supply. Editorial changes throughout. - glg	98-04-16	Raymond Monnin
C	Changed standoff width on "U" package. Added vendor CAGE 0EU86 as a source of supply. - glg	99-11-16	Raymond Monnin

REV																			
SHEET																			
REV	C	C	C	C	C	C	C	C	C	C									
SHEET	15	16	17	18	19	20	21	22	23	24									

REV STATUS OF SHEETS		REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
		SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Gary L. Gross	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216**			
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin				
	APPROVED BY Michael A. Frye	MICROCIRCUIT, MEMORY, DIGITAL, CMOS 128K X 8 BIT FLASH EEPROM, MONOLITHIC SILICON			
	DRAWING APPROVAL DATE 92-08-31				
		SIZE **A**	CAGE CODE **67268**		**5962-90899**
	REVISION LEVEL C	SHEET	1	OF	24

1. SCOPE

1.1 <u>Scope</u>. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 <u>PIN</u>. The PIN shall be as shown in the following example:

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  5962    -    90899        01         Q            X            X
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| Federal stock class designator | RHA designator (See 1.2.1) | Device type (See 1.2.2) | Device class designator (See 1.2.3) | Case outline (See 1.2.4) | Lead finish (See 1.2.5) |

_____V_____/
                        Drawing number

1.2.1 <u>RHA designator</u>. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Endurance
01	28F010	(128 K x 8) CMOS flash EEPROM	250 ns	10,000 cycles
02	28F010	(128 K x 8) CMOS flash EEPROM	200 ns	10,000 cycles
03	28F010	(128 K x 8) CMOS flash EEPROM	150 ns	10,000 cycles
04	28F010	(128 K x 8) CMOS flash EEPROM	120 ns	10,000 cycles
05	28F010	(128 K x 8) CMOS flash EEPROM	250 ns	1,000 cycles
06	28F010	(128 K x 8) CMOS flash EEPROM	200 ns	1,000 cycles
07	28F010	(128 K x 8) CMOS flash EEPROM	150 ns	1,000 cycles
08	28F010	(128 K x 8) CMOS flash EEPROM	120 ns	1,000 cycles
09	28F010	(128 K x 8) CMOS flash EEPROM	90 ns	10,000 cycles
10	28F010A	(128 K x 8) CMOS flash EEPROM	250 ns	100,000 cycles
11	28F010A	(128 K x 8) CMOS flash EEPROM	200 ns	100,000 cycles
12	28F010A	(128 K x 8) CMOS flash EEPROM	150 ns	100,000 cycles
13	28F010A	(128 K x 8) CMOS flash EEPROM	120 ns	100,000 cycles

1.2.3 <u>Device class designator</u>. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 <u>Case outline(s)</u>. The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	32	"J" lead chip carrier
U	See figure 1	32	Flat pack
X	GDIP1-T32 or CDIP2-T32	32	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	See figure 1	32	Gullwing lead chip carrier

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1.2.5 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 <u>Absolute maximum ratings</u>. <u>1</u>/

Endurance:
Device types 01-04, 09 . . . . 10,000 cycles/byte, minimum
Device types 05-08 . . . . 1,000 cycles/byte, minimum
Device types 10-13 . . . . 100,000 cycles/byte, minimum
Supply voltage range (V_{CC}) <u>2</u>/ . . . . -2.0 V dc to +7.0 V dc
Storage temperature range (T_{stg}) . . . . -65°C to +150°C
Maximum power dissipation (P_D) . . . . 1.0 W
Lead temperature (soldering, 10 seconds) . . . . +300°C
Junction temperature (T_J) <u>3</u>/ . . . . +150°C
Thermal resistance, junction-to-case (Θ_{JC}) (case outline X, Y) . . . . . . See MIL-STD-1835
Thermal resistance, junction-to-case (Θ_{JC}) (case outlines T, Z) . . . . . . 13°C/W
Thermal resistance, junction-to-case (Θ_{JC}) (case outline U) . . . . 27°C/W
Voltage on any pin with respect to ground <u>2</u>/ . . . . -2.0 V dc to +7.0 V dc
Voltage on pin A_9 with respect to ground <u>4</u>/ . . . . -2.0 V dc to +13.5 V dc
V_{PP} supply voltage with respect to ground <u>4</u>/ . . . . -2.0 V dc to +14.0 V dc
V_{CC} supply voltage with respect to ground <u>2</u>/ . . . . -2.0 V dc to +7.0 V dc
Output short circuit current <u>5</u>/ . . . . 200 mA
Data retention . . . . 10 years minimum

1.4 <u>Recommended operating conditions</u>. <u>6</u>/

Supply voltage range (V_{CC}) . . . . +4.5 V dc to +5.5 V dc
Operating temperature range (T_{case}) . . . . -55°C to +125°C
Low level input voltage range (V_{IL}) . . . . -0.5 V dc to +0.8 V dc
High level input voltage range (V_{IH}) . . . . +2.0 V dc to V_{CC} +0.5 V dc
High level input voltage range, CMOS (V_{IH}) . . . . V_{CC} -0.5 V dc to V_{CC} +0.5 V dc
Chip clear (V_P) . . . . 11.4 V dc to 12.6 V dc

1.5 <u>Digital logic testing for device classes Q and V</u>.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) . . . . 100 percent

_____

<u>1</u>/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
<u>2</u>/ Minimum dc voltage on input or V_O pins is -0.5 V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum dc voltage on output and V_O pins is V_{CC} +0.5 V. During voltage transitions outputs may overshoot to V_{CC} +2.0 V for periods up to 20 ns.
<u>3</u>/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
<u>4</u>/ Minimum dc input voltage on A_9 or V_{PP} may overshoot to +14.0 V for periods less than 20 ns.
<u>5</u>/ No more than one output shorted at a time. Duration of short circuit should not be greater than 1 second.
<u>6</u>/ All voltages are referenced to V_{SS} (ground).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

  DEPARTMENT OF DEFENSE

    MIL-PRF-38535   - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

  DEPARTMENT OF DEFENSE

    MIL-STD-883   -   Test Method Standard Microcircuits.
    MIL-STD-973   -   Configuration Management.
    MIL-STD-1835   -   Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

  DEPARTMENT OF DEFENSE

    MIL-HDBK-103 -   List of Standard Microcircuit Drawings (SMD's).
    MIL-HDBK-780 -   Standard Microcircuit Drawings.

  (Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

  AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

    ASTM Standard F1192-95   -   Standard Guide for the Measurement of Single Event Phenomena from
                                                  Heavy Ion Irradiation of Semiconductor Devices.

      (Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

  ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

    JEDEC Standard EIA/JESD78   -   IC Latch-Up Test.

  (Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Blvd., Arlington, VA 22201.)

  (Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 <u>Case outline(s)</u>. The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.

3.2.3 <u>Truth tables</u>. The truth tables shall be as specified on figure 3.

3.2.3.1 <u>Unprogrammed devices</u>. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3 herein. When required, in screening (see 4.2 herein), or quality conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.3.2 <u>Programmed devices</u>. The requirements for supplying programmed devices are not part of this document.

3.2.3.3 <u>Command definitions</u>. The command definitions table shall be as specified on figure 3.

3.2.4 <u>Switching test circuits and waveforms</u>. The switching test circuits and waveforms shall be as specified on figure 4.

3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change for device class M</u>. For device class M, notification to DSCC-VA of change of product (see 6.2 - herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ 1/ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
DC CHARACTERISTICS							
Input leakage current	I_{LI}	$V_{CC} = V_{CC}$ max, $V_{IN} = V_{CC}$ max or V_{SS}	1, 2, 3	All		±1.0	µA
Output leakage current	I_{LO}	$V_{CC} = V_{CC}$ max, $V_{OUT} = V_{CC}$ max or V_{SS}	1, 2, 3	All		±10	µA
V_{CC} standby current (TTL)	I_{CCS1}	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IH}$	1, 2, 3	All		1.0	mA
V_{CC} standby current (CMOS)	I_{CCS2}	$\overline{CE} = V_{CC} \pm 0.2\ V$, $V_{CC} = V_{CC}$ max	1, 2, 3	All		100	µA
V_{CC} active read current	I_{CC1}	$V_{CC} = V_{CC}$ max, $\overline{CE} = V_{IL}$ $I_{OUT} = 0$ mA, $f = 6.0$ MHz, $\overline{OE} = V_{IH}$	1, 2, 3	All		30	mA
V_{CC} programming current	I_{CC2}	$\overline{CE} = V_{IL}$, programming in progress	1, 2, 3	All		30 2/	mA
V_{CC} erase current	I_{CC3}	$\overline{CE} = V_{IL}$, erasure in progress	1, 2, 3	All		30 2/	mA
V_{PP} standby current	I_{PPS}	$V_{PP} = V_{PPL}$	1, 2, 3	All		±10	µA
V_{PP} read current	I_{PP1}	$V_{PP} = V_{PPH}$	1, 2, 3	All		200	µA
		$V_{PP} = V_{PPL}$				±10	
V_{PP} programming current	I_{PP2}	$V_{PP} = V_{PPH}$, programming in progress	1, 2, 3	All		30 2/	mA

See footnotes at end of table.

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STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	**A**			
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TABLE I. Electrical performance characteristics - Continued.							
Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ 1/ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
DC CHARACTERISTICS - Continued							
V_{PP} erase current	I_{PP3}	$V_{PP} = V_{PPH}$ erasure in progress	1, 2, 3	All		30 2/	mA
Low level input voltage	V_{IL}		1, 2, 3	All	-0.5 2/	0.8	V
High level input voltage (TTL)	V_{IH1}		1, 2, 3	All	2.0	V_{CC}+ 0.5 2/	V
High level input voltage (CMOS)	V_{IH2}		1, 2, 3	All	0.7 V_{CC}	V_{CC}+ 0.5 2/	V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA, $V_{CC} = V_{CC}$ min	1, 2, 3	All		0.45	V
High level output voltage (TTL)	V_{OH1}	I_{OH} = -2.5 mA, $V_{CC} = V_{CC}$ min	1, 2, 3	All	2.4		V
High level output voltage (CMOS)	V_{OH2}	I_{OH} = -2.5 mA, $V_{CC} = V_{CC}$ min	1, 2, 3	All	0.85 V_{CC}		V
	V_{OH3}	I_{OH} = -100 µA, $V_{CC} = V_{CC}$ min			V_{CC}- 0.4 2/		V
A9 auto select voltage	V_{ID}	A9 = V_{ID}	1, 2, 3	All	11.5	13.0	V
A9 auto select current	I_{ID}	A9 = V_{ID} max, $V_{CC} = V_{CC}$ max	1, 2, 3	All		500 2/	µA
V_{PP} during read only operations	V_{PPL}	NOTE: erase/program are inhibited when $V_{PP} = V_{PPL}$	1, 2, 3	All	0	V_{CC}+ 2.0 2/	V
V_{PP} during read/write operations	V_{PPH}		1, 2, 3	All	11.4	12.6	V
Functional tests		See 4.4.1d	7, 8A, 8B	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T$_C$ ≤ +125°C 1/ 4.5 V ≤ V$_{CC}$ ≤ 5.5 V unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
CAPACITANCE 2/							
Input capacitance	C$_{IN1}$	V$_{IN}$ = 0 V, T$_A$ = 25°C, f = 1.0 Mhz, see 4.4.1c	4	All		10	pF
Output capacitance	C$_{OUT}$	V$_{OUT}$ = 0 V, T$_A$ = 25°C, f = 1.0 Mhz, see 4.4.1c	4	All		12	pF
V$_{PP}$ input capacitance	C$_{IN2}$	V$_{IN}$ = 0 V, T$_A$ = 25°C, f = 1.0 Mhz, see 4.4.1c	4	All		12	pF
AC CHARACTERISTICS - READ ONLY OPERATIONS (See figure 5 as applicable.)							
Read cycle time	t$_{AVAV}$	2/	9, 10, 11	01,05,10 02,06,11 03,07,12 04,08,13 09	250 200 150 120 90		ns
Chip enable access time	t$_{ELQV}$		9, 10, 11	01,05,10 02,06,11 03,07,12 04,08,13 09		250 200 150 120 90	ns
Address access time	t$_{AVQV}$		9, 10, 11	01,05,10 02,06,11 03,07,12 04,08,13 09		250 200 150 120 90	ns

See footnotes at end of table.

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ 1/ $4.5 V \leq V_{CC} \leq 5.5 V$ unless otherwise specified	Group A Subgroups	Device type	Limits Min	Limits Max	Units
AC CHARACTERISTICS - READ ONLY OPERATIONS - Continued. (See figure 5 as applicable.)							
Output enable access time	t_{GLQV}		9, 10, 11	01,05 02,06 03,07,10, 11,12 04,08,13 09		65 60 55 50 40	ns
Chip enable to output in low Z	t_{ELQX}		9, 10, 11	All	0 2/		ns
Chip disable to output in high Z	t_{EHQZ}	2/	9, 10, 11	All		55	ns
Output enable to output in low Z	t_{GLQX}		9, 10, 11	All	0 2/		ns
Output disable to output in high Z	t_{GHQZ}	2/	9, 10, 11	01,05 02,06 03,07,10, 11,12 04,08,09, 13		60 45 35 30	ns
Output hold from address, $\overline{CE}$, or $\overline{OE}$ change	t_{AXQX}	3/	9, 10, 11	All	0 2/		ns
Write recovery time before read	t_{WHGL}		9, 10, 11	All	6.0		µs
ERASE AND PROGRAMMING PERFORMANCE							
Chip erase		Excludes 00H programming	9, 10, 11	All		60	s
Chip program		Excludes system overhead 4/	9, 10, 11	All		24	s

1/ Case temperatures are instant on.
2/ Parameters shall be tested as part of device initial characterization and after design and process change. Parameter
   shall be guaranteed to the limits specified in table I for all lots not specifically tested.
3/ Whichever occurs first.
4/ Minimum byte programming time excluding system overhead is 16 µs (10 µs programming +6.0 µs write recovery), while
   maximum is 400 µs/byte (16 µs x 25 loops allowed by algorithm). Maximum chip programming time is specified lower
   than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst
   case byte.

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3.9 <u>Verification and review for device class M</u>. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 <u>Microcircuit group assignment for device class M</u>. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

3.11 <u>Processing of EEPROMs</u>. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 <u>Conditions of the supplied devices</u>. Devices will be supplied in an unprogrammed or clear state. No provision will be made for supplying programmed devices.

3.11.2 <u>Erasure of EEPROMs</u>. When specified, devices shall be erased in accordance with procedures and characteristics specified in 4.5.1.

3.11.3 <u>Programming of EEPROMs</u>. When specified, devices shall be programmed in accordance with procedures and characteristics specified in 4.5.2.

3.11.4 <u>Verification of state of EEPROMs</u>. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

3.12 <u>Endurance</u>. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.13 <u>Data retention</u>. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

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Case T

NOTE: Metric equivalents are given in parenthesis.

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.057	.080	1.45	2.03	
A_1	.122	.159	3.10	4.04	Solid lid
A_2	.010	.014	0.25	0.36	Solid lid
A_3	.055	.065	1.38	1.65	
ϕB	.014	.018	0.36	0.46	
CP	.000	.004	0.00	0.10	
D	.540	.565	13.72	14.35	
D_1	.400		10.16		Reference
D_2	.500		12.70		
E	.440	.464	11.17	11.79	
E_1	.300		7.62		Reference
E_2	.400		10.16		
e	.043	.057	1.09	1.45	Typical
R	0.027	0.033	0.68	0.84	
N	32				

FIGURE 1. Case outlines.

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Case U

NOTES 1 AND 2

.050 ±.005

.017 ±.002
32 PLACES

1   32

16   17

.045 MAX
4 PLACES

.005 MIN TYP

.820
±.010

.295 ±.020   .410 ±.006   .295 ±.020

.132 MAX

.034
±.008 TYP

.050
±.015

.005 ±.002
32 PLACES

.280 ±.006 TYP
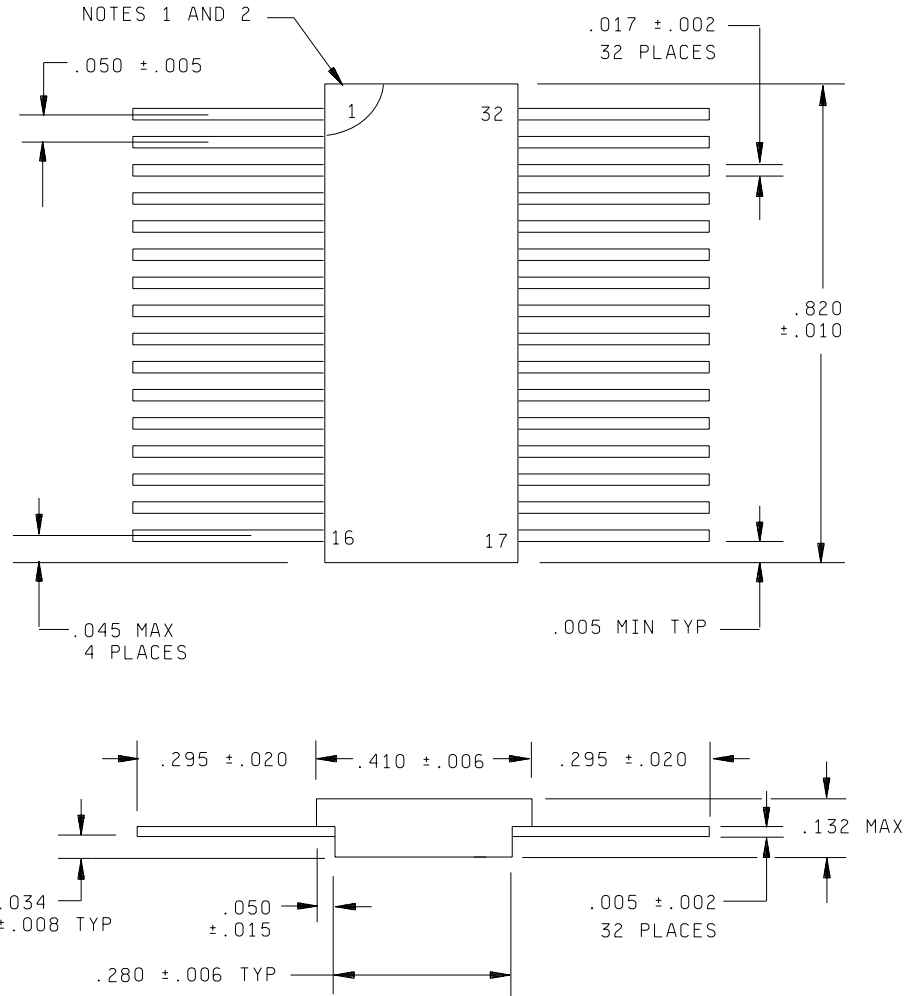
Inches	mm	Inches	mm
.001	0.03	.040	1.02
.002	0.05	.045	1.15
.005	0.13	.050	1.27
.006	0.15	.132	3.35
.008	0.20	.295	7.49
.017	0.43	.280	7.11
.020	0.51	.410	10.41
.034	0.86	.820	20.83

NOTES:
1. Terminal one shall be identified by a mechanical index on the lead or body, or a mark on the top surface within the region shown.
2. Terminal identification numbers need not appear on the package.
3. Weight: 1.5 g maximum.
4. Dimensions are in inches.
5. Metric equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

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Case Z
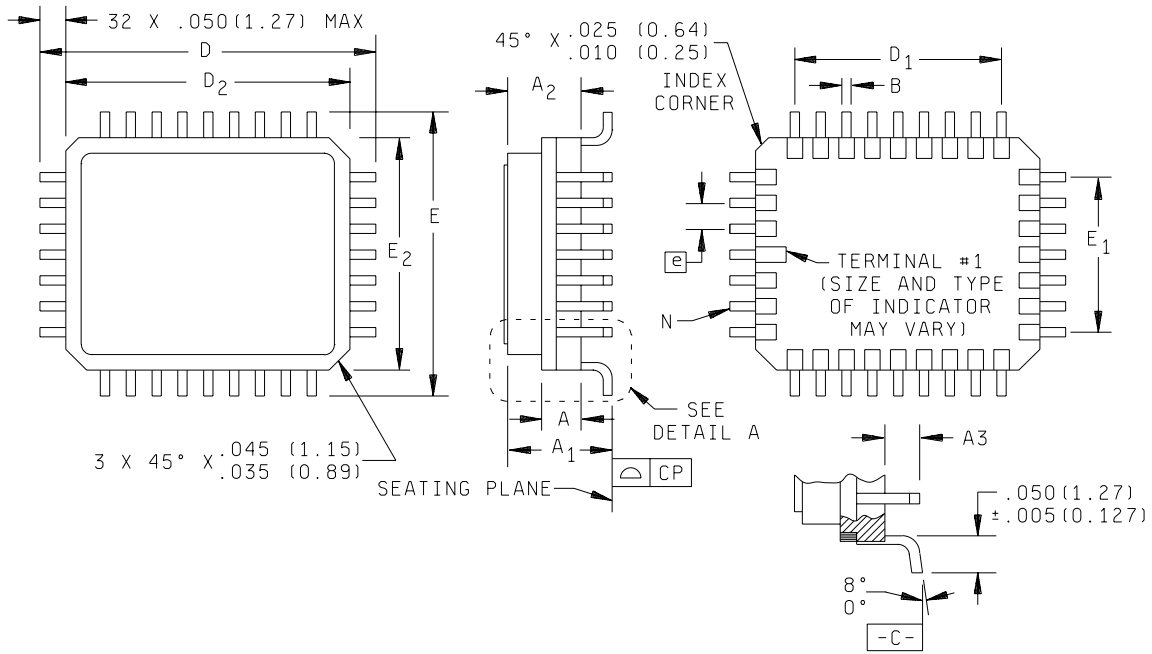
NOTE: METRIC EQUIVALENTS ARE GIVEN IN PARENTHESIS.

DETAIL A

Family: Ceramic leadless chip carrier					
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.057	.080	1.45	2.03	
A$_1$	.122	.159	3.10	4.04	Solid lid
A$_2$	.010	.014	0.25	0.36	Solid lid
A$_3$	.055	.065	1.40	1.65	
B	.014	.018	0.36	0.46	
CP	.000	.004	0.00	0.10	
D		.670		17.01	
D$_1$	.400		10.16		Reference
D$_2$	.540	.560	13.71	14.22	
E		.570		14.49	
E$_1$	.300		7.62		Reference
E$_2$	.440	.460	11.18	11.68	
e	.043	.057	1.09	1.45	Typical
N	32				

FIGURE 1. Case outlines - Continued.

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Device types	All
Case outlines	All
Terminal number	Terminal symbol
1	V_{PP}
2	A_{16}
3	A_{15}
4	A_{12}
5	A_7
6	A_6
7	A_5
8	A_4
9	A_3
10	A_2
11	A_1
12	A_0
13	DQ_0
14	DQ_1
15	DQ_2
16	V_{SS}
17	DQ_3
18	DQ_4
19	DQ_5
20	DQ_6
21	DQ_7
22	$\overline{CE}$
23	A_{10}
24	$\overline{OE}$
25	A_{11}
26	A_9
27	A_8
28	A_{13}
29	A_{14}
30	NC
31	$\overline{WE}$
32	V_{CC}

FIGURE 2. Terminal connections.

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Bus operations

Pins		V_{PP} 1/	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$DQ_0 - DQ_7$
Read only	Operation							
	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data out
	Output disable	V_{PPL}	X 2/	X 2/	V_{IL}	V_{IH}	V_{IH}	3-state
	Standby	V_{PPL}	X 2/	X 2/	V_{IH}	X 2/	X 2/	3-state
	Auto-select manufacturer code 3/	V_{PPL}	V_{IL}	V_{ID} 4/	V_{IL}	V_{IL}	V_{IH}	5/
	Auto-select device code 3/	V_{PPL}	V_{IH}	V_{ID} 4/	V_{IL}	V_{IL}	V_{IH}	6/
Read/write	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data out 7/
	Output disable	V_{PPH}	X 2/	X 2/	V_{IL}	V_{IH}	V_{IH}	3-state
	Standby 8/	V_{PPH}	X 2/	X 2/	V_{IH}	X 2/	X 2/	3-state
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data in 9/

1/ Refer to dc characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2/ X can be V_{IL} or V_{IH}.
3/ Manufacture and device code may also be accessed via a command register write sequence.
4/ V_{ID} is the auto select high voltage. Refer to dc characteristics.
5/ The output for $DQ_0 - DQ_7$ shall be as follows:

   $DQ_0 - DQ_7$
   _____
   DATA = 89H
   DATA = 01H

6/ The output for $DQ_0 - DQ_7$ shall be as follows:

   $DQ_0 - DQ_7$
   _____
   DATA = B4H (device types 01-09, 11-13)
   DATA = A7H (device types 01-09)
   DATA = A2H (device types 10-13)

7/ Read operations with $V_{PP} = V_{PPH}$ may access array data or the auto select codes.
8/ With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
9/ Refer to command definitions for valid Data-In during a write operation.

FIGURE 3. Truth tables.

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Command definitions, device types 01-09

Command	BUS cycles required	First BUS cycle			Second BUS cycle		
		Operation 1/	Address 2/	Data 3/	Operation 1/	Address 2/	Data 3/
Read memory	1	Write	X	00H/FFH	Read	RA	RD
Read auto select codes 4/	2	Write	X	90H/80H	Read	IA	ID
Setup erase/erase	2	Write	X	20H	Write	X	20H
Erase verify	2	Write	EA	A0H	Read	X	EVD
Setup program/program	2	Write	X	40H	Write	PA	PD
Program verify	2	Write	X	C0H	Read	X	PVD
Reset 5/	2	Write	X	FFH	Write	X	FFH

1/ Refer to BUS operations for definitions.
2/ RA = Address of the memory location to be read.
   IA = Identifier address: 00H/01H for manufacturer code, 01H/A7H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Address are latched on the falling edge of the write-enable pulse.
3/ RD = Data read from location RA during read operation.
   ID = Data read from location IA during device identification.
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of write-enable.
   PVD = Data read from location PA during program verify. PA is latched on the program command.
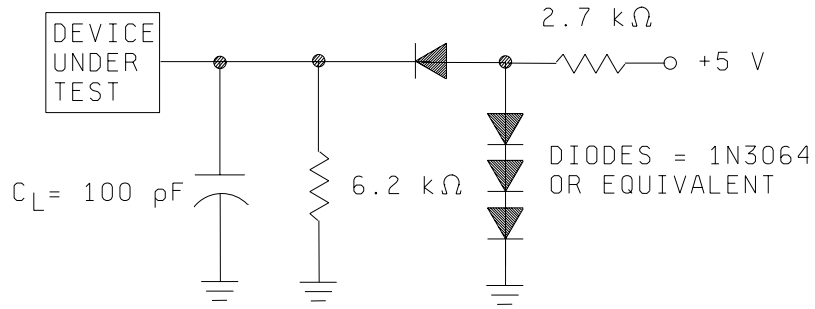4/ Following the read Auto Select code ID command, two read operations access manufacturer and device codes.
5/ The second bus cycle must be followed by the desired command register write.

Command definitions, device types 10-13

Command	BUS cycles required	First BUS cycle			Second BUS cycle		
		Operation 1/	Address 2/	Data 3/	Operation 1/	Address 2/	Data 3/
Read memory	1	Write	X	00H/FFH	Read	RA	RD
Read auto select codes 4/	3	Write	X	80H/90H	Read	00H/01H	01H/A2H
Embedded erase setup/erase	2	Write	X	30H	Write	X	30H
Embedded program setup/program	2	Write	X	10H/50H	Write	PA	PD
Reset 5/	2	Write	X	FFH	Write	X	FFH

1/ Refer to BUS operations for definitions.
2/ RA = Address of the memory location to be read.
   PA = Address of memory location to be programmed.
   Address are latched on the falling edge of the $\overline{WE}$ pulse.
3/ RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
4/ Following the read Auto Select code ID command, two read operations access manufacturer and device codes.
5/ The second bus cycle must be followed by the desired command register write.
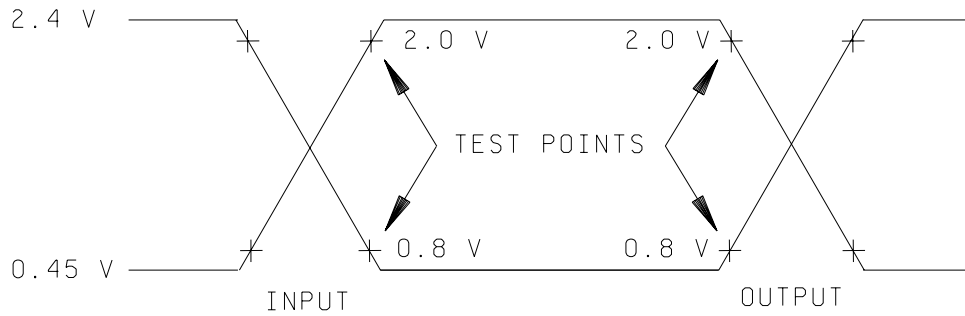

FIGURE 3. Truth tables - Continued.

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DEVICE
UNDER
TEST

2.7 kΩ

+5 V

C_L = 100 pF

6.2 kΩ

DIODES = 1N3064
OR EQUIVALENT

SWITCHING TEST CIRCUIT
OR EQUIVALENT

C_L INCLUDES JIG CAPACITANCE

2.4 V

2.0 V   2.0 V

TEST POINTS

0.45 V

0.8 V   0.8 V

INPUT   OUTPUT

AC testing: Inputs are driven at 2.4 V for a
logic "1" and 0.45 V for a logic "0". Input pulse
rise and fall times are ≤ 10 ns.

FIGURE 4. Switching test circuits and waveforms.

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AC waveforms for read operations
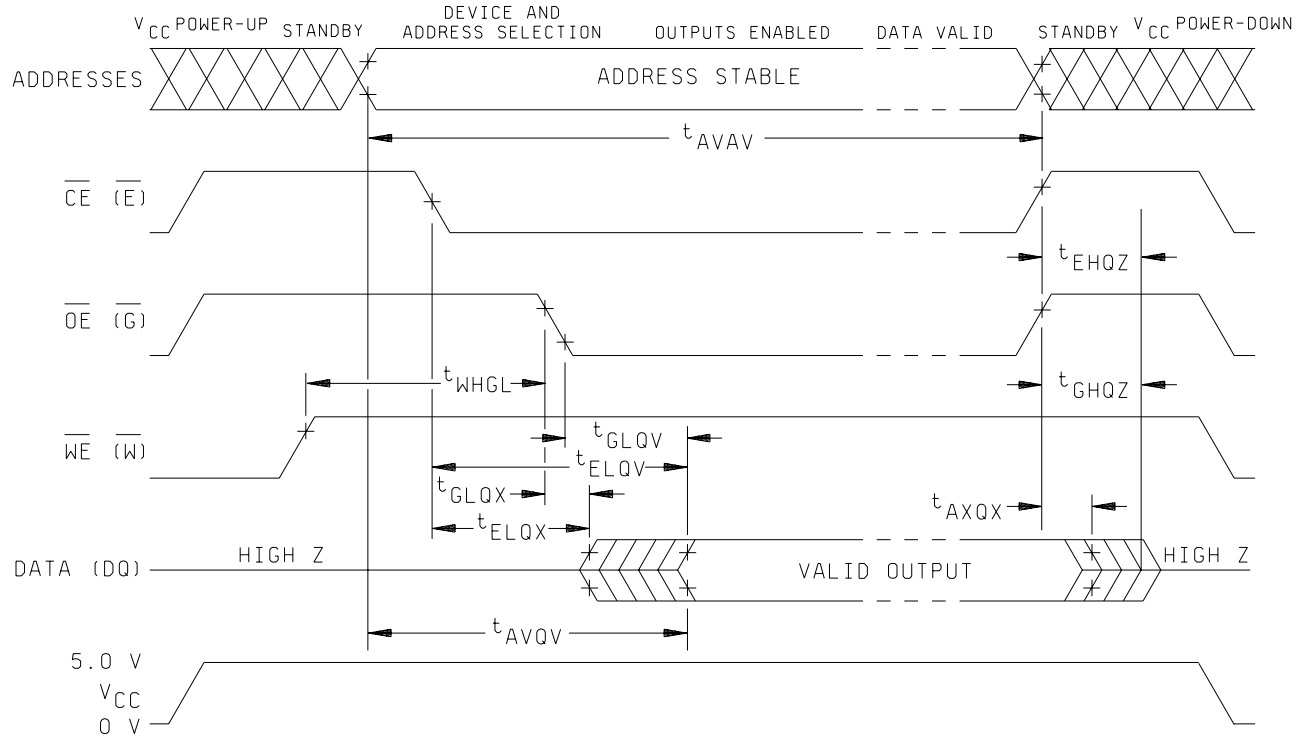
FIGURE 4. Switching test circuits and waveforms - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 <u>Additional criteria for device class M</u>.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.5.2 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot.

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

   (1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. After the completion of all screening, the device shall be erased and verified prior to delivery.

4.2.2 <u>Additional criteria for device classes Q and V</u>.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535 and as detailed in table IIB herein.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE IIA. <u>Electrical test requirements</u>. <u>1</u>/ <u>2</u>/ <u>3</u>/ <u>4</u>/ <u>5</u>/ <u>6</u>/ <u>7</u>/

Line no.	Test requirements	Subgroups (per method 5005, table I) Device class M	Subgroups (per MIL-PRF-38535, table III) Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 2,8A,10
2	Static burn-in I method 1015	Not required	Not required	Not required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7,8A, 8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,8A,10	1,2,3,7 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,8A,10	2,3,7 8A,8B	2,3,7 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

<u>1</u>/   Blank spaces indicate test are not applicable.
<u>2</u>/   Any or all subgroups may be combined when using high-speed testers.
<u>3</u>/   Subgroups 7 and 8 functional tests shall verify the truth table.
<u>4</u>/   * Indicates PDA applies to subgroups 1 and 7.
<u>5</u>/   ** See 4.4.1c.
<u>6</u>/   Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
<u>7</u>/   See 4.4.1e.

4.4.1   <u>Group A inspection</u>.

a.   Tests shall be as specified in table IIA herein.

b.   Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

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c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups B, C, and D testing).

4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 <u>Additional criteria for device class M</u>.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The device selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. After the completion of all testing, the devices shall be cleared and verified prior to delivery.

4.4.2.2 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified.

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TABLE IIB. Delta limits at 25°C.

Test 1/	Device types
	All
I_{CCS2} standby	±10 percent of specified value in table I.
I_{LI}	±10 percent of specified value in table I.
I_{LO}	±10 percent of specified value in table I.

1/ The above parameter shall be recorded before and after
the required burn-in and life tests to determine delta.

   4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q, and V shall be as specified in MIL-PRF-38535.

   a. End-point electrical parameters shall be as specified in table IIA herein.

   b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

   c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

   4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate figures and tables as follows.

   4.5.1 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be available upon request.

   4.5.2 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

   4.6 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

   5. PACKAGING

   5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

   6. NOTES

   6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

   6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

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...

6.1.2 <u>Substitutability</u>. Device class Q devices will replace device class M devices.

6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 <u>Record of users</u>. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.
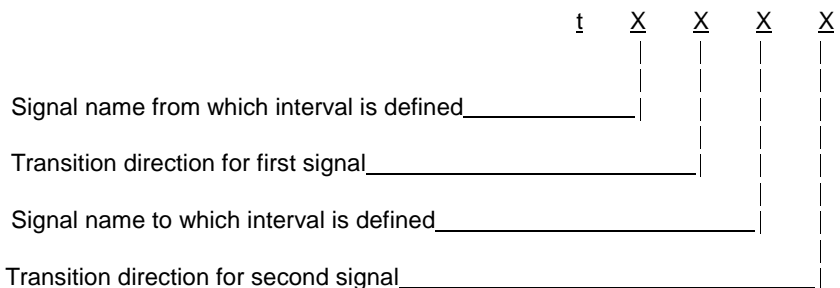
6.4 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

C_{IN}, C_{OUT} . . . . Input and bidirectional output, terminal-to-GND capacitance.
GND . . . . Ground zero voltage potential.
I_{CC} . . . . Supply current.
I_{IL} . . . . Input current low.
I_{IH} . . . . Input current high.
T_C . . . . Case temperature.
T_A . . . . Ambient temperature.
V_{CC} . . . . Positive supply voltage.
V_H . . . . Output enable and Write enable voltage during chip erase.
O/V . . . . Latchup over-voltage.

6.5.1 <u>Timing limits</u>. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 <u>Timing parameter abbreviations</u>. All timing abbreviations use lower case characters with upper case subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:

$$t \quad X \quad X \quad X \quad X$$

Signal name from which interval is defined_____|

Transition direction for first signal_____|

Signal name to which interval is defined_____|

Transition direction for second signal_____|

a. Signal definitions:
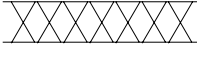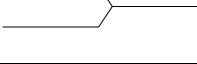
A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
G = Output enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

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6.5.3 <u>Waveforms</u>.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WIIL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 <u>Sources of supply</u>.

6.6.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 <u>Approved sources of supply for device class M</u>. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

	SIZE A		5962-90899
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DSCC FORM 2234
APR 97

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-11-16

Approved sources of supply for SMD 5962-90899 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9089901QXA	0EU86	SMJ28F010B-25JDDM
5962-9089901MXX	3/	AM28F010-250/BXA
	3/	MD28F010-25/B
5962-9089901QYA	0EU86	SMJ28F010B-25FEM
5962-9089901MYX	3/	AM28F010-250/BUA
	3/	MR28F010-25/B
5962-9089901MTX	3/	MT28F010-25/B
5962-9089901MZX	3/	MZ28F010-25/B
5962-9089901QUA	0EU86	SMJ28F010B-25HKM
5962-9089901MUX	3/	MF28F010-25/B
5962-9089902QXA	0EU86	SMJ28F010B-20JDDM
5962-9089902MXX	3/	AM28F010-200/BXA
	3/	MD28F010-20/B
5962-9089902QYA	0EU86	SMJ28F010B-20FEM
5962-9089902MYX	3/	AM28F010-200/BUA
	3/	MR28F010-20/B
5962-9089902MTX	3/	MT28F010-20/B
5962-9089902MZX	3/	MZ28F010-20/B
5962-9089902QUA	0EU86	SMJ28F010B-20HKM
5962-9089902MUX	3/	MF28F010-20/B
5962-9089903QXA	0EU86	SMJ28F010B-15JDDM
5962-9089903MXX	3/	AM28F010-150/BXA
	3/	MD28F010-15/B
5962-9089903QYA	0EU86	SMJ28F010B-15FEM
5962-9089903MYX	3/	AM28F010-150/BUA
	3/	MR28F010-15/B
5962-9089903MTX	3/	MT28F010-15/B
5962-9089903MZX	3/	MZ28F010-15/B
5962-9089903QUA	0EU86	SMJ28F010B-15HKM
5962-9089903MUX	3/	MF28F010-15/B
5962-9089904QXA	0EU86	SMJ28F010B-12JDDM
5962-9089904MXX	3/	AM28F010-120/BXA
	3/	MD28F010-12/B
5962-9089904QYA	0EU86	SMJ28F010B-12FEM
5962-9089904MYX	3/	AM28F010-120/BUA
	3/	MR28F010-12/B
5962-9089904MTX	3/	MT28F010-12/B
5962-9089904MZX	3/	MZ28F010-12/B
5962-9089904QUA	0EU86	SMJ28F010B-12HKM
5962-9089904MUX	3/	MF28F010-12/B

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9089905QXA	0EU86	SMJ28F010B-25JDDM
5962-9089905MXX	3/	AM28F010-250C3/BXA
	3/	MD28F010-25/B
5962-9089905QYA	0EU86	SMJ28F010B-25FEM
5962-9089905MYX	3/	AM28F010-250C3/BUA
	3/	MR28F010-25/B
5962-9089905MTX	3/	MT28F010-25/B
5962-9089905MZX	3/	MZ28F010-25/B
5962-9089905QUA	0EU86	SMJ28F010B-25HKM
5962-9089905MUX	3/	MF28F010-25/B
5962-9089906QXA	0EU86	SMJ28F010B-20JDDM
5962-9089906MXX	3/	AM28F010-200C3/BXA
	3/	MD28F010-20/B
5962-9089906QYA	0EU86	SMJ28F010B-20FEM
5962-9089906MYX	3/	AM28F010-200C3/BUA
	3/	MR28F010-20/B
5962-9089906MTX	3/	MT28F010-20/B
5962-9089906MZX	3/	MZ28F010-20/B
5962-9089906QUA	0EU86	SMJ28F010B-20HKM
5962-9089906MUX	3/	MF28F010-20/B
5962-9089907QXA	0EU86	SMJ28F010B-15JDDM
5962-9089907MXX	3/	AM28F010-150C3/BXA
	3/	MD28F010-15/B
5962-9089907QYA	0EU86	SMJ28F010B-15FEM
5962-9089907MYX	3/	AM28F010-150C3/BUA
	3/	MR28F010-15/B
5962-9089907MTX	3/	MT28F010-15/B
5962-9089907MZX	3/	MZ28F010-15/B
5962-9089907QUA	0EU86	SMJ28F010B-15HKM
5962-9089907MUX	3/	MF28F010-15/B
5962-9089908QXA	0EU86	SMJ28F010B-12JDDM
5962-9089908MXX	3/	AM28F010-120C3/BXA
	3/	MD28F010-12/B
5962-9089908QYA	0EU86	SMJ28F010B-12FEM
5962-9089908MYX	3/	AM28F010-120C3/BUA
	3/	MR28F010-12/B
5962-9089908MTX	3/	MT28F010-12/B
5962-9089908MZX	3/	MZ28F010-12/B
5962-9089908QUA	0EU86	SMJ28F010B-12HKM
5962-9089908MUX	3/	MF28F010-12/B
5962-9089909MXX	3/	MD28F010-90/B
5962-9089909MYX	3/	MR28F010-90/B
5962-9089909MTX	3/	MT28F010-90/B
5962-9089909MZX	3/	MZ28F010-90/B
5962-9089909MUX	3/	MF28F010-90/B
5962-9089910QXA	0EU86	SMJ28F010B-25JDDM
5962-9089910MXX	3/	AM28F010A-250/BXA
5962-9089910QYA	0EU86	SMJ28F010B-25FEM
5962-9089910MYX	3/	AM28F010A-250/BUA
5962-9089910QUA	0EU86	SMJ28F010B-25HKM

See footnotes at end of table.

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9089911QXA	0EU86	SMJ28F010B-20JDDM
5962-9089911QYA	0EU86	SMJ28F010B-20FEM
5962-9089911MXX	3/	AM28F010A-200/BXA
5962-9089911MYX	3/	AM28F010A-200/BUA
5962-9089911QUA	0EU86	SMJ28F010B-20HKM
5962-9089912QXA	0EU86	SMJ28F010B-15JDDM
5962-9089912QYA	0EU86	SMJ28F010B-15FEM
5962-9089912MXX	3/	AM28F010A-150/BXA
5962-9089912MYX	3/	AM28F010A-150/BUA
5962-9089912QUA	0EU86	SMJ28F010B-15HKM
5962-9089913QXA	0EU86	SMJ28F010B-12JDDM
5962-9089913QYA	0EU86	SMJ28F010B-12FEM
5962-9089913MXX	3/	AM28F010A-120/BXA
5962-9089913MYX	3/	AM28F010A-120/BUA
5962-9089913QUA	0EU86	SMJ28F010B-12HKM

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address	Manufacturer code	Device code
0EU86	Austin Semiconductor Inc. 8701 Cross Park Drive Austin, TX 78754-4566	97	B4H

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