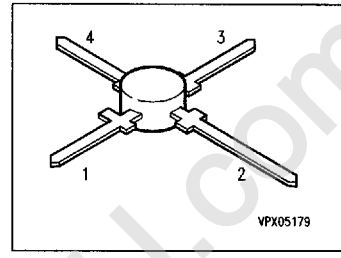
SIEMENS

Silicon N Channel MOSFET Tetrode

BF 963

- For high-gain, low-distortion VHF TV and FM mixer and input stages



Type	Marking	Ordering Code	Pin Configuration 1	2	3	4	Package[1]
BF 963	–	Q62702-F904	S	D	G_2	G_1	X-plast

Maximum Ratings

Parameter	Symbol	Values	Unit
Drain-source voltage	V_{DS}	20	V
Drain current	I_D	50	mA
Gate 1/gate 2 peak source current	$\pm I_{G1/2SM}$	10	
Total power dissipation, $T_A \leq 60$ °C	P_{tot}	200	mW
Storage temperature range	T_{stg}	– 55 ... + 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Junction - ambient	$R_{th\,JA}$	≤ 450	K/W

[1] For detailed information see chapter Package Outlines.

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Electrical Characteristics
at T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 10 µA, $-V_{G1S} = -V_{G2S}$ = 4 V	$V_{(BR)DS}$	20	–	–	V
Gate 1 source breakdown voltage $\pm I_{G1S}$ = 10 mA, $V_{G2S} = V_{DS}$ = 0	$\pm V_{(BR)G1SS}$	8.5	–	14	
Gate 2 source breakdown voltage $\pm I_{G2S}$ = 10 mA, $V_{G1S} = V_{DS}$ = 0	$\pm V_{(BR)G2SS}$	8.5	–	14	
Gate 1 source leakage current $\pm V_{G1S}$ = 5 V, $V_{G2S} = V_{DS}$ = 0	$\pm I_{G1SS}$	–	–	50	nA
Gate 2 source leakage current $\pm V_{G2S}$ = 5 V, $V_{G1S} = V_{DS}$ = 0	$\pm I_{G2SS}$	–	–	50	
Drain current V_{DS} = 15 V, V_{G1S} = 0, V_{G2S} = 4 V	I_{DSS}	6	–	40	mA
Gate 1 source pinch-off voltage V_{DS} = 15 V, V_{G2S} = 4 V, I_D = 20 µA	$-V_{G1S(p)}$	–	–	2.5	V
Gate 2 source pinch-off voltage V_{DS} = 15 V, V_{G1S} = 0, I_D = 20 µA	$-V_{G2S(p)}$	–	–	2.0	
AC Characteristics					
Forward transconductance V_{DS} = 15 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 kHz	g_{fs}	16	25	–	mS
Gate 1 input capacitance V_{DS} = 15 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{g1ss}	–	6	–	pF
Gate 2 input capacitance V_{DS} = 15 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{g2ss}	–	2.5	–	
Feedback capacitance V_{DS} = 15 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{dg1}	–	50	–	fF
Output capacitance V_{DS} = 15 V, I_D = 10 mA, V_{G2S} = 4 V, f = 1 MHz	C_{dss}	–	2.5	–	pF
Power gain, V_{DS} = 15 V, I_D = 10 mA, f = 200 MHz, G_G = 2.5 mS, G_L = 0.8 mS $2\Delta f$ = 12 MHz (test circuit)	G_{ps}	–	25	–	dB
Noise figure, V_{DS} = 15 V, I_D = 10 mA f = 200 MHz, G_G = 2.5 mS, G_L = 0.8 mS (test circuit)	F	–	1.5	–	

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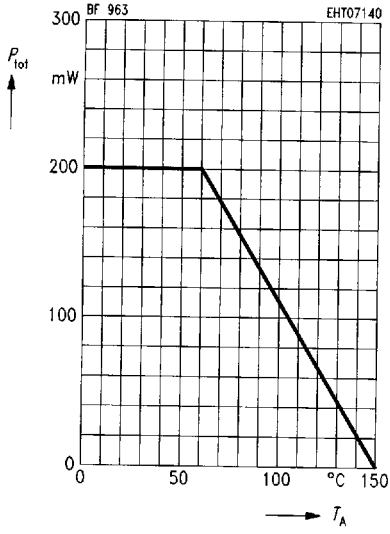
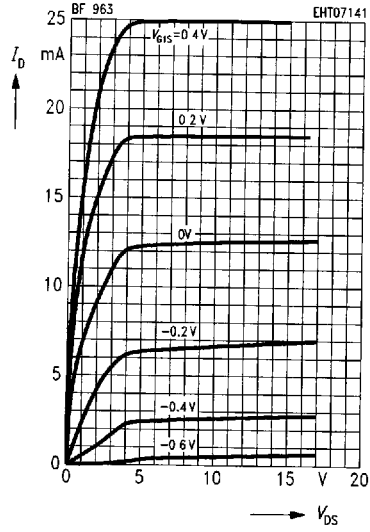
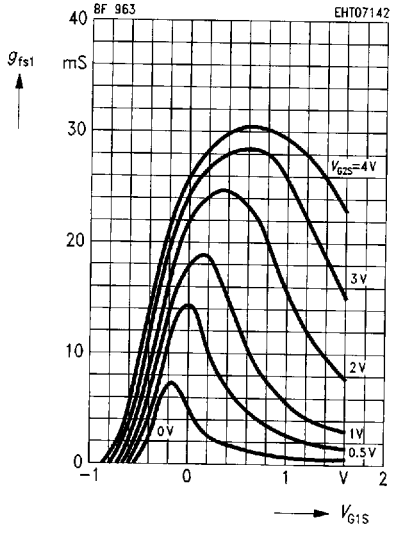
Total power dissipation $P_{tot} = f(T_A)$



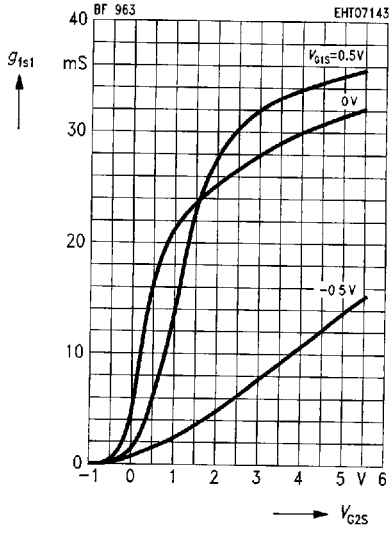
Output characteristics $I_D = f(V_{DS})$
V_{G2S} = 4 V



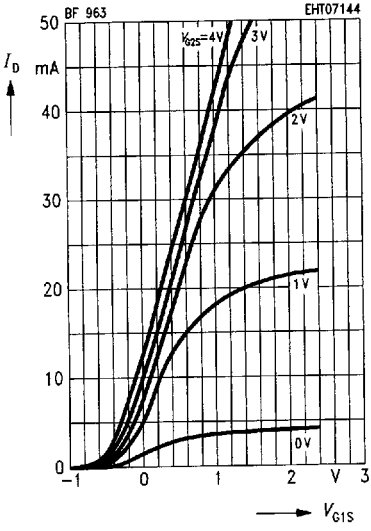
Gate 1 forward transconductance
$g_{fs1} = f(V_{G1S})$
V_{DS} = 15 V
I_{DSS} = 10 mA, f = 1 kHz



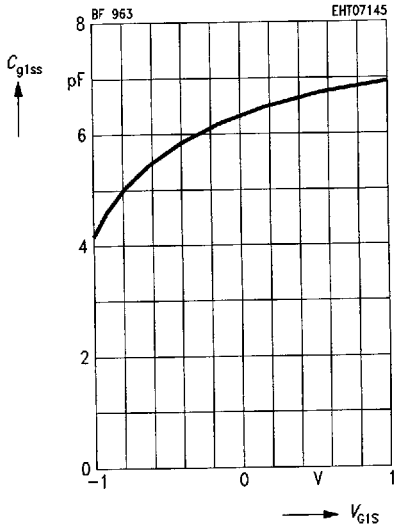
Gate 1 forward transconductance
$g_{fs1} = f(V_{G2S})$
V_{DS} = 15 V
I_{DSS} = 10 mA, f = 1 kHz



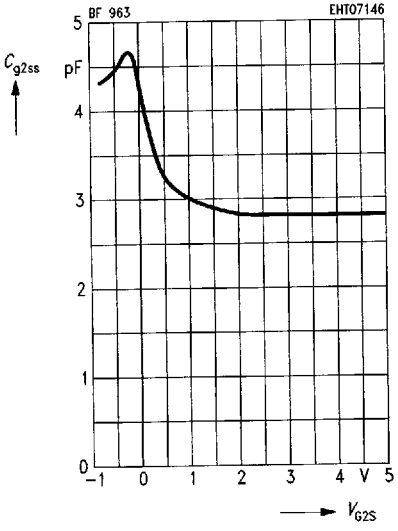
Drain current $I_D = f(V_{G1S})$
V_{DS} = 15 V



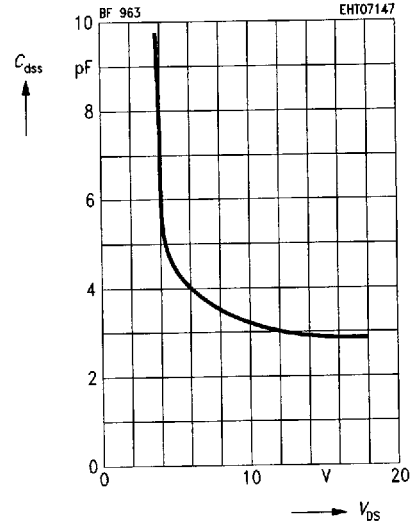
Gate 1 input capacitance $C_{g1ss} = f(V_{G1S})$
V_{G2S} = 4 V, V_{DS} = 15 V
I_{DSS} = 10 mA, f = 1 MHz



Gate 2 input capacitance $C_{g2ss} = f(V_{G2S})$
V_{G1S} = 0 V, V_{DS} = 15 V
I_{DSS} = 10 mA, f = 1 MHz



Output capacitance $C_{dss} = f(V_{DS})$
V_{G1S} = 0 V, V_{G2S} = 4 V
I_{DSS} = 10 mA, f = 1 MHz



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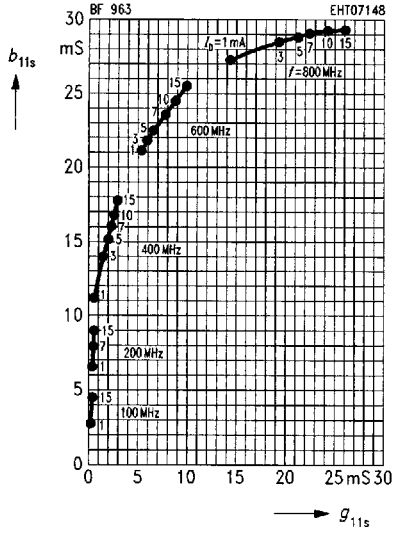
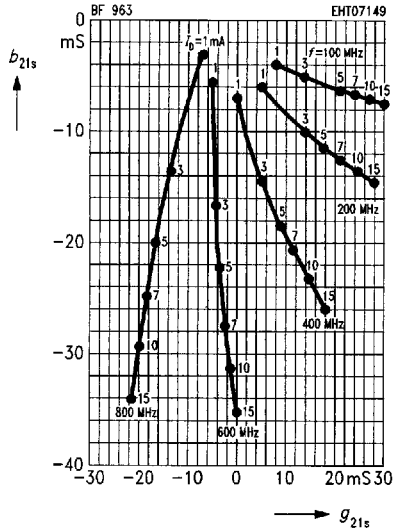
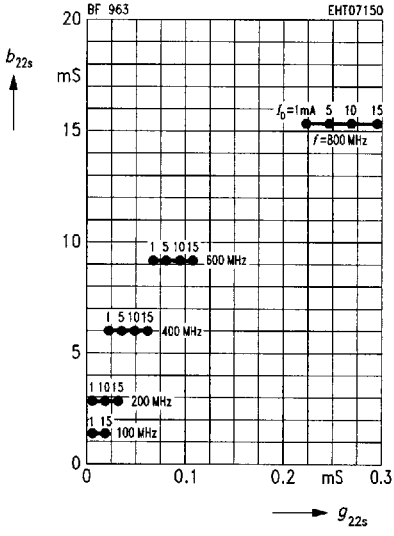
Gate 1 input admittance y_{11s}
V_{DS} = 15 V, V_{G2S} = 4 V
(common source)



Gate 1 forward transfer admittance y_{21s}
V_{DS} = 15 V, V_{G2S} = 4 V
(common source)



Output admittance y_{22s}
V_{DS} = 15 V, V_{G2S} = 4 V
(common source)



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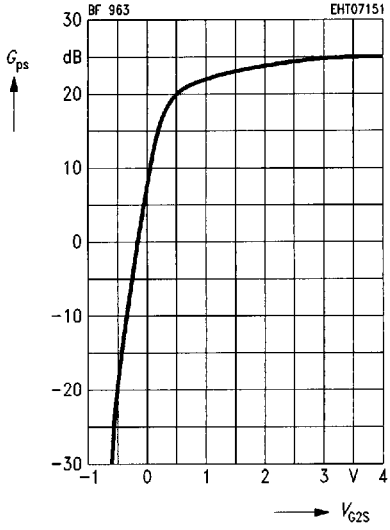
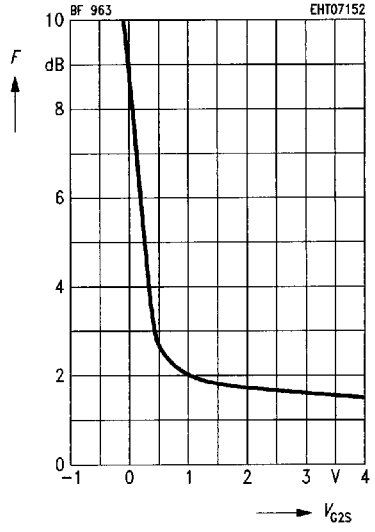
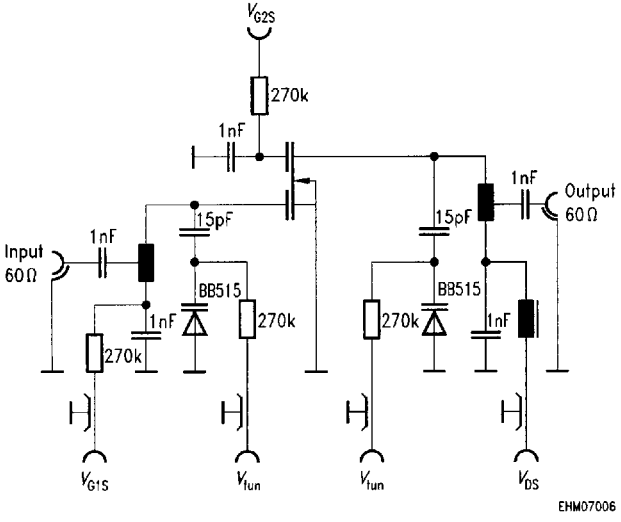
Power gain $G_{ps} = f(V_{G2S})$
V_{DS} = 15 V, V_{G1S} = 0 V, I_{DSS} = 10 mA
f = 200 MHz
(see test circuit)



Noise figure $F = f(V_{G2S})$
V_{DS} = 15 V, V_{G1S} = 0 V, I_{DSS} = 10 mA
f = 200 MHz
(see test circuit)



Test circuit for power gain and noise figure
f = 200 MHz, G_G = 2 mS, G_L = 0.5 mS



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