74AHC594; 74AHCT594

8-bit shift register with output register

Rev. 01 — 4 July 2006 Product data sheet

1. General description

The 74AHC594; 74AHCT594 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC594; 74AHCT594 is an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (SHCP and STCP) and direct overriding clears ($\overline{SHR}$ and $\overline{STR}$) are provided on both the shift and storage registers. A serial output (Q7S) is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

2. Features

- Wide supply voltage range from 2.0 V to 5.5 V
- 8-bit serial-in, parallel-out shift register with storage
- Independent direct overriding clears on shift and storage registers
- Independent clocks for shift and storage registers
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Input levels:
  - CMOS levels: 74AHC594 only
  - TTL levels: 74AHCT594 only
- ESD protection:
  - HBM JESD22-A114-C exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101-C exceeds 1000 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Serial-to parallel data conversion
- Remote control holding register

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4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC594D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC594DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74AHC594PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHC594BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AHCT594D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT594DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74AHCT594PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHCT594BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

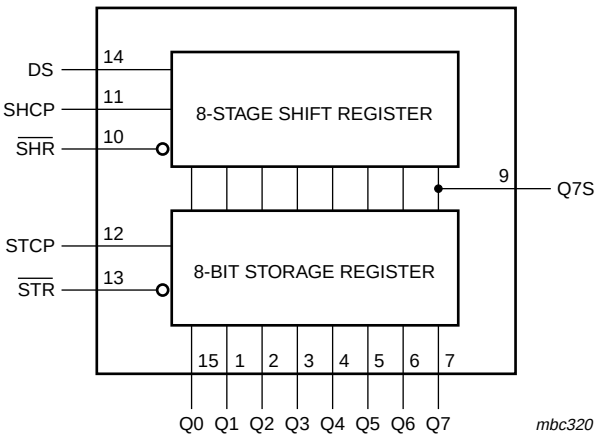


Fig 1. Functional diagram

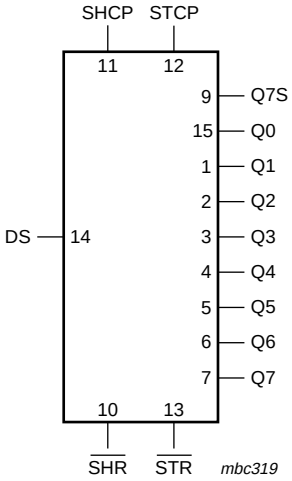


Fig 2. Logic symbol

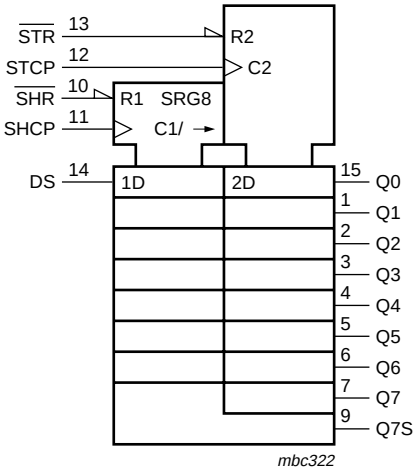


Fig 3. IEC logic symbol

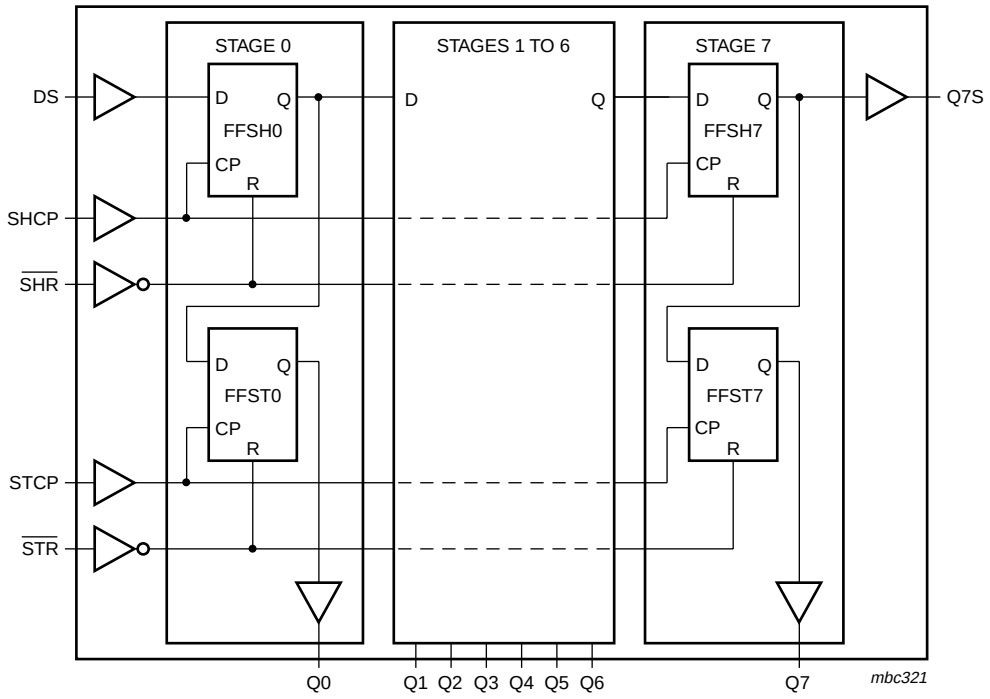


Fig 4. Logic diagram

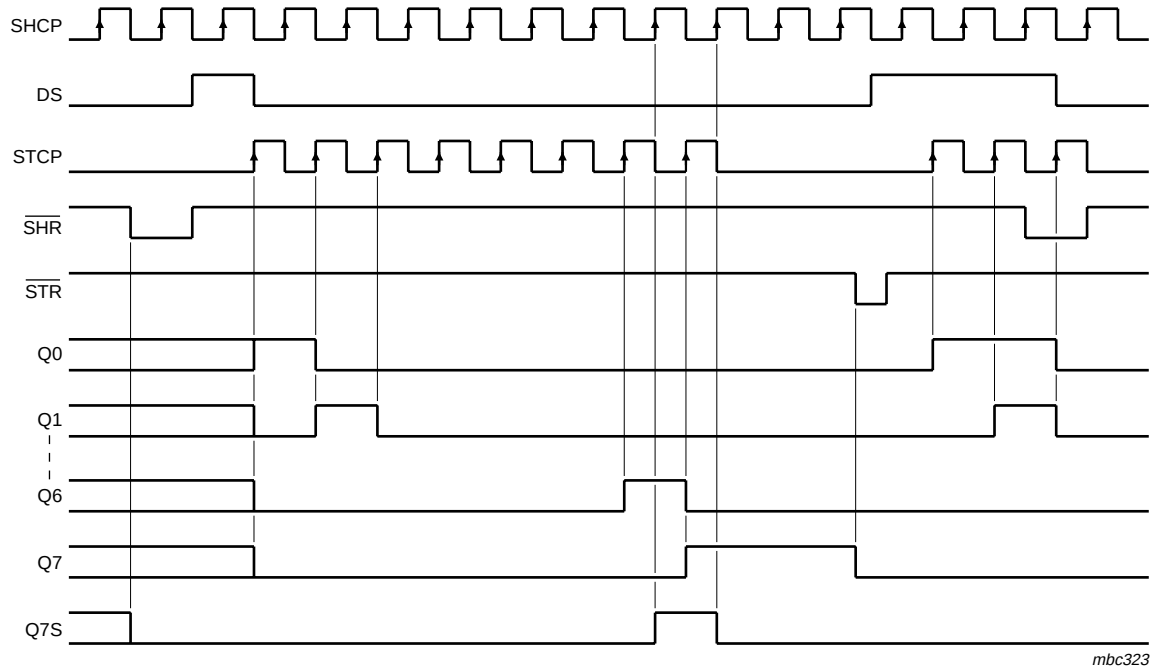


Fig 5. Timing diagram

6. Pinning information

6.1 Pinning

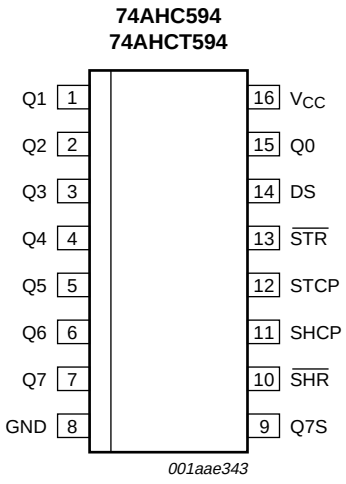


Fig 6. Pin configuration SO16

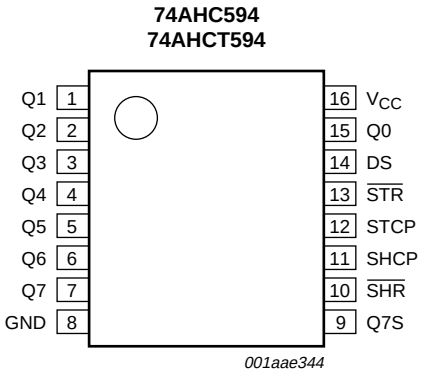
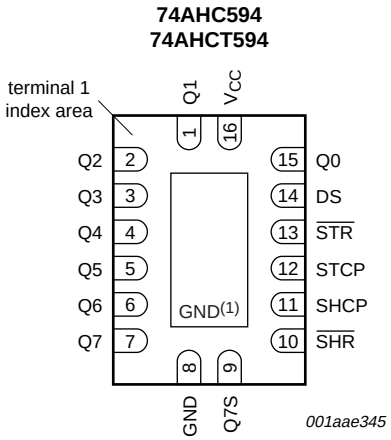


Fig 7. Pin configuration TSSOP16



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input

Fig 8. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q1	1	parallel data output Q1
Q2	2	parallel data output Q2
Q3	3	parallel data output Q3
Q4	4	parallel data output Q4
Q5	5	parallel data output Q5
Q6	6	parallel data output Q6
Q7	7	parallel data output Q7
GND	8	ground (0 V)
Q7S	9	serial data output Q7S
$\overline{SHR}$	10	shift register reset $\overline{SHR}$ (active LOW)
SHCP	11	shift register clock input SHCP
STCP	12	storage register clock input STCP
$\overline{STR}$	13	storage register reset $\overline{STR}$ (active LOW)
DS	14	serial data input DS
Q0	15	parallel data output Q0
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table[1]

Function	Inputs				
	$\overline{SHR}$	$\overline{STR}$	SHCP	STCP	DS
Clear shift register	L	X	X	X	X
Clear storage register	X	L	X	X	X
Load DS into shift register stage 0, advance previous stage data to the next stage	H	X	↑	X	H or L
Transfer shift register data to storage register and outputs Qn	X	H	X	↑	X

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH transition;
X = don't care.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	-	–20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	quiescent supply current			-	75	mA
I_{GND}	ground current			-	–75	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74AHC594						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	ns/V
		V_{CC} = 5 V ± 0.5 V	-	-	20	ns/V
Type 74AHCT594						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics type 74AHC594

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –50 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –50 µA; V_{CC} = 3.0 V	2.9	3.0	-	V
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.36	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	0.1	µA

Table 6. Static characteristics type 74AHC594 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	4.0	µA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	pF
$T_{amb} = -40$ °C to +85 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 3.0$ V	2.1	-	-	V
		$V_{CC} = 5.5$ V	3.85	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 3.0$ V	-	-	0.9	V
		$V_{CC} = 5.5$ V	-	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ µA; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -50$ µA; $V_{CC} = 3.0$ V	2.9	-	-	V
		$I_O = -50$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.48	-	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50$ µA; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 50$ µA; $V_{CC} = 3.0$ V	-	-	0.1	V
		$I_O = 50$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 3.0$ V	-	-	0.44	V
		$I_O = 8$ mA; $V_{CC} = 4.5$ V	-	-	0.44	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	40	µA
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 3.0$ V	2.1	-	-	V
		$V_{CC} = 5.5$ V	3.85	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 3.0$ V	-	-	0.9	V
		$V_{CC} = 5.5$ V	-	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ µA; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -50$ µA; $V_{CC} = 3.0$ V	2.9	-	-	V
		$I_O = -50$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.40	-	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.70	-	-	V

Table 6. Static characteristics type 74AHC594 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	2.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	µA

Table 7. Static characteristics type 74AHCT594

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.36	V
I_I	input leakage current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V	-	-	0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	mA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.44	V
I_I	input leakage current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V	-	-	1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	40	µA

Table 7. Static characteristics type 74AHCT594 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.5	mA
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.70	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 8$ mA; $V_{CC} = 4.5$ V	-	-	0.55	V
I_I	input leakage current	$V_I = V_{IH}$ or V_{IL}; $V_{CC} = 5.5$ V	-	-	2.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	80	µA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.5	mA

11. Dynamic characteristics

Table 8. Dynamic characteristics type 74AHC594

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 15.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C[1]						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 9				
		$C_L = 15$ pF	-	5.2	8.5	ns
		$C_L = 50$ pF	-	7.4	11.5	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 9				
		$C_L = 15$ pF	-	3.8	6.3	ns
		$C_L = 50$ pF	-	4.8	8.0	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	$V_{CC} = 3.0$ V to 3.6 V; see Figure 9				
		$C_L = 15$ pF	-	5.5	8.9	ns
		$C_L = 50$ pF	-	7.4	12.1	ns
		$V_{CC} = 4.5$ V to 5.5 V; see Figure 9				
		$C_L = 15$ pF	-	4.1	6.7	ns
		$C_L = 50$ pF	-	5.4	8.8	ns

Table 8. Dynamic characteristics type 74AHC594 *...continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 15.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 10				
		C_L = 15 pF	-	5.1	8.3	ns
		C_L = 50 pF	-	7.3	11.9	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 10				
		C_L = 15 pF	-	3.5	5.7	ns
		C_L = 50 pF	-	4.8	7.8	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 10				
		C_L = 15 pF	-	5.5	9.1	ns
		C_L = 50 pF	-	7.3	12.0	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 10				
		C_L = 15 pF	-	3.7	6.0	ns
		C_L = 50 pF	-	5.2	8.5	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{SHR}$ to Q7S	V_{CC} = 3.0 V to 3.6 V; see Figure 13				
		C_L = 15 pF	-	5.7	9.5	ns
		C_L = 50 pF	-	7.5	12.2	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 13				
		C_L = 15 pF	-	4.1	6.7	ns
		C_L = 50 pF	-	5.4	8.8	ns
	HIGH-to-LOW propagation delay $\overline{STR}$ to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 14				
		C_L = 15 pF	-	5.8	9.6	ns
		C_L = 50 pF	-	7.7	12.5	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 14				
		C_L = 15 pF	-	4.1	7.2	ns
		C_L = 50 pF	-	5.4	9.4	ns
t_W	pulse width HIGH or LOW SHCP and STCP	C_L = 50 pF; see Figure 9 and Figure 10				
		V_{CC} = 3.0 V to 3.6 V	6.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.5	-	-	ns
	pulse width HIGH or LOW $\overline{SHR}$ and $\overline{STR}$	C_L = 50 pF; see Figure 13 and Figure 14				
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
t_{su}	set-up time DS to SHCP	C_L = 50 pF; see Figure 11				
		V_{CC} = 3.0 V to 3.6 V	3.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.0	-	-	ns
	set-up time $\overline{SHR}$ to STCP	C_L = 50 pF; see Figure 12				
		V_{CC} = 3.0 V to 3.6 V	8.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
	set-up time SHCP to STCP	C_L = 50 pF; see Figure 10				
		V_{CC} = 3.0 V to 3.6 V	8.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns

Table 8. Dynamic characteristics type 74AHC594 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 15.

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
t_h	hold time DS to SHCP	C_L = 50 pF; see Figure 11					
		V_{CC} = 3.0 V to 3.6 V		1.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.0	-	-	ns
t_{rec}	recovery time $\overline{SHR}$ to SHCP	C_L = 50 pF; see Figure 13					
		V_{CC} = 3.0 V to 3.6 V		4.2	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.9	-	-	ns
	recovery time $\overline{STR}$ to STCP	C_L = 50 pF; see Figure 14					
		V_{CC} = 3.0 V to 3.6 V		4.6	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		3.2	-	-	ns
f_{max}	maximum frequency SHCP or STCP	C_L = 50 pF; see Figure 9 and Figure 10					
		V_{CC} = 3.0 V to 3.6 V		80	125	-	MHz
		V_{CC} = 4.5 V to 5.5 V		90	170	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; C_L = 50 pF; f_i = 1 MHz	[2]	-	55	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	V_{CC} = 3.0 V to 3.6 V; see Figure 9					
		C_L = 15 pF		2.2	-	9.7	ns
		C_L = 50 pF		3.0	-	13.2	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 9					
		C_L = 15 pF		1.7	-	7.2	ns
		C_L = 50 pF		2.4	-	9.1	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	V_{CC} = 3.0 V to 3.6 V; see Figure 9					
		C_L = 15 pF		2.3	-	10.2	ns
		C_L = 50 pF		3.0	-	13.9	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 9					
		C_L = 15 pF		1.9	-	7.6	ns
		C_L = 50 pF		2.5	-	10.1	ns
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 10					
		C_L = 15 pF		2.3	-	9.5	ns
		C_L = 50 pF		3.3	-	13.6	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 10					
		C_L = 15 pF		1.8	-	6.5	ns
		C_L = 50 pF		2.6	-	9.0	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 10					
		C_L = 15 pF		2.4	-	10.4	ns
		C_L = 50 pF		3.2	-	13.8	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 10					
		C_L = 15 pF		1.9	-	6.9	ns
		C_L = 50 pF		2.6	-	9.7	ns

Table 8. Dynamic characteristics type 74AHC594 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 15.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay $\overline{SHR}$ to Q7S	V_{CC} = 3.0 V to 3.6 V; see Figure 13				
		C_L = 15 pF	2.3	-	10.8	ns
		C_L = 50 pF	3.6	-	14.0	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 13				
		C_L = 15 pF	2.0	-	7.6	ns
		C_L = 50 pF	2.8	-	10.1	ns
	HIGH-to-LOW propagation delay $\overline{STR}$ to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 14				
		C_L = 15 pF	2.8	-	11.0	ns
		C_L = 50 pF	3.8	-	14.4	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 14				
		C_L = 15 pF	2.2	-	8.2	ns
		C_L = 50 pF	3.0	-	10.7	ns
t_W	pulse width HIGH or LOW SHCP and STCP	C_L = 50 pF; see Figure 9 and Figure 10				
		V_{CC} = 3.0 V to 3.6 V	6.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	6.0	-	-	ns
	pulse width HIGH or LOW $\overline{SHR}$ and $\overline{STR}$	C_L = 50 pF; see Figure 13 and Figure 14				
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.2	-	-	ns
t_{su}	set-up time DS to SHCP	C_L = 50 pF; see Figure 11				
		V_{CC} = 3.0 V to 3.6 V	3.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.0	-	-	ns
	set-up time $\overline{SHR}$ to STCP	C_L = 50 pF; see Figure 12				
		V_{CC} = 3.0 V to 3.6 V	9.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
	set-up time SHCP to STCP	C_L = 50 pF; see Figure 10				
		V_{CC} = 3.0 V to 3.6 V	8.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
t_h	hold time DS to SHCP	C_L = 50 pF; see Figure 11				
		V_{CC} = 3.0 V to 3.6 V	1.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.0	-	-	ns
t_{rec}	recovery time $\overline{SHR}$ to SHCP	C_L = 50 pF; see Figure 13				
		V_{CC} = 3.0 V to 3.6 V	4.8	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.3	-	-	ns
	recovery time $\overline{STR}$ to STCP	C_L = 50 pF; see Figure 14				
		V_{CC} = 3.0 V to 3.6 V	5.3	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.7	-	-	ns

Table 8. Dynamic characteristics type 74AHC594 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 15.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{max}	maximum frequency SHCP or STCP	C_L = 50 pF; see Figure 9 and Figure 10				
		V_{CC} = 3.0 V to 3.6 V	70	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V	80	-	-	MHz
T_{amb} = −40 °C to +125 °C						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	V_{CC} = 3.0 V to 3.6 V; see Figure 9				
		C_L = 15 pF	2.2	-	10.6	ns
		C_L = 50 pF	3.0	-	14.3	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 9				
		C_L = 15 pF	1.7	-	7.8	ns
		C_L = 50 pF	2.4	-	10.0	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	V_{CC} = 3.0 V to 3.6 V; see Figure 9				
		C_L = 15 pF	2.3	-	11.0	ns
		C_L = 50 pF	3.0	-	15.1	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 9				
		C_L = 15 pF	1.9	-	8.2	ns
		C_L = 50 pF	2.5	-	11.0	ns
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 10				
		C_L = 15 pF	2.3	-	10.6	ns
		C_L = 50 pF	3.3	-	14.7	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 10				
		C_L = 15 pF	1.8	-	7.1	ns
		C_L = 50 pF	2.6	-	9.8	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 10				
		C_L = 15 pF	2.4	-	11.3	ns
		C_L = 50 pF	3.2	-	15.0	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 10				
		C_L = 15 pF	1.9	-	7.5	ns
		C_L = 50 pF	2.6	-	10.5	ns

Table 8. Dynamic characteristics type 74AHC594 *...continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 15.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{PHL}	HIGH-to-LOW propagation delay $\overline{SHR}$ to Q7S	V_{CC} = 3.0 V to 3.6 V; see Figure 13				
		C_L = 15 pF	2.3	-	11.7	ns
		C_L = 50 pF	3.6	-	15.2	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 13				
		C_L = 15 pF	2.0	-	8.2	ns
		C_L = 50 pF	2.8	-	11.0	ns
	HIGH-to-LOW propagation delay $\overline{STR}$ to Qn	V_{CC} = 3.0 V to 3.6 V; see Figure 14				
		C_L = 15 pF	2.8	-	12.0	ns
		C_L = 50 pF	3.8	-	15.6	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 14				
		C_L = 15 pF	2.2	-	8.9	ns
		C_L = 50 pF	3.0	-	11.6	ns
t_W	pulse width HIGH or LOW SHCP and STCP	C_L = 50 pF; see Figure 9 and Figure 10				
		V_{CC} = 3.0 V to 3.6 V	7.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	6.5	-	-	ns
	pulse width HIGH or LOW $\overline{SHR}$ and $\overline{STR}$	C_L = 50 pF; see Figure 13 and Figure 14				
		V_{CC} = 3.0 V to 3.6 V	5.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.7	-	-	ns
t_{su}	set-up time DS to SHCP	C_L = 50 pF; see Figure 11				
		V_{CC} = 3.0 V to 3.6 V	4.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.5	-	-	ns
	set-up time $\overline{SHR}$ to STCP	C_L = 50 pF; see Figure 12				
		V_{CC} = 3.0 V to 3.6 V	9.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.5	-	-	ns
	set-up time SHCP to STCP	C_L = 50 pF; see Figure 10				
		V_{CC} = 3.0 V to 3.6 V	9.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.5	-	-	ns
t_h	hold time DS to SHCP	C_L = 50 pF; see Figure 11				
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	2.5	-	-	ns
t_{rec}	recovery time $\overline{SHR}$ to SHCP	C_L = 50 pF; see Figure 13				
		V_{CC} = 3.0 V to 3.6 V	5.3	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.8	-	-	ns
	recovery time $\overline{STR}$ to STCP	C_L = 50 pF; see Figure 14				
		V_{CC} = 3.0 V to 3.6 V	5.8	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	4.3	-	-	ns

Table 8. Dynamic characteristics type 74AHC594 *...continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 15.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{max}	maximum frequency SHCP or STCP	C_L = 50 pF; see Figure 9 and Figure 10				
		V_{CC} = 3.0 V to 3.6 V	65	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V	70	-	-	MHz

[1] Typical values are measured at nominal V_{CC}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 9. Dynamic characteristics type 74AHCT594

GND = 0 V; $t_r = t_f \leq 3.0$ ns; V_{CC} = 4.5 V to 5.5 V; see Figure 15

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C[1]						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	see Figure 9				
		C_L = 15 pF	-	3.8	6.3	ns
		C_L = 50 pF	-	4.8	8.0	ns
t_{PHL}	HIGH-to-LOW and LOW-to-HIGH propagation delay SHCP to Q7S	see Figure 9				
		C_L = 15 pF	-	4.1	6.7	ns
		C_L = 50 pF	-	5.4	8.8	ns
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	see Figure 10				
		C_L = 15 pF	-	3.5	5.7	ns
		C_L = 50 pF	-	4.6	7.7	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	see Figure 10				
		C_L = 15 pF	-	3.7	6.1	ns
		C_L = 50 pF	-	5.2	8.5	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{SHR}$ to Q7S	see Figure 13				
		C_L = 15 pF	-	4.3	7.0	ns
		C_L = 50 pF	-	5.4	8.8	ns
	HIGH-to-LOW propagation delay $\overline{STR}$ to Qn	see Figure 14				
		C_L = 15 pF	-	4.5	7.4	ns
		C_L = 50 pF	-	5.7	9.4	ns
t_W	pulse width HIGH or LOW SHCP and STCP	C_L = 50 pF; see Figure 9 and Figure 10	5.5	-	-	ns
	pulse width HIGH or LOW $\overline{SHR}$ and $\overline{STR}$	C_L = 50 pF; see Figure 13 and Figure 14	5.2	-	-	ns

Table 9. Dynamic characteristics type 74AHCT594 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; V_{CC} = 4.5 V to 5.5 V; see Figure 15

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
t_{su}	set-up time DS to SHCP	C_L = 50 pF; see Figure 11		3.0	-	-	ns
	set-up time $\overline{SHR}$ to STCP	C_L = 50 pF; see Figure 12		5.0	-	-	ns
	set-up time SHCP to STCP	C_L = 50 pF; see Figure 10		5.0	-	-	ns
t_h	hold time DS to SHCP	see Figure 11		2.0	-	-	ns
t_{rec}	recovery time $\overline{SHR}$ to SHCP	C_L = 50 pF; see Figure 13		2.9	-	-	ns
	recovery time $\overline{STR}$ to STCP	C_L = 50 pF; see Figure 14		3.4	-	-	ns
f_{max}	maximum frequency SHCP or STCP	C_L = 50 pF; see Figure 9 and Figure 10		90	160	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; C_L = 50 pF; f_i = 1 MHz	[2]	-	55	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	see Figure 9					
		C_L = 15 pF		1.7	-	7.2	ns
		C_L = 50 pF		2.2	-	9.1	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	see Figure 9					
		C_L = 15 pF		1.8	-	7.6	ns
		C_L = 50 pF		2.4	-	10.1	ns
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	see Figure 10					
		C_L = 15 pF		1.8	-	6.5	ns
		C_L = 50 pF		2.6	-	8.8	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	see Figure 10					
		C_L = 15 pF		1.9	-	6.9	ns
		C_L = 50 pF		2.6	-	9.7	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{SHR}$ to Q7S	see Figure 13					
		C_L = 15 pF		2.4	-	8.0	ns
		C_L = 50 pF		2.7	-	10.1	ns
	HIGH-to-LOW propagation delay $\overline{STR}$ to Qn	see Figure 14					
		C_L = 15 pF		2.3	-	8.4	ns
		C_L = 50 pF		3.1	-	10.7	ns
t_W	pulse width HIGH or LOW SHCP and STCP	C_L = 50 pF; see Figure 9 and Figure 10		6.0	-	-	ns
	pulse width HIGH or LOW $\overline{SHR}$ and $\overline{STR}$	C_L = 50 pF; see Figure 13 and Figure 14		5.5	-	-	ns

Table 9. Dynamic characteristics type 74AHCT594 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; $V_{CC} = 4.5$ V to 5.5 V; see Figure 15

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{su}	set-up time DS to SHCP	C_L = 50 pF; see Figure 11	3.0	-	-	ns
	set-up time $\overline{SHR}$ to STCP	C_L = 50 pF; see Figure 12	5.0	-	-	ns
	set-up time SHCP to STCP	C_L = 50 pF; see Figure 10	5.0	-	-	ns
t_h	hold time DS to SHCP	see Figure 11	2.0	-	-	ns
t_{rec}	recovery time $\overline{SHR}$ to SHCP	C_L = 50 pF; see Figure 13	3.3	-	-	ns
	recovery time $\overline{STR}$ to STCP	C_L = 50 pF; see Figure 14	3.8	-	-	ns
f_{max}	maximum frequency SHCP or STCP	C_L = 50 pF; see Figure 9 and Figure 10	80	-	-	MHz
T_{amb} = −40 °C to +125 °C						
t_{PLH}	LOW-to-HIGH propagation delay SHCP to Q7S	see Figure 9				
		C_L = 15 pF	1.7	-	7.8	ns
		C_L = 50 pF	2.2	-	9.9	ns
t_{PHL}	HIGH-to-LOW propagation delay SHCP to Q7S	see Figure 9				
		C_L = 15 pF	1.8	-	8.3	ns
		C_L = 50 pF	2.4	-	11.0	ns
t_{PLH}	LOW-to-HIGH propagation delay STCP to Qn	see Figure 10				
		C_L = 15 pF	1.8	-	7.1	ns
		C_L = 50 pF	2.6	-	9.6	ns
t_{PHL}	HIGH-to-LOW propagation delay STCP to Qn	see Figure 10				
		C_L = 15 pF	1.9	-	7.2	ns
		C_L = 50 pF	2.6	-	10.5	ns
t_{PHL}	HIGH-to-LOW propagation delay $\overline{SHR}$ to Q7S	see Figure 13				
		C_L = 15 pF	2.4	-	8.7	ns
		C_L = 50 pF	2.7	-	11.0	ns
	HIGH-to-LOW propagation delay $\overline{STR}$ to Qn	see Figure 14				
		C_L = 15 pF	2.3	-	9.2	ns
		C_L = 50 pF	3.1	-	11.7	ns
t_W	pulse width HIGH or LOW SHCP and STCP	C_L = 50 pF; see Figure 9 and Figure 10	6.5	-	-	ns
	pulse width HIGH or LOW $\overline{SHR}$ and $\overline{STR}$	C_L = 50 pF; see Figure 13 and Figure 14	6.0	-	-	ns
t_{su}	set-up time DS to SHCP	C_L = 50 pF; see Figure 11	3.5	-	-	ns
	set-up time $\overline{SHR}$ to STCP	C_L = 50 pF; see Figure 12	5.5	-	-	ns
	set-up time SHCP to STCP	C_L = 50 pF; see Figure 10	5.5	-	-	ns
t_h	hold time DS to SHCP	see Figure 11	2.5	-	-	ns

Table 9. Dynamic characteristics type 74AHCT594 *…continued*

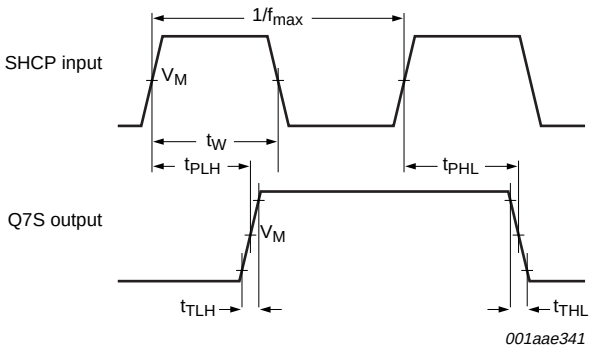
GND = 0 V; $t_r = t_f \leq 3.0$ ns; V_{CC} = 4.5 V to 5.5 V; see Figure 15

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{rec}	recovery time $\overline{SHR}$ to SHCP	C_L = 50 pF; see Figure 13	3.8	-	-	ns
	recovery time $\overline{STR}$ to STCP	C_L = 50 pF; see Figure 14	4.3	-	-	ns
f_{max}	maximum frequency SHCP or STCP	C_L = 50 pF; see Figure 9 and Figure 10	70	-	-	MHz

[1] Typical values are measured at V_{CC} = 5.0 V.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

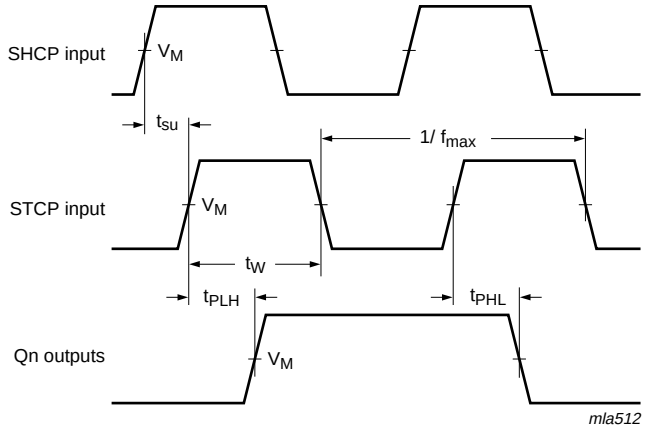
12. Waveforms



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

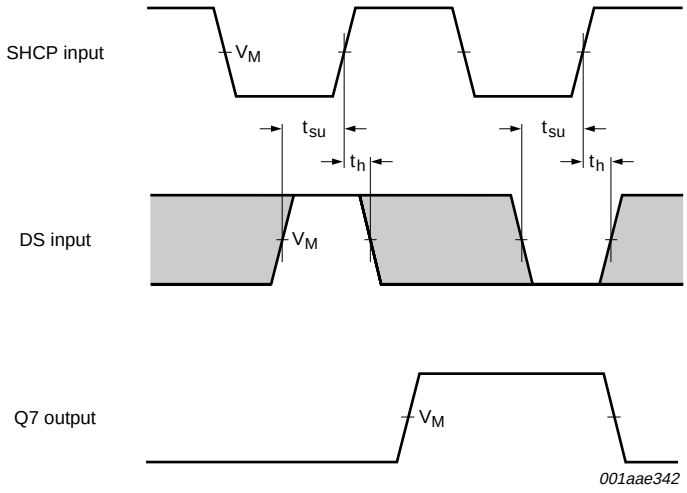
Fig 9. The shift clock (SHCP) to output (Q7S) propagation delays, the shift clock pulse width, and the maximum shift clock frequency



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 10. The storage clock (STCP) to output (Qn), propagation delays, the storage clock pulse width, the maximum storage clock pulse frequency and the shift clock to storage clock set-up time

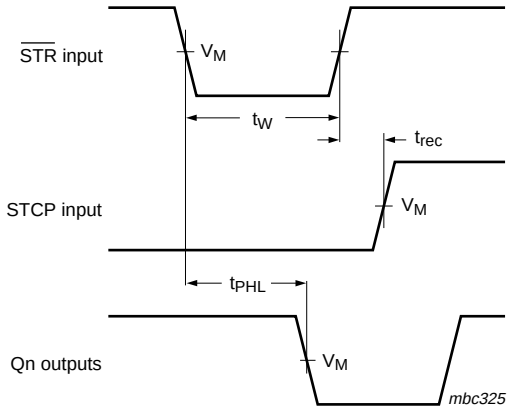


Measurement points are given in Table 10.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

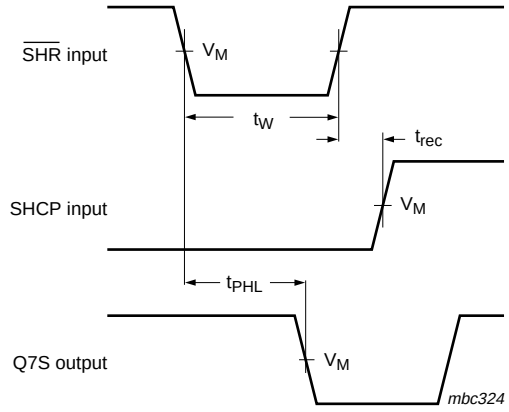
Fig 11. The data set-up time and hold times for DS input to SHCP



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

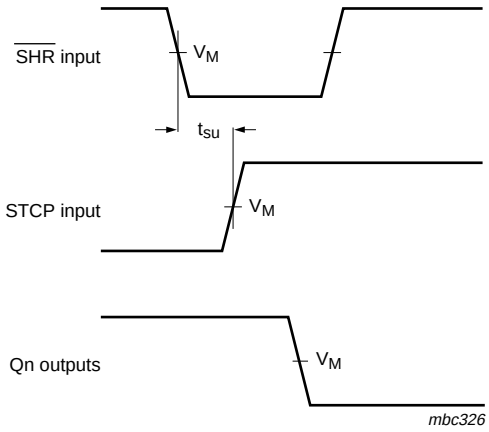
Fig 12. The set-up time shift reset ($\overline{SHR}$) to storage clock (STCP)



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 13. The shift reset ($\overline{SHR}$) pulse width, the shift reset to output (Q7S) propagation delay and the shift reset to shift clock (SHCP) recovery time



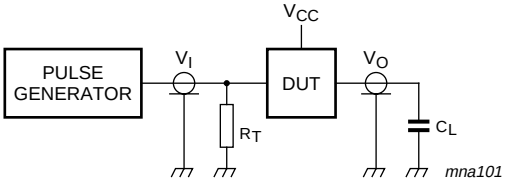
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 14. The storage reset ($\overline{STR}$) pulse width, the storage reset to output (Qn) propagation delay and the storage reset to storage clock (STCP) recovery time

Table 10. Measurement points

Type	Input	Output
	V_M	V_M
74AHC594	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT594	1.5 V	$0.5 \times V_{CC}$



For test data see Table 11.

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

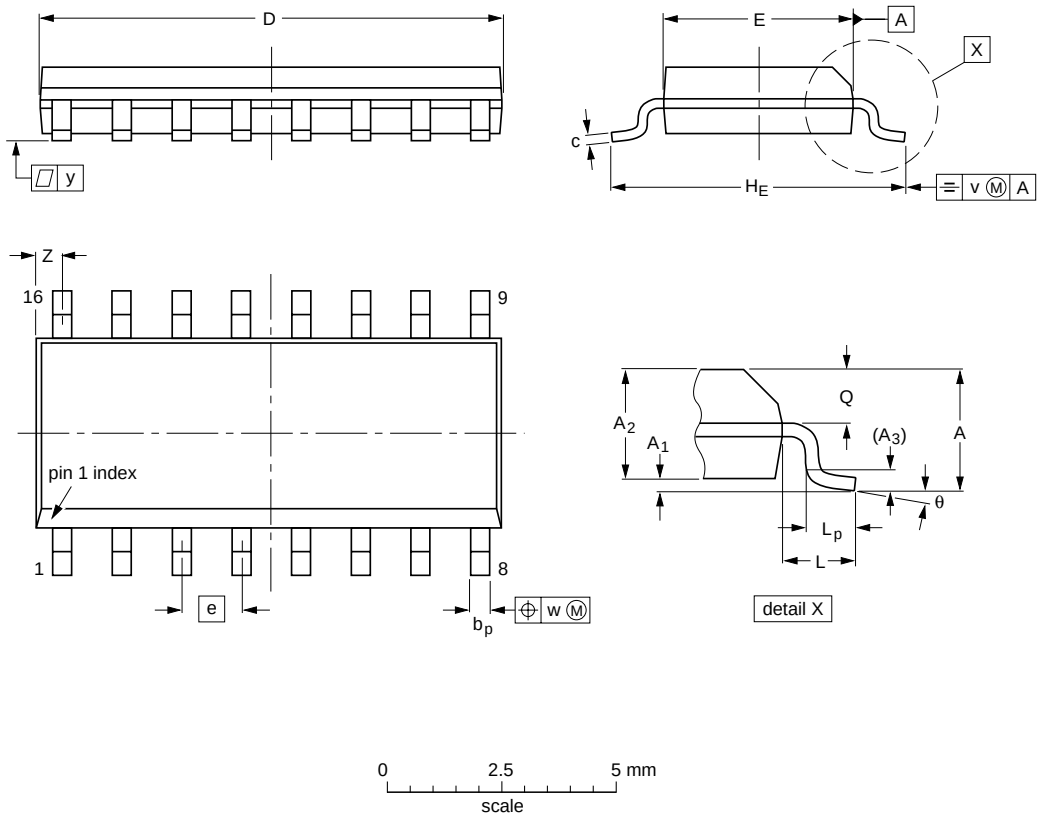
Fig 15. Load circuitry for switching times

Table 11. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC594	V_{CC}	≤ 3.0 ns	50 pF, 15 pF	t_{PLH}, t_{PHL}
74AHCT594	3.0 V	≤ 3.0 ns	50 pF, 15 pF	t_{PLH}, t_{PHL}

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

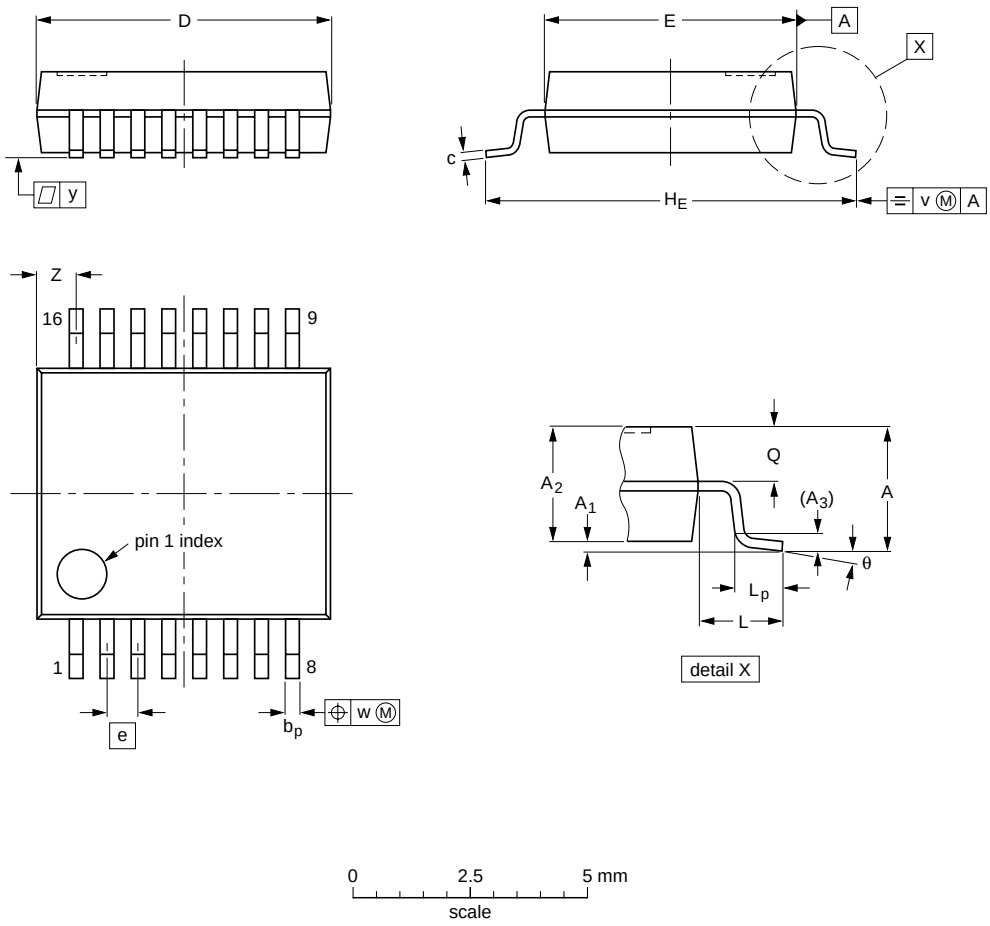
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

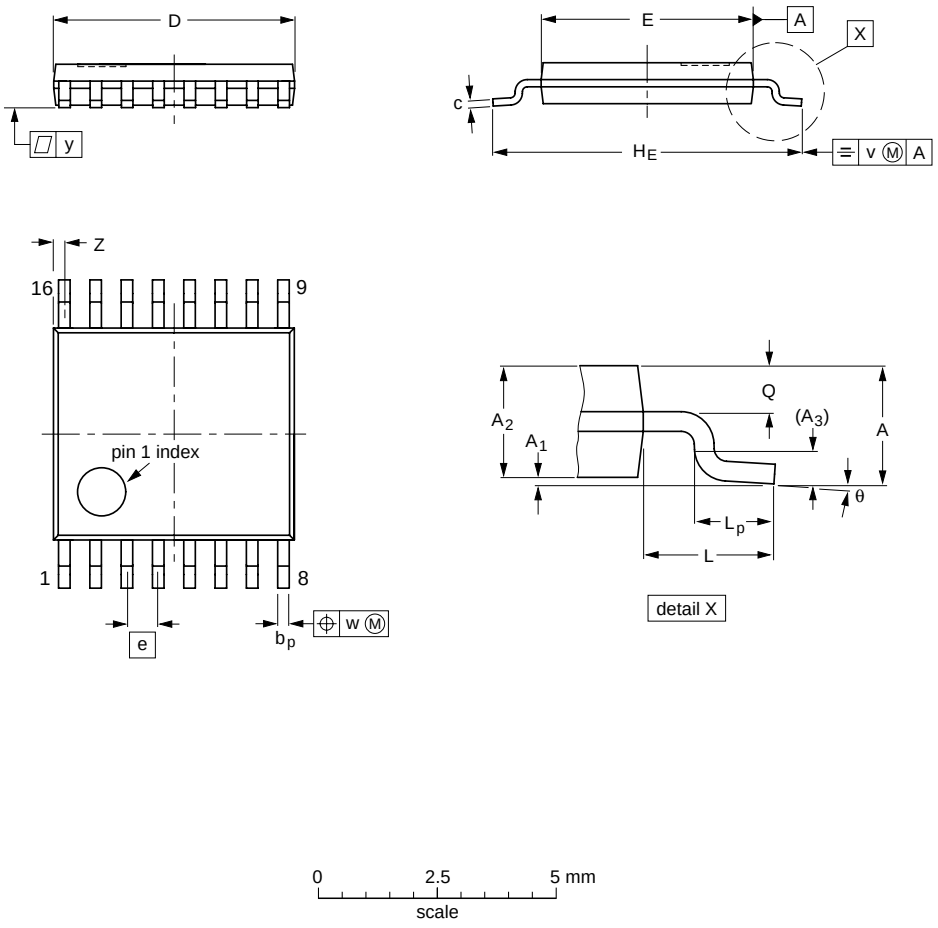
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

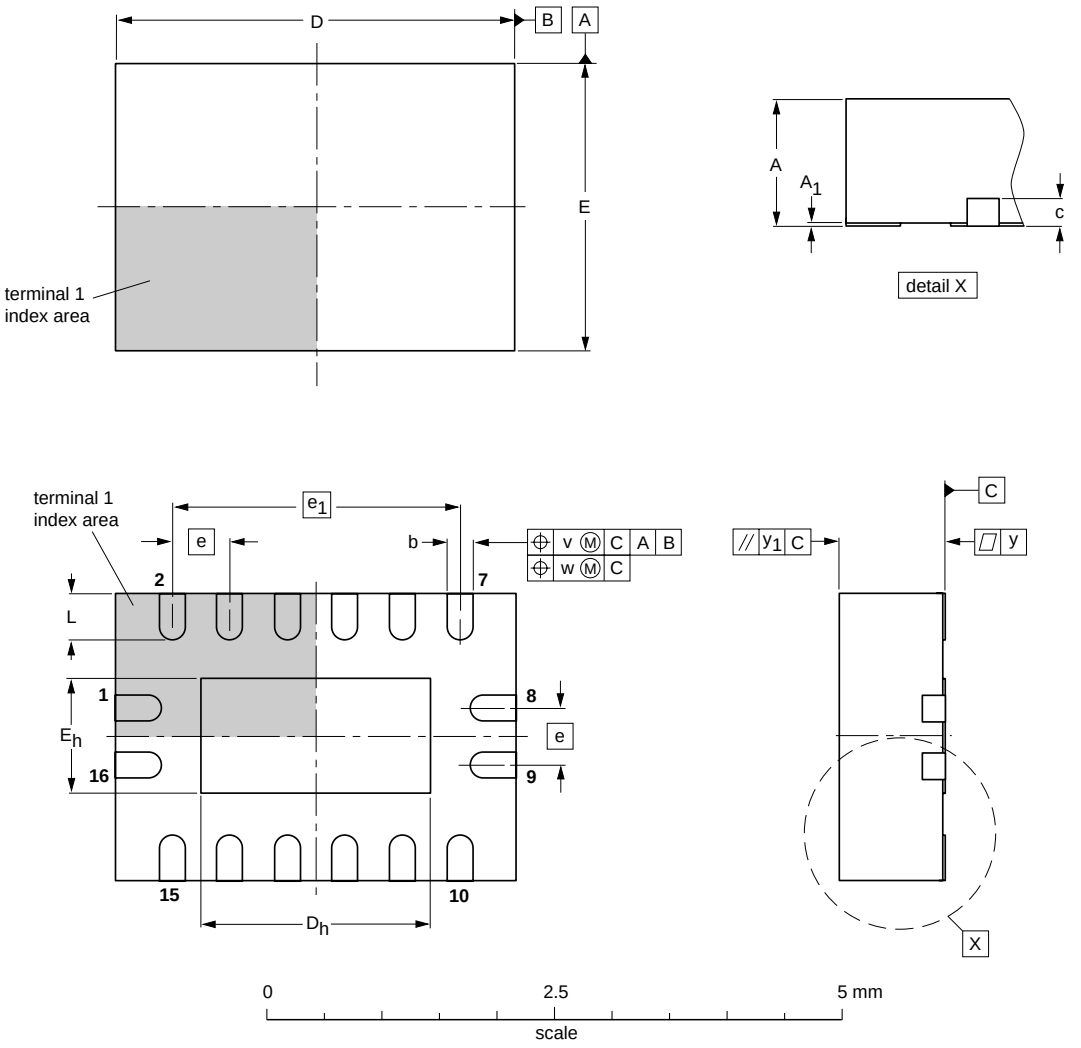
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 18. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 19. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT594_1	20060704	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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