



LI-ION PROTECTION IC WITH POWER MOS

Preliminary

EC9525

Features

Low supply current	Supply current	TYP. 3.0uA
	Standby current (after detecting over-discharge)	TYP. 0.25uA
High accuracy detector	Over-charge detector($T_{opt}=25^{\circ}\text{C}$)	+/- 25mV
Threshold	Over-charge detector ($T_{opt}=0$ to 50°C)	+/- 30mV
	Over-discharge detector	+/- 3.0%
Variety of detector threshold	Over-charge detector threshold	4.0V to 4.4V step of 0.005V
	Over-discharge detector threshold	2.0V to 3.0V step of 0.005V
Built in protection circuit	Excess current protection	0.04V to 0.32V step of 0.04V
	Accuracy	$\pm 20\%$
Output delay of over charge	Time delay at $V_{DD}=4.3\text{V}$	1.0S
Output delay of over-discharg	$V_{DD}=2.4\text{V}$ with built-in capacitor	10mS
Package		SOP-8/8-pin



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General Description

The EC9525 is protection IC with Power MOS for over-charge/discharge of rechargeable one-cell Lithium-ion(Li+) excess load current, further include a short circuit protector for preventing large external short circuit current.

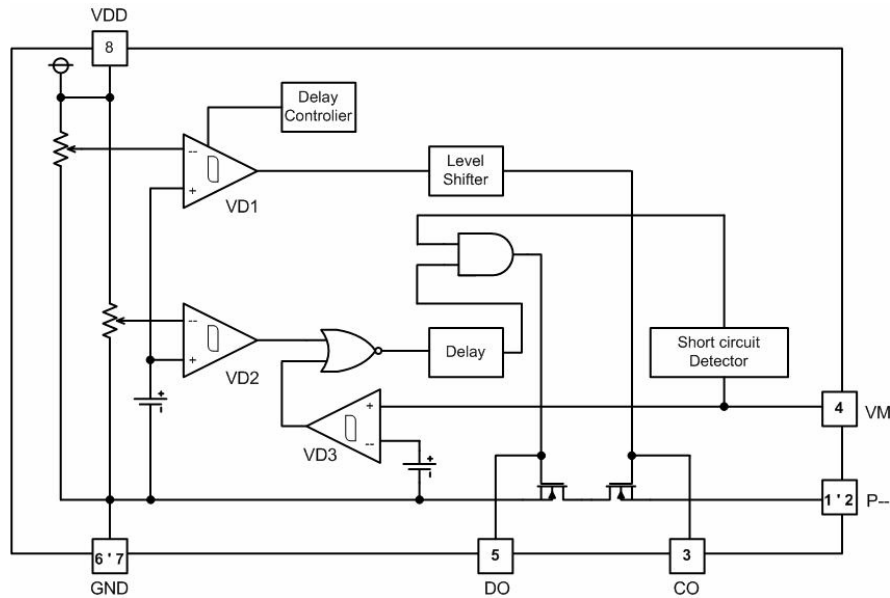
Each of these IC is composed of three voltage detectors, a reference unit, a delay circuit, a short circuit protector, a logic circuit and two N-type Power MOS. When charging voltage crosses the detector threshold from a low value to value higher than VDET1, the output of Cout pin, the output of over-charge detector/VD1, switches to low level, charger's negative pin level. After detecting over-charge the VD1 can be reset and the output of Cout becomes high when the VDD voltage is coming down to a level lower than "VREL1", or when a kind of loading is connected to VDD after a charger is disconnected from the battery pack while the VDD level is in between "VDET1" and "VREL1" in the EC9525.

The output of Dout pin, the output of over-discharge detector/VD2, switches to low level after internally fixed delay time passed, when discharging voltage crosses the detector threshold from a high value lower than VDET2. After EC9525 detect the over-discharge voltage, connect a charger to the battery pack, and when the battery supply voltage becomes higher than the over-discharge detector threshold, VD2 is released and the voltage of Dout becomes "H" level.

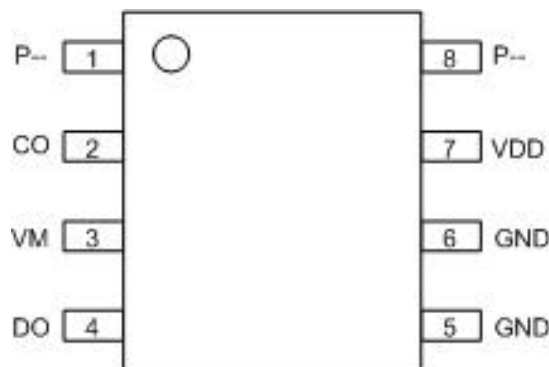
An excess load current can be sensed and cut off after internally fixed delay time passed through the built in excess current detector, VD3 with Dout being enabled to low level. Once after detecting excess current, the VD3 is released and Dout level switches to high by detaching a battery pack from a load system.

Further, short circuit protector makes Dout level to low immediately with external short circuit current and re-moving external short circuit leads Dout level to high. After detecting over-discharge, supply current will be kept extremely low by halt some internal circuits operation. The output delay of over-charge detectors can be set by connecting internal capacitors. Output type of Cout and Dout are observed. 8-pin package, SOP-8 is available.

Block Diagram



Pin Configurations



PIN DESCRIPTION

Pin No.	Symbol	Pin description
1	P-	Pin for charge negative input
2	Cout	Output of over-charge detection, CMOS output
3	VM	Internal pin for charge negative input
4	DO	Output of over-discharge detection, CMOS output
5	VSS	Ground
6	VSS	Ground
7	VDD	Power supply
8	P-	Pin for charge negative input



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ABSOLUTE MAXIMUM RATINGS

			V _{SS} =0V
Symbol	Item	Ratings	Unit
VDD	Supply voltage	-0.3 to 12	V
V- VcI-	Input voltage		
	V- pin	V _{DD} -20 to V _{DD} +0.3	V
	VI-pin	V _{DD} -20 to V _{DD} +0.3	V
Vcout Vdout	Output voltage		
	Cout pin	V _{DD} -20 to V _{DD} +0.3	V
	Dout pin	V _{SS} -0.3 to V _{DD} +0.3	V
P _D	Power dissipation	150	mW
T _{opt}	Operating temperature range	-40 to 85	°C
T _{stg}	Storage temperature range	-55 to 125	°C

Absolute Maximum ratings are threshold limit values that must not be exceeded ever for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.



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ELECTRICAL CHARACTERISTIC

Temp=25°C

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit		
VDD1	Operating input voltage	Voltage defined as VDD-Vss	1.5		10	V		
VDET1	Over-charge threshold	Detect rising edge of supply voltage	003	25°C	4.250	4.275	4.300	V
				0~50°C *Note	4.240	4.275	4.310	V
VREL1	Release voltage for over-charge detection	--	003	4.050	4.075	4.10	V	
tVDET1	Output delay of over charge	VDD=3.6V to 4.3V	0.6	1.0	1.4	S		
VDET2	Over-discharge threshold	Detect falling edge of supply voltage	003	2.425	2.500	2.575	V	
tVDET2	Output delay of over-discharge	VDD=3.6V to 2.4V	7	10	13	ms		
VDET3	Excess current threshold	Detect rising edge of "V-" pin voltage	003	0.1	0.12	0.14	V	
tVDET3	Output delay of excess current	VDD=3.0V	11	16	21	ms		
Vshort	Short protection voltage	VDD=3.0V	VDD-1.2	VDD-0.9	VDD-0.6	V		
tshort	Output delay of short protection	VDD=3.0V		300	400	us		
Rshort	Reset resistance for excess current protection	VDD=3.6V, V-=1.0V	50	100	150	kOhm		
IGSS	Gate leakage current	V _{GS} = ±10 V, V _{DS} = 0 V			±10	uA		
IDSS	Drain cut.off current	V _{DS} = 20 V, V _{GS} = 0 V			10	uA		
V (BR) DSS	Drain.source breakdown voltage	I _D = 10 mA, V _{GS} = 0 V	20			V		
V (BR) DSX		I _D = 10 mA, V _{GS} = -12 V	15			V		
Vth	Gate threshold voltage	V _{DS} = 10 V, I _D = 200 μA	0.5		1.2	V		
R _{DS (ON)}	Drain-source ON resistance	V _{GS} = 2.5 V, I _D = 3A		28		mΩ		
R _{DS (ON)}		V _{GS} = 4 V, I _D = 3 A		40		mΩ		
Vol1	Nch ON voltage of Cout	I _{ol} =50uA, VDD=4.4V		0.35	0.5	V		
Voh1	Pch ON voltage of Cout	I _{ol} =-50uA, VDD=3.9V	3.4	3.7		V		
Vol2	Nch ON voltage of Dout	I _{ol} =50uA, VDD=2.4V		0.2	0.5	V		
Voh2	Pch ON voltage of Dout	I _{ol} =-50uA, VDD=3.9V	3.4	3.7		V		
IDD	Supply current	VDD=3.9V, V-=0V		3.0	5.0	uA		
Istandby	Standby current	VDD=2.0V		0.25	0.4	uA		



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*Note: Considering of variation in process parameters, we compensate for this characteristic related to temperature by laser-trim, however, this specification is guaranteed by design, not production tested.

OPERATION

VD1/Over-Charge Detector

The VD1 monitors VDD pin voltage. When the VDD voltage crosses over charge detector threshold VDET1 from a low value to a value higher than the VDET1, the VD1 can sense a over-charging and an external charge control Nch-MOS-FET turns to “OFF” with Cout pin being at “L” level.

There can be two cases to reset the VD1 making the Cout pin level to “H” again after detecting over-charge. Resetting the VD1 can make charging system allowable to resumption of charging process. The first case is in such conditions that a time when the VDD voltage is coming down to a level lower than “VREL1”. While in the second case, connecting a kind of loading to VDD after disconnecting a charger from the battery pack can make the VD1 resetting when the VDD level is in between “VDET1” and “VREL1”.

After detecting over-charge with the VDD voltage of higher than VDET1, connecting system load to the battery pack makes load current allowable through parasitic diode of external charge control FET. The Cout level would be high when the VDD level is coming down to a level below the VDET1 by continuous drawing of load current.

An output delay time for over-charge detection can be set by external capacitor C3 connecting between the Vss pin and Ct pin. The external capacitor can make a delay time from a moment detecting over-charge to a time output a signal which enables charge control FET turn off.

When the VDD level is going up to a higher level than VDET1 if the VDD voltage would be back to a level lower than the VDET1 within a time period of the output delay time, VD1 would not output a signal for turning off the charge control FET.

A level shifter incorporated in a buffer driver for the Cout pin makes the “L” level of Cout pin to the V- pin voltage and the “H” level of Cout pin is set to VDD voltage with CMOS buffer

VD2/Over-Discharge Detector

The VD2 is monitoring a VDD pin voltage. When the VDD voltage crosses the over-discharge detector threshold VDET2 from a high value to a value lower than the VDET2, the VD2 can sense an over-discharging and the external discharge control Nch MOSFET turns to “OFF” with the Dout pin being at “L” level.

To reset the VD2 with the Dout pin level being “H” again after detecting over-discharge it is necessary to connect a charger to the battery pack for EC9525. When the VDD voltage stays under over-discharge detector threshold VDET2 charge current can flow through parasitic diode of external discharge control MOSFET, then after the VDD voltage comes up to a value larger than VDET2, Dout becomes “H” and discharging process would be able to advance through ON state MOSFET for discharge control.

Connecting a charger to the battery pack makes the Dout level being “H” instantaneously when the VDD voltage is higher than VDET2.



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Besides, for EC9525, when a cell voltage reaches equal or more than over-discharge released voltage, or VDET2, over-discharge condition can be also released.

An output delay time for the over-discharge detection is fixed internally, $t_{VDET2} = 10\text{ms}$ typ. At $V_{DD} = 2.4\text{V}$. When the V_{DD} level is going down to a lower level than VDET2 if the V_{DD} voltage would be back to a level higher than the VDET2 within a time period of the output delay time, VD2 would not output a signal for turning off the discharge control FET.

After detection of an over-discharge by VD2, supply current would be reduced to typ. $0.3\mu\text{A}$ at $V_{DD} = 2.0\text{V}$ and into standby, only the charger detector is operating.

The output type of Dout pin is CMOS having “H” level of V_{DD} and “L” level of V_{SS} .

VD3/Excess Current Detector, Short Circuit Protector

Both of the excess current detector and short circuit protector can work when both control FETs are in “ON” state. When the V- pin voltage is going up to a value between the short protection voltage V_{short}/V_{DD} and excess current threshold VDET3, the excess current detector operates and further soaring of V- pin voltage higher than V_{short} makes the short circuit protector enabled. This leads the external discharge control Nch MOSFET turn off with the Dout pin being at “L” level.

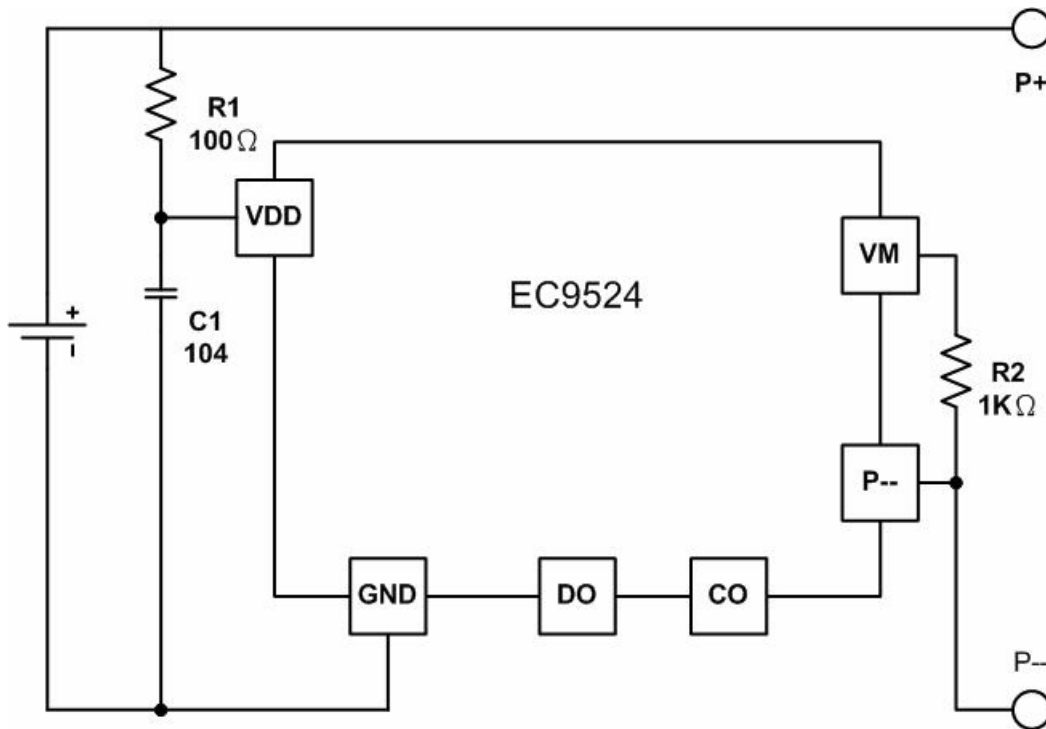
An output delay time for the excess current detector is internally fixed, 13ms typ. At $V_{DD} = 3.0\text{V}$. A quick recovery of V- pin level from a value between V_{short} and VDET3 within the delay time keeps the discharge control FET staying “H” state.

When the short circuit protector is enabled, the Dout would be low and its delay time would be $5\mu\text{s}$ typ. The V- pin has a built-in pulled down resistor, typ. $100\text{k}\Omega$ with connecting to the V_{SS} pin.

After an excess current or short circuit protection is detected, removing a cause of excess current or external short circuit makes an external discharge control FET to an “ON” state automatically with the V- pin level being down to the V_{SS} level through pulled down resistor built-in internally.

If V_{DD} voltage would be higher than VDET2 at a time when the excess current is detected the EC9525 does not enter a standby mode, or otherwise in case of lower V_{DD} voltage than VDET2 would lead the EC9525 into a standby. After detecting short circuit the EC9525 will not enter a standby mode.

Application Circuits



Application Hints

R1 and C1 will stabilize a supply voltage to the EC9525. A recommended R1 value is less than 1kOhm. A larger value of R1 leads higher detection voltage, makes some errors, because of shoot through current flowed in the EC9525.

R1 and R2 may cause power consumption over rating of power dissipation of the EC9525 and a total of “R1+R2” should be more than 1kOhm.



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