



# 74ABT126 Quad Buffer with 3-STATE Outputs

## **Features**

- Non-inverting buffers
- Output sink capability of 64mA, source capability of 32mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

## **General Description**

The ABT126 contains four independent non-inverting buffers with 3-STATE outputs.

# **Ordering Information**

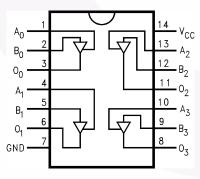
Order Number	Package Number	Package Description
74ABT126CSC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ABT126CSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT126CMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

# **Connection Diagram**



## **Pin Description**

Pin Names	Description
A <sub>n</sub> , B <sub>n</sub>	Inputs
O <sub>n</sub>	Outputs

## **Function Table**

Inp	uts	Output
An	B <sub>n</sub>	O <sub>n</sub>
Н	L	L
Н	Н	Н
L	Х	Z

H = HIGH Voltage Level

L = LOW Voltage Level

Z = HIGH Impedance

X = Immaterial

## **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T <sub>STG</sub>	Storage Temperature	−65°C to +150°C
T <sub>A</sub>	Ambient Temperature Under Bias	–55°C to +125°C
T <sub>J</sub>	Junction Temperature Under Bias	−55°C to +150°C
V <sub>CC</sub>	V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
V <sub>IN</sub>	Input Voltage <sup>(1)</sup>	-0.5V to +7.0V
I <sub>IN</sub>	Input Current <sup>(1)</sup>	-30mA to +5.0mA
V <sub>O</sub>	Voltage Applied to Any Output	
	Disabled or Power-Off State	-0.5V to 5.5V
	HIGH State	–0.5V to V <sub>CC</sub>
	Current Applied to Output in LOW State (Max.)	twice the rated I <sub>OL</sub> (mA)
	DC Latchup Source Current (Across Comm Operating Range)	-300mA
	Over Voltage Latchup (I/O)	10V

#### Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

# **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T <sub>A</sub>	Free Air Ambient Temperature	-40°C to +85°C
V <sub>CC</sub>	Supply Voltage	+4.5V to +5.5V
ΔV / Δt	Minimum Input Edge Rate	
	Data Input	
	Enable Input	100mV/ns

# **DC Electrical Characteristics**

Symbol	Parameter		V <sub>CC</sub>	Conditions	Min.	Тур.	Max.	Units
V <sub>IH</sub>	Input HIGH Voltage			Recognized HIGH Signal	2.0			V
V <sub>IL</sub>	Input LOW Voltage			Recognized LOW Signal			0.8	V
V <sub>CD</sub>	Input Clam	o Diode Voltage	Min.	I <sub>IN</sub> = -18mA			-1.2	V
V <sub>OH</sub>	Output HIG	H Voltage	Min.	$I_{OH} = -3mA$	2.5			V
				$I_{OH} = -32mA$	2.0			
V <sub>OL</sub>	Output LOV	V Voltage	Min.	I <sub>OL</sub> = 64mA			0.55	V
I <sub>IH</sub>	Input HIGH	Current	Max.	$V_{IN} = 2.7V^{(2)}$			1	μA
				$V_{IN} = V_{CC}$			1	
I <sub>BVI</sub>	Input HIGH Test	Current Breakdown	Max.	V <sub>IN</sub> = 7.0V			7	μA
I <sub>IL</sub>	Input LOW	Current	Max.	$V_{IN} = 0.5V^{(2)}$			-1	μA
				$V_{IN} = 0.0V$			-1	
V <sub>ID</sub>	Input Leakage Test		0.0	I <sub>ID</sub> = 1.9μA, All Other Pins Grounded	4.75			V
I <sub>OZH</sub>	Output Leakage Current		0-5.5V	$V_{OUT} = 2.7V$ , $\overline{OE}_n = 2.0V$			10	μA
I <sub>OZL</sub>	Output Leakage Current		0-5.5V	$V_{OUT} = 0.5V$ , $\overline{OE}_n = 2.0V$			-10	μΑ
Ios	Output Short-Circuit Current		Max.	$V_{OUT} = 0.0V$	-100		-275	mA
I <sub>CEX</sub>	Output HIG	H Leakage Current	Max.	$V_{OUT} = V_{CC}$			50	μΑ
I <sub>ZZ</sub>	Bus Draina	ge Test	0.0	V <sub>OUT</sub> = 5.5V, All Others GND			100	μΑ
I <sub>CCH</sub>	Power Supp	oly Current	Max.	All Outputs HIGH			50	μΑ
I <sub>CCL</sub>	Power Supp	oly Current	Max.	All Outputs LOW			15	mA
I <sub>CCZ</sub>	Power Supply Current		Max.	$\overline{OE}_n = V_{CC}$ , All Others at $V_{CC}$ or Ground			50	μA
I <sub>CCT</sub>	Additional Outputs Enabled		Max.	$V_I = V_{CC} - 2.1V$			1.5	mA
	I <sub>CC</sub> /Input	Outputs 3-STATE		Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V			1.5	mA
	Outputs 3-STATE			Data Input $V_I = V_{CC} - 2.1V$ , All Others at $V_{CC}$ or Ground			50	μA
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> No Load <sup>(2)</sup>		Max.	Outputs OPEN, $\overline{OE}_n = \text{GND}^{(3)}$ , One-Bit Toggling, 50% Duty Cycle			0.1	mA/ MHz

## Notes:

- 2. Guaranteed, but not tested.
- 3. For 8-bit toggling,  $I_{CCD} < 0.8 mA/MHz$ .

# **AC Electrical Characteristics**

		$T_A = +25$ °C, $V_{CC} = +5$ V, $C_L = 50$ pF		C, V, F	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V} -5.5\text{V}$ $C_L = 50\text{pF}$		
Symbol	Parameter	Min.	Тур.	Max.	Min.	Max.	Units
t <sub>PLH</sub>	Propagation Delay, Data to Outputs	1.0		4.4	1.0	4.4	ns
t <sub>PHL</sub>		1.0		4.6	1.0	4.6	
t <sub>PZH</sub>	Output Enable Time	1.0		6.5	1.0	6.5	ns
t <sub>PZL</sub>		1.0		6.5	1.0	6.5	
t <sub>PHZ</sub>	Output Disable Time	1.0		5.8	1.0	5.8	ns
t <sub>PLZ</sub>		1.0		5.5	1.0	5.5	

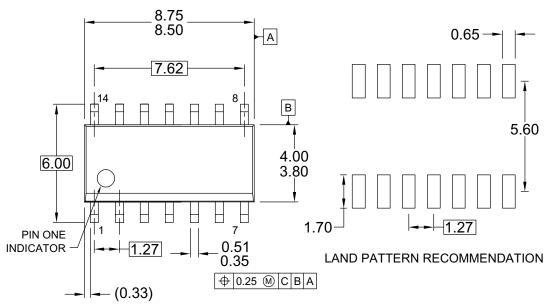
# Capacitance

Symbol	Parameter	Conditions T <sub>A</sub> = 25°C	Тур.	Units
C <sub>IN</sub>	Input Capacitance	$V_{CC} = 0V$	5.0	pF
C <sub>OUT</sub> <sup>(4)</sup>	Output Capacitance	$V_{CC} = 5.0V$	9.0	pF

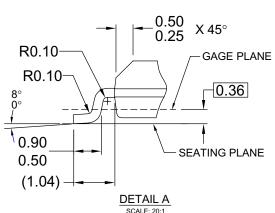
### Note:

4.  $C_{OUT}$  is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

## **Physical Dimensions**







A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,

NOTES: UNLESS OTHERWISE SPECIFIED

- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

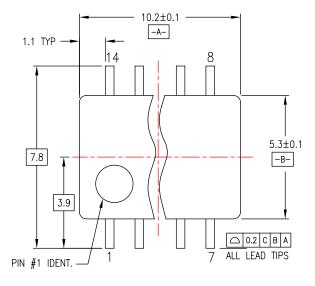
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

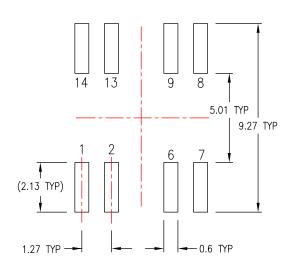
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

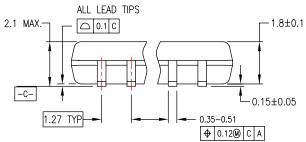
http://www.fairchildsemi.com/packaging/

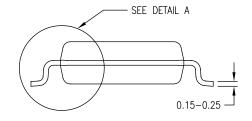
## Physical Dimensions (Continued)





LAND PATTERN RECOMMENDATION



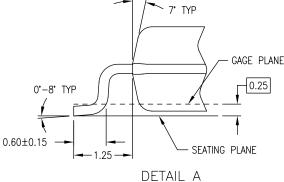


DIMENSIONS ARE IN MILLIMETERS

### NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  B. DIMENSIONS ARE IN MILLIMETERS.
  C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD

FLASH, AND TIE BAR EXTRUSIONS.



M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/

## Physical Dimensions (Continued) 5.0±0.1 -A-0.65 0.43 TYP 6.4 4.4±0.1 -B-1.65 3.2 □ 0.2 C B A PIN #1 IDENT. 6.10 0.45 -LAND PATTERN RECOMMENDATION SEE DETAIL A ALL LEAD TIPS 0.90+0.15 1.2 MAX □ 0.1 C 0.09-0.20 -C-0.10±0.05 0.65 0.19 - 0.30⊕ |0.13\( \omega \ \omega \omega \ \omega \ \omega \ \omega \ \omega \omega \ \omeg 12.00°TOP & BOTTOM R0.09 min GAGE PLANE 0.25 0°-8° NOTES: 0.6±0.1 A. CONFORMS TO JEDEC REGISTRATION MO-153, SEATING PLANE R0.09min VARIATION AB, REF NOTE 6 -1 00 **B. DIMENSIONS ARE IN MILLIMETERS DETAIL A**

- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: <a href="http://www.fairchildsemi.com/packaging/">http://www.fairchildsemi.com/packaging/</a>





#### **TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

Build it Now<sup>TM</sup>
CorePLUS<sup>TM</sup>
CROSSVOLT<sup>TM</sup>
CTL<sup>TM</sup>

Current Transfer Logic™ EcoSPARK<sup>®</sup> EZSWITCH™ \*

FI M

Fairchild<sup>®</sup>
Fairchild Semiconductor<sup>®</sup>
FACT Quiet Series<sup>™</sup>

FACT<sup>®</sup>
FAST<sup>®</sup>
FastvCore<sup>™</sup>
FlashWriter<sup>®</sup>\*

FPS™ FRFET®

Global Power Resource<sup>sм</sup>

Green FPS™

Green FPS™ e-Series™ GTO™

*i-Lo™* IntelliMAX™ ISOPLANAR™ MegaBuck™

MICROCOUPLER™ MicroFET™ MicroPak™

MillerDrive™ Motion-SPM™ OPTOLOGIC® OPTOPLANAR® PDP-SPM™ Power220® Power247® POWEREDGE® Power-SPM™ PowerTrench®

Programmable Active Droop™

QFĒT<sup>®</sup> QS™

QT Optoelectronics™ Quiet Series™ RapidConfigure™ SMART START™

SPM<sup>®</sup>
STEALTH™
SuperFET™
SuperSOT™-3

SuperSOT<sup>TM</sup>-6
SuperSOT<sup>TM</sup>-8

SyncFET™

SYSTEM®

GENERAL

The Power Franchise®

Franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®

Ultra FRFET™ UniFET™ VCX™

\* EZSWITCH™ and FlashWriter® are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

#### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

#### As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification		Definition		
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.		
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.		
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.		
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.		

Rev. 132

ON Semiconductor and in are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at <a href="www.onsemi.com/site/pdf/Patent-Marking.pdf">www.onsemi.com/site/pdf/Patent-Marking.pdf</a>. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor and see no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and h

## **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5817–1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative