FINAL

Am27H010
1 Megabit (131,072 x 8-Bit) High Speed CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  — 45 ns
- **JEDEC-approved pinout**
  — Plug in upgrade of standard 1 Mbit EPROMs
  — Easy upgrade from 28-pin JEDEC EPROMs
- **Single +5 V power supply**
- **±10% power supply tolerance available**

- **100% Flashrite™ programming**
  — Typical programming time of 16 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP, PDIP, LCC and PLCC packages**
- **DESC SMD No. 5962-89614**

GENERAL DESCRIPTION

The Am27H010 is a 1 Mbit ultraviolet erasable programmable read-only memory. It is organized as 131,072 words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 45 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27H010 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$)

controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 220 mW in active mode, and 50 mW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27H010 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming time of 16 seconds.
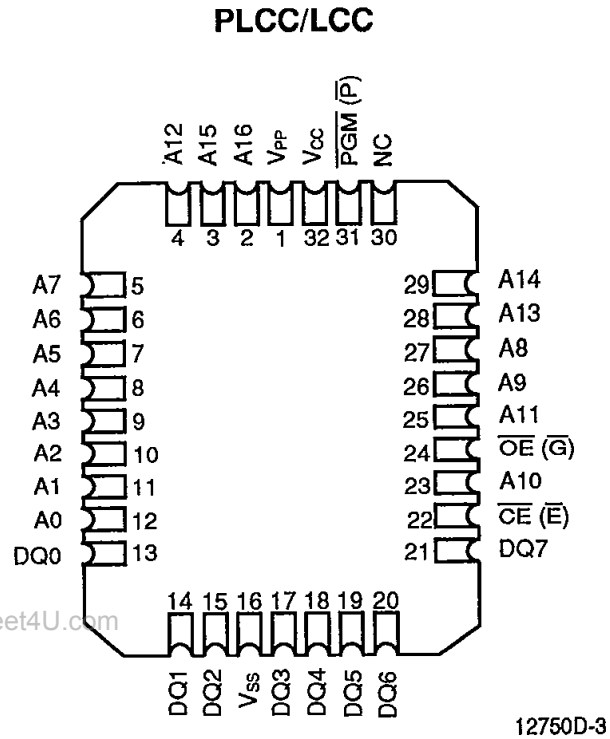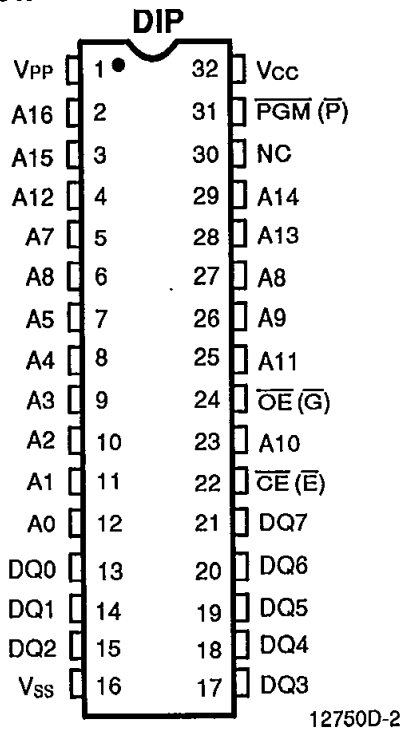
BLOCK DIAGRAM

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AMD
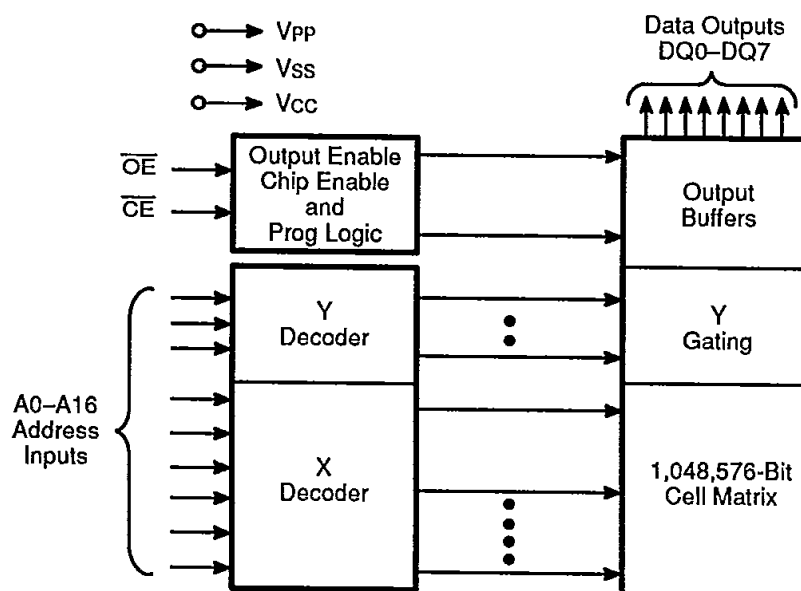
PRODUCT SELECTOR GUIDE

| Family Part No.	Am27H010			
Ordering Part No: Vcc ±5%	-45V05			-90V05
Vcc ±10%	-45	-55	-70	-90
Max Access Time (ns)	45	55	70	90
$\overline{CE}$ (E) Access (ns)	45	55	70	90
$\overline{OE}$ (G) Access (ns)	20	25	35	40

CONNECTION DIAGRAMS

Top View

DIP

Vpp	1	32	Vcc
A16	2	31	$\overline{PGM}$ (P)
A15	3	30	NC
A12	4	29	A14
A7	5	28	A13
A8	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{OE}$ (G)
A2	10	23	A10
A1	11	22	$\overline{CE}$ (E)
A0	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
Vss	16	17	DQ3

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PLCC/LCC

Top pins (4 3 2 1 32 31 30): A12, A15, A16, Vpp, Vcc, $\overline{PGM}$ (P), NC

Left side:
A7 - 5
A6 - 6
A5 - 7
A4 - 8
A3 - 9
A2 - 10
A1 - 11
A0 - 12
DQ0 - 13

Right side:
29 - A14
28 - A13
27 - A8
26 - A9
25 - A11
24 - $\overline{OE}$ (G)
23 - A10
22 - $\overline{CE}$ (E)
21 - DQ7

Bottom pins (14 15 16 17 18 19 20): DQ1, DQ2, Vss, DQ3, DQ4, DQ5, DQ6

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Note:

1. JEDEC nomenclature is in parentheses.

PIN DESIGNATIONS

A0–A16	=	Address Inputs
$\overline{CE}$ (E)	=	Chip
DQ0–DQ7	=	Data Inputs/Outputs
NC	=	No Internal Connection
$\overline{OE}$ (G)	=	Output Enable Input
$\overline{PGM}$ (P)	=	Program Enable Input
Vcc	=	Vcc Supply Voltage
Vpp	=	Program Supply Voltage
Vss	=	Ground

LOGIC SYMBOL

17 → A0–A16

DQ0–DQ7 ← 8

$\overline{CE}$ (E) →
$\overline{PGM}$ (P) →
$\overline{OE}$ (G) →

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Am27H010

AMD ◢◣
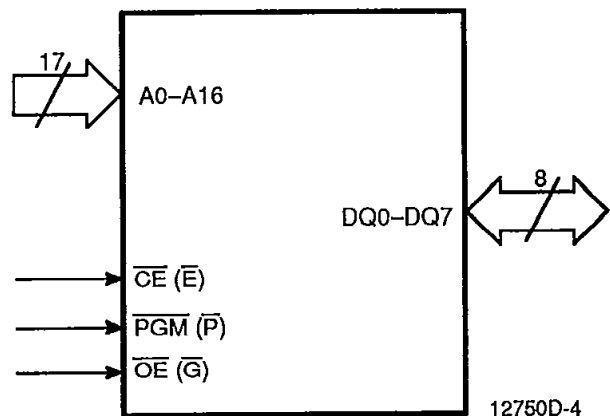
ORDERING INFORMATION
EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

```
AM27H010    -45    D    C    B
```

OPTIONAL PROCESSING
Blank = Standard Processing
   B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended Commercial (–55°C to +125°C)

PACKAGE TYPE
D = 32-Pin Ceramic DIP (CDV032)
L = 32-Pin Ceramic Leadless Chip Carrier (CLV032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER
Am27H010
1 Megabit (131,072 x 8-Bit) High Speed CMOS EPROM
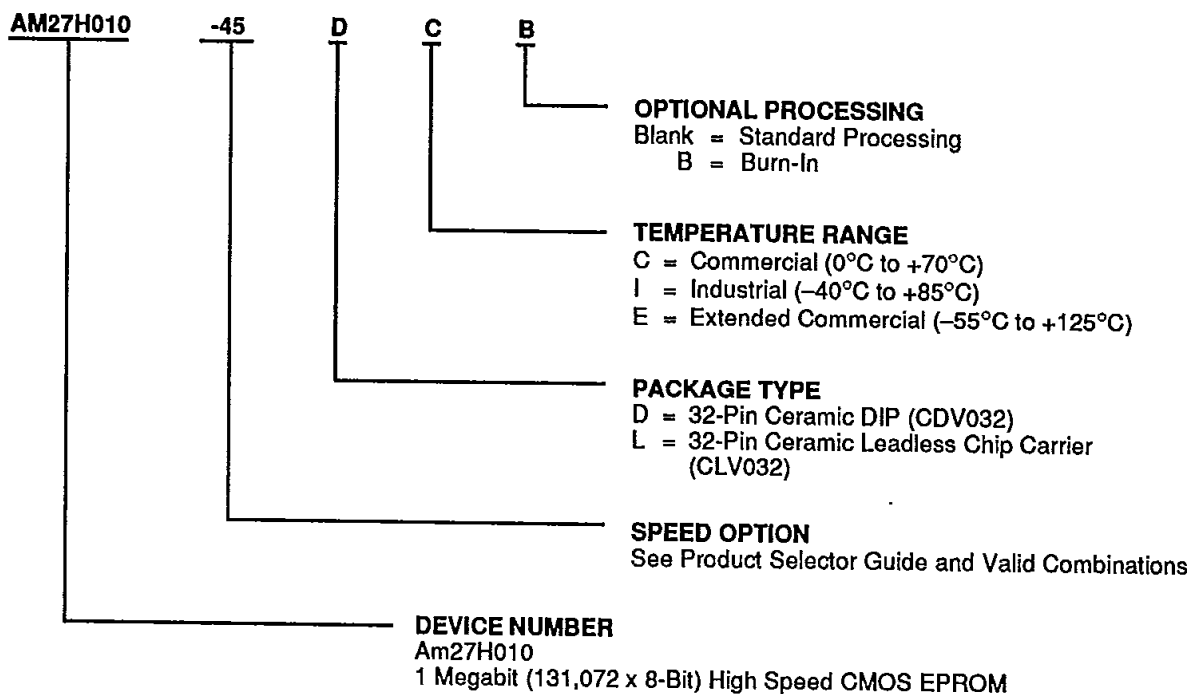
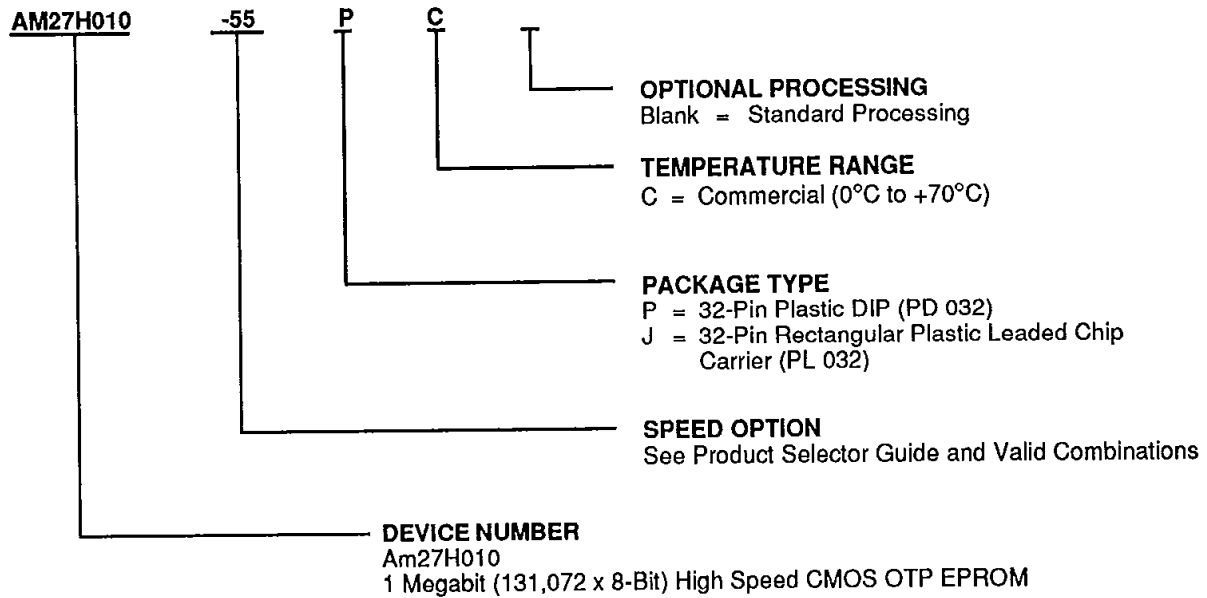| Valid Combinations	
AM27H010-45	DC, DCB, DI, DIB, LC, LI, LCB, LIB
AM27H010-45V05	
AM27H010-55	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27H010-70	
AM27H010-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Am27H010

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AMD

ORDERING INFORMATION
OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
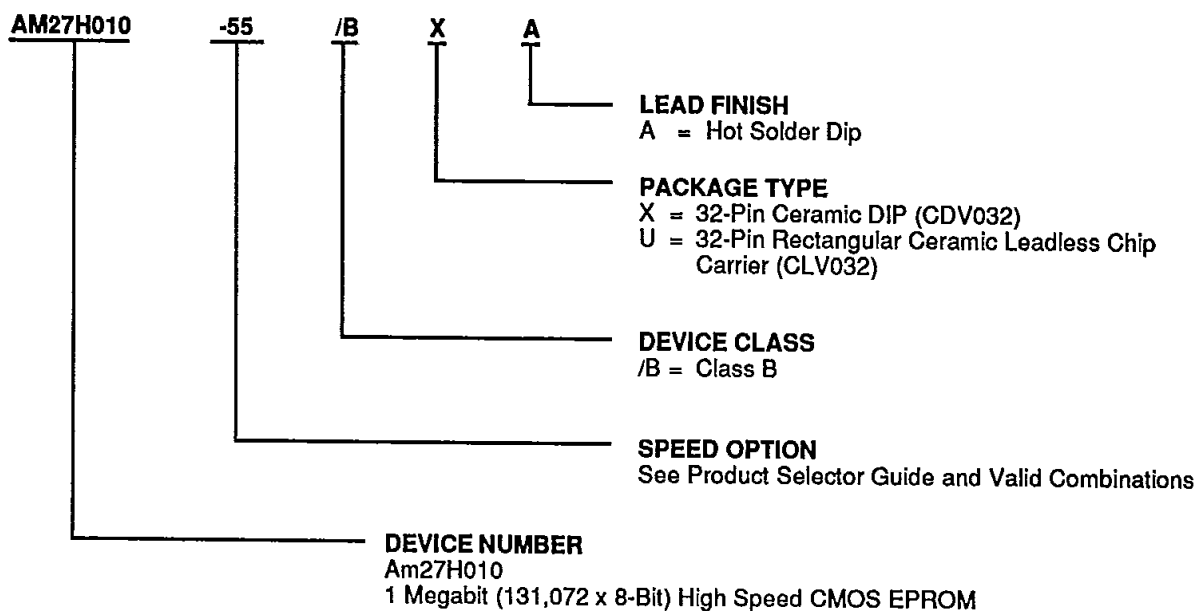
AM27H010   -55   P   C

OPTIONAL PROCESSING
Blank = Standard Processing

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER
Am27H010
1 Megabit (131,072 x 8-Bit) High Speed CMOS OTP EPROM

Valid Combinations	
AM27H010-55	
AM27H010-70	PC, JC
AM27H010-90	
AM27H010-90V05	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

```
AM27H010        -55      /B      X      A
```

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CDV032)
U = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLV032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER
Am27H010
1 Megabit (131,072 x 8-Bit) High Speed CMOS EPROM

Valid Combinations	
AM27H010-55	
AM27H010-70	/BXA, /BUA
AM27H010-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests
Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

AMD

FUNCTIONAL DESCRIPTION
Erasing the Am27H010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27H010 to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase an Am27H010. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Å—with intensity of 12,000 µW/cm² for 15 to 20 minutes. The Am27H010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27H010 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27H010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27H010

Upon delivery or after each erasure the Am27H010 has all 1,048,576 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27H010 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP}, $\overline{CE}$ and $\overline{PGM}$ is at V_{IL} and $\overline{OE} = V_{IH}$.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27H010. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V_{CC} = V_{PP} = 5.25 V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27H010 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27H010 may be common. A TTL low-level program pulse applied to an Am27H010 $\overline{CE}$ input and with V_{PP} = 12.75 V ± 0.25 V, $\overline{PGM}$ Low and $\overline{OE}$ High will program that Am27H010. A high-level $\overline{CE}$ input inhibits the other Am27H010 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27H010.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27H010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device code. For the Am27H010, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27H010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{OE}). Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27H010 has a standby mode which reduces the maximum V_{CC} current to 50% of the active current. It is placed in standby mode when $\overline{CE}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The Am27H010 is specified with 50% of the address lines

toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce the actual standby current.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$/Vpp be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and Vss to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between Vcc and Vss for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode	Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	Vpp	Outputs
Read		V_{IL}	V_{IL}	X	A0	A9	V_{IH}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	x	V_{IH}	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{IH}	Hi-Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	Vcc	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	Vcc	0EH

Notes:

1. $V_H = 12.0\ V \pm 0.5\ V$
2. X = Either V_{IH} or V_{IL}
3. A1–A8 = A10–A18 = V_{IL}
4. The Am27H010 uses the same Flashrite algorithm as the Am27C010.

AMD

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products . . . . −65°C to +125°C

All Other Products . . . . −65°C to +150°C

Ambient Temperature
with Power Applied . . . . −55°C to +125°C

Voltage with Respect to V_{SS}
All pins except A9,V_{PP},V_{CC} . . . −0.6 V to V_{CC} + 0.5 V
(Note 1)

A9 and V_{PP} (Note 2) . . . . −0.6 V to +13.5 V

V_{CC} . . . . −0.6 V to +7.0 V

Notes:

1. Minimum DC voltage on input or I/O pins is −0.5 V. During transitions, the inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

2. For A9 and V_{PP} the minimum DC input is −0.5 V. During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

    Case Temperature (Tc) . . . . 0°C to +70°C

Industrial (I) Devices

    Case Temperature (Tc) . . . . −40°C to +85°C

Extended Commercial (E) Devices

    Case Temperature (Tc) . . . . −55°C to +125°C

Military (M) Devices

    Case Temperature (Tc) . . . . −55°C to +125°C

Supply Read Voltages

    V_{CC} for Am27H010-XXV05 . . . +4.75 V to +5.25 V

 V_{CC} for Am27H010-XX0 . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, 3 and 4) (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -4$ mA		2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 12$ mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage			-0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$	C/I Devices		1.0	μA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$	C/I Devices		10	μA
			E/M Devices		10	
I_{CC1}	Vcc Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 10 MHz $I_{OUT} = 0$ mA	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{IH}$	C/I Devices		25	mA
			E/M Devices		35	
I_{PP1}	Vpp Current During Read	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$			100	μA

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. **Caution:** The Am27H010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.

3. I_{CC1} is tested with $\overline{OE}/V_{PP} = V_{IH}$ to simulate open outputs.

4. Minimum DC Input Voltage is -0.5 V. During transitions, the inputs may overshoot to -2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is $V_{CC} + 0.5$ V, which may overshoot to $V_{CC} + 2.0$ V for periods less than 20 ns.
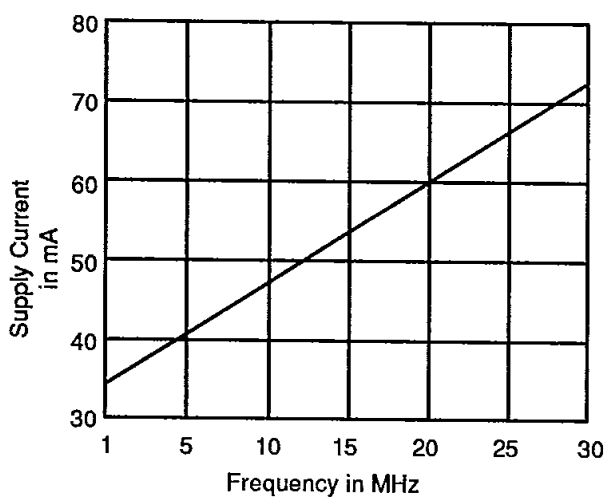
12750D-5

Figure 1. Typical Supply Current vs. Frequency
$V_{CC} = 5.0$ V, T = 25°C
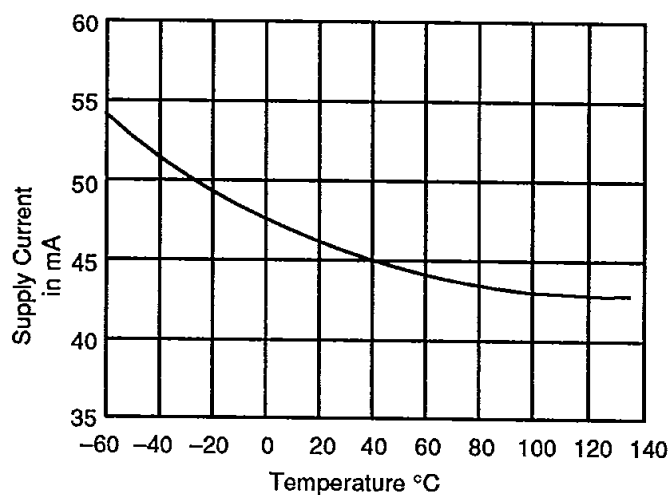
12750D-6

Figure 2. Typical Supply Current vs. Temperature
$V_{CC} = 5.0$ V, f = 10 MHz

AMD

CAPACITANCE

| Parameter Symbol	Parameter Description	Test Conditions	CDV032 Typ	CDV032 Max	CLV032 Typ	CLV032 Max	PD 032 Typ	PD 032 Max	PL 032 Typ	PL 032 Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	12	6	12	8	12	8	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	15	6	15	10	15	10	15	pF

Notes:

1. This parameter is only sampled and not 100% tested.

2. $T_A = +25°C$, $f = 1$ MHz.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3 and 4) (for APL Products, Group A, Subgroups 9,10 and 11 are tested unless otherwise noted)

Parameter Symbols JEDEC	Parameter Symbols Standard	Parameter Description	Test Conditions		Am27H010 -45V05 -45	Am27H010 -55	Am27H010 -70	Am27H010 -90V05 -90	Unit
t_{AVQV}	t_{RCC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $C_L = C_{L1}$	Min					ns
				Max	45	55	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$ $C_L = C_{L1}$	Min					ns
				Max	45	55	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$ $C_L = C_{L1}$	Min					ns
				Max	20	25	35	40	ns
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float	$C_L = C_{L2}$	Min	0	0	0	0	ns
				Max	20	25	35	40	ns
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	ns
				Max					ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. This parameter is only sampled and not 100% tested.

3. **Caution:** The Am27H010 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.

4. Output Load: 1 TTL gate and $C = C_L$
   Input Rise and Fall Times: 5 ns
   Input Pulse Levels: 0 V to 3 V.
   Timing Measurement Reference Level: 1.5 V for inputs and outputs
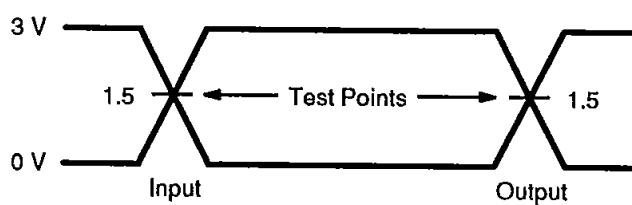
SWITCHING TEST CIRCUIT
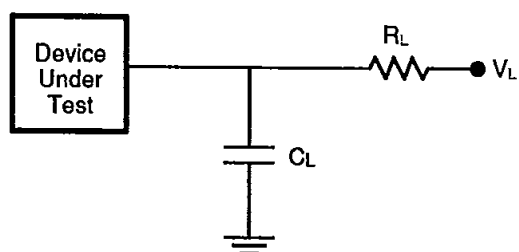
$R_L = 121\ \Omega$
$V_L = 1.9\ V$
$C_{L1} = 30\ pF$
$C_{L2} = 5\ pF$

12750D-7

## SWITCHING TEST WAVEFORM

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AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0." Input pulse rise and fall times are ≤ 5 ns.

AMD

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
————	Must Be Steady	Will Be Steady
\\\\\	May Change from H to L	Will Be Changing from H to L
/////	May Change from L to H	Will Be Changing from L to H
XXXXX	Don't Care, Any Change Permitted	Changing State Unknown
>>—<<	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS

12750D-9
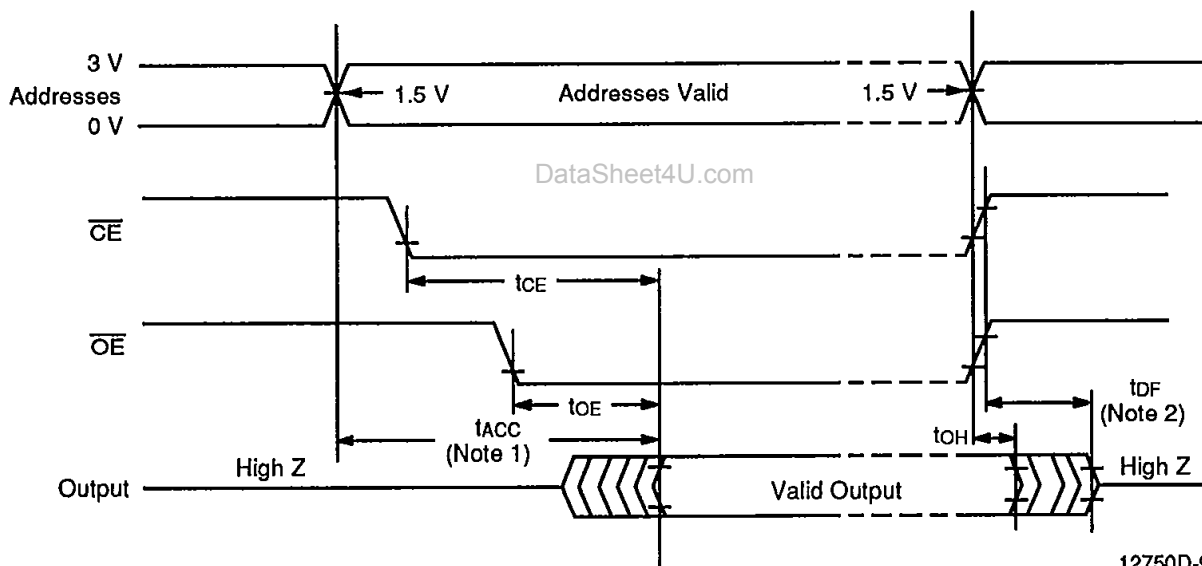
Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.

2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.