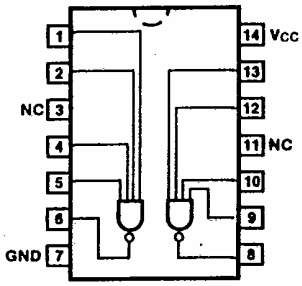
54S/74S140

DUAL 4-INPUT NAND LINE DRIVER

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S140PC		9A
Ceramic DIP (D)	A	74S140DC	54S140DM	6A
Flatpak (F)	A	74S140FC	54S140FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74S (U.L.) HIGH/LOW
Inputs	2.5/2.5
Outputs	75/37.5

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74S Min	54/74S Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.0		V	V_{CC} = Min, V_{IN} = 0.5 V, R_0 = 50 Ω to Gnd
V_{OL}	Output LOW Voltage		0.5	V	V_{CC} = Min, I_{OL} = 60 mA V_{IN} = 2.0 V
I_{OS}	Output Short Circuit Current	-50	-225	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CCH}	Power Supply Current		18	mA	V_{IN} = Gnd; V_{CC} = Max
I_{CCL}			44		V_{IN} = Open; V_{CC} = Max
t_{PLH}	Propagation Delay		6.5	ns	Figs. 3-1, 3-4
t_{PHL}			6.5		

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.