FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27237-2E

ASSP for Power Supply Applications

(DC/DC converter for DSC/camcorder)

5 ch DC/DC Converter IC with Synchronous Rectification

MB39A108

■ DESCRIPTION

The MB39A108 is 5-channel DC/DC converter IC using pulse width modulation (PWM), and is suitable for up conversion, down conversion, and up/down conversion. The MB39A108 is built in 5 channels into TSSOP-38P/ BCC-40P package and operates at 2 MHz maximum. Each channel can be controlled with soft-start.

The MB39A108 is suitable for power supply of high performance portable instruments such as DSC.

■ FEATURES

- Supports for down-conversion with synchronous rectification (CH1)
- Supports for down-conversion and up/down Zeta conversion (CH2, CH3)
- Supports for up-conversion and up/down Sepic conversion (CH4, CH5)
- Low voltage start-up (CH4, CH5) : 1.7 V
- Power supply voltage range : 2.5 V to 11 V
- Reference voltage : 2.0 V ± 1%
- Error amplifier threshold voltage : 1.00 V ± 1% (CH1), 1.23 V ± 1% (CH2 to CH5)
- Oscillation frequency range : 200 kHz to 2.0 MHz
- Standby current : 0 µA (Typ)

- Built-in soft-start circuit independent of loads
- Built-in totem-pole type output for MOS FET
- Short-circuit detection capability by external signal (– INS terminal)
- Two types of package (TSSOP-38 pin : 1 type, BCC-40 pin : 1 type)

■ APPLICATIONS

- Digital still camera (DSC)
- Digital video camera (DVC)
- Surveillance camera etc.

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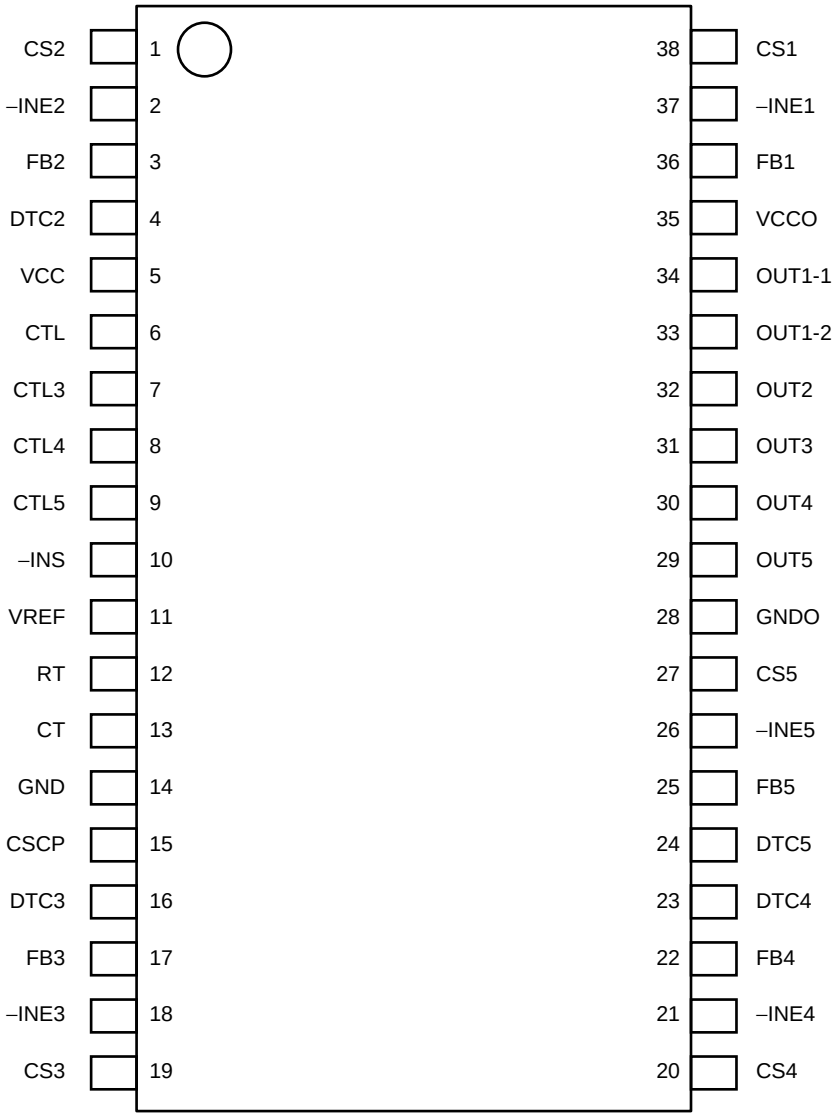
■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-38P-M03)

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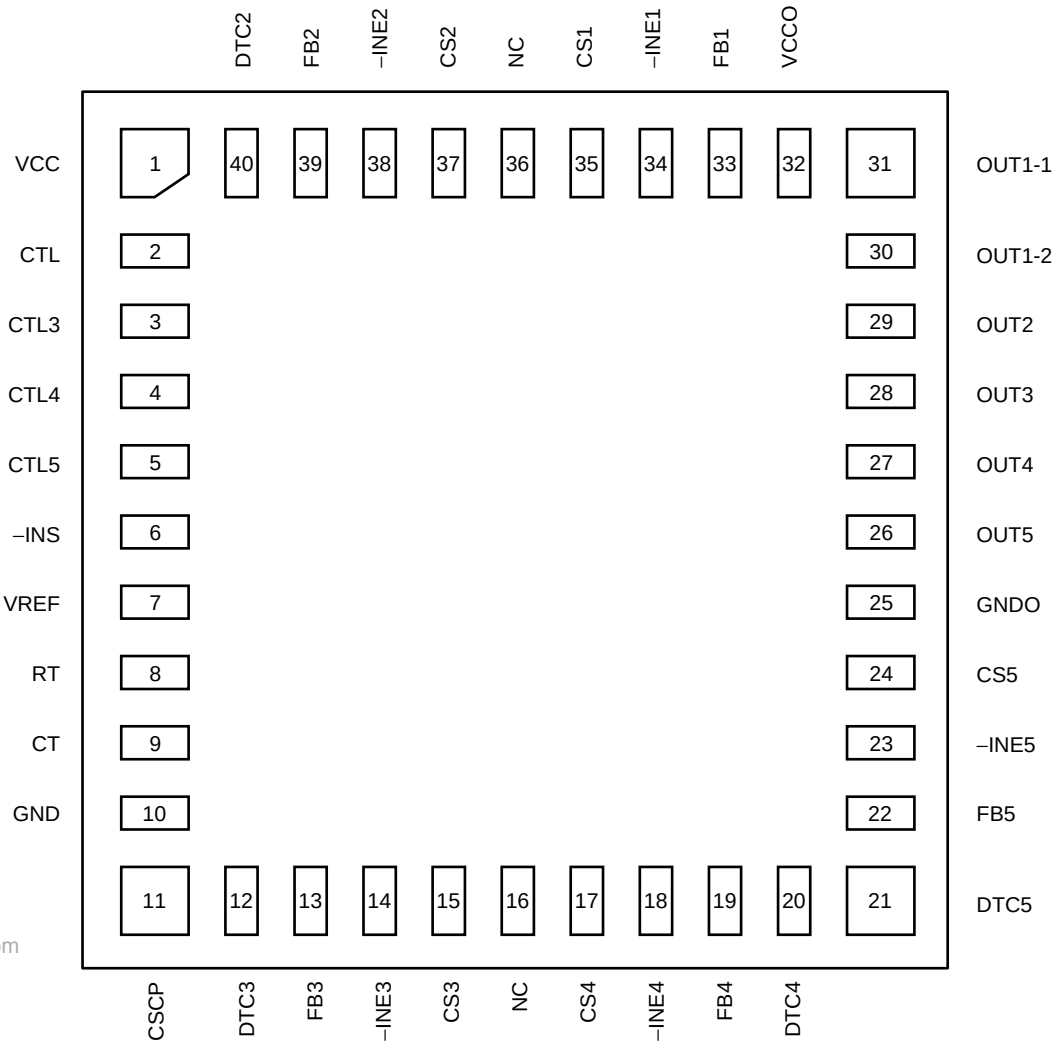
<TOP VIEW (Penetration diagram from surface)>



(LCC-40P-M07)

■ PIN DESCRIPTION

Block	Pin No. PKG TSSOP	Pin No. PKG BCC	Pin name	I/O	Description
CH1	36	33	FB1	O	Error amplifier output terminal.
	37	34	– INE1	I	Error amplifier inverted input terminal.
	38	35	CS1	—	Soft-start setting capacitor connection terminal.
	34	31	OUT1-1	O	P-ch drive output terminal (External main side FET gate driving).
	33	30	OUT1-2	O	N-ch drive output terminal (External synchronous rectification side FET gate driving).
CH2	4	40	DTC2	I	Dead time control terminal.
	3	39	FB2	O	Error amplifier output terminal
	2	38	– INE2	I	Error amplifier inverted input terminal.
	1	37	CS2	—	Soft-start setting capacitor connection terminal.
	32	29	OUT2	O	P-ch drive output terminal.
CH3	16	12	DTC3	I	Dead time control terminal.
	17	13	FB3	O	Error amplifier output terminal
	18	14	– INE3	I	Error amplifier inverted input terminal.
	19	15	CS3	—	Soft-start setting capacitor connection terminal.
	31	28	OUT3	O	P-ch drive output terminal.
CH4	23	20	DTC4	I	Dead time control terminal.
	22	19	FB4	O	Error amplifier output terminal.
	21	18	– INE4	I	Error amplifier inverted input terminal.
	20	17	CS4	—	Soft-start setting capacitor connection terminal.
	30	27	OUT4	O	N-ch drive output terminal.
CH5	24	21	DTC5	I	Dead time control terminal.
	25	22	FB5	O	Error amplifier output terminal.
	26	23	– INE5	I	Error amplifier inverted input terminal.
	27	24	CS5	—	Soft-start setting capacitor connection terminal.
	29	26	OUT5	O	N-ch drive output terminal.
OSC	13	9	CT	—	Triangular wave frequency setting capacitor connection terminal.
	12	8	RT	—	Triangular wave frequency setting resistor connection terminal.

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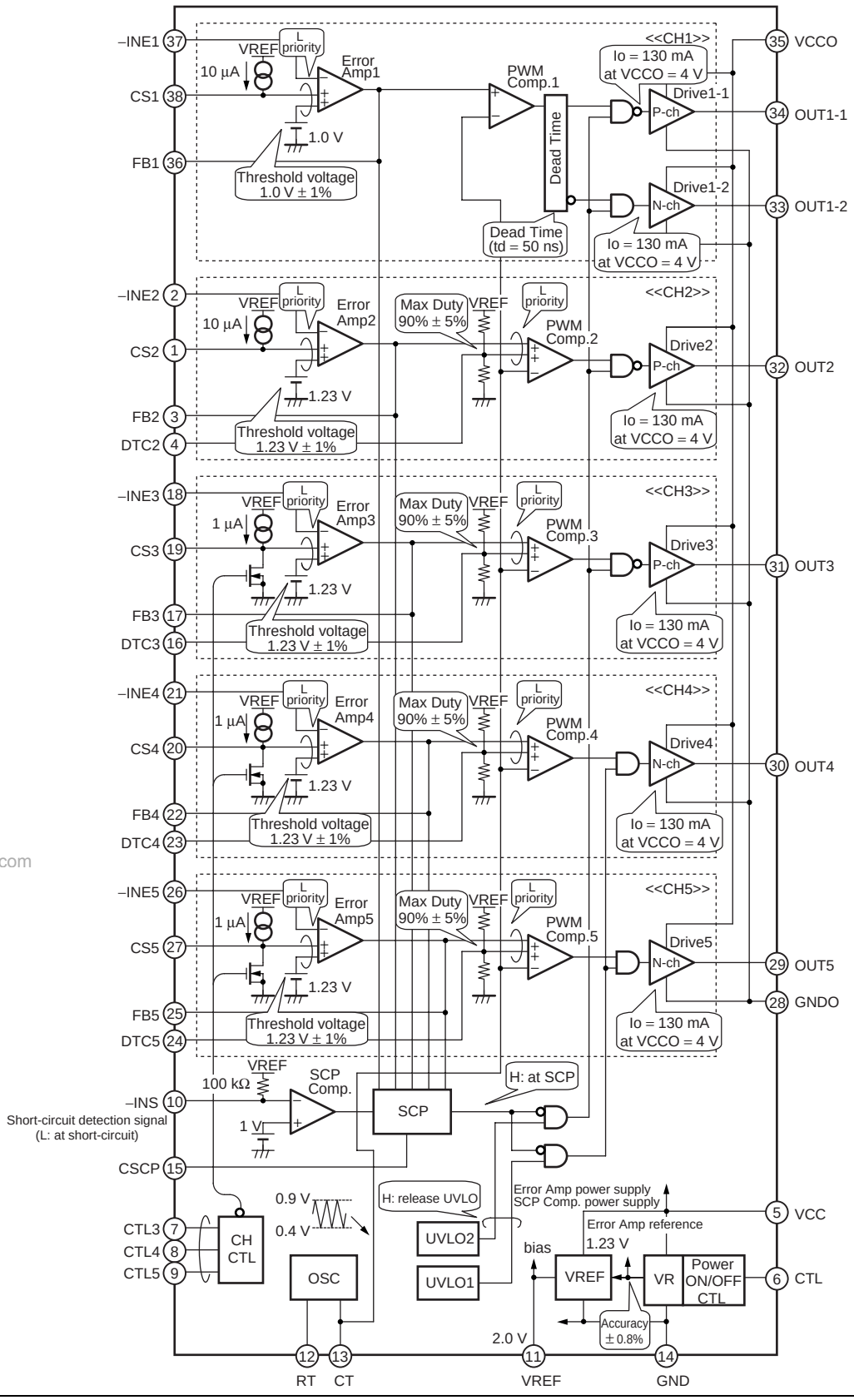
Block	Pin No. PKG TSSOP	Pin No. PKG BCC	Pin name	I/O	Description
Control	6	2	CTL	I	Power supply control terminal.
	7	3	CTL3	I	CH3 control terminal.
	8	4	CTL4	I	CH4 control terminal.
	9	5	CTL5	I	CH5 control terminal.
	15	11	CSCP	—	Short-circuit detection circuit capacitor connection terminal.
	10	6	– INS	I	Short-circuit detection comparator inverted input terminal.
Power	35	32	VCCO	—	Drive output block power supply terminal.
	5	1	VCC	—	Power supply terminal.
	11	7	VREF	O	Reference voltage output terminal.
	28	25	GNDO	—	Drive output block ground terminal.
	14	10	GND	—	Ground terminal.

Note : The terminal number which has been described in the text is the one of the TSSOP-38P package after this.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC, VCCO terminal	—	12	V
Output current	I_O	OUT1 to OUT5 terminal	—	20	mA
Peak output current	I_{OP}	OUT1 to OUT5 terminal Duty ≤ 5% (t = 1/fosc × Duty)	—	400	mA
Power dissipation	P_D	Ta ≤ + 25 °C (TSSOP-38P)	—	1680*1	mW
		Ta ≤ + 25 °C (BCC-40P)	—	1020*2	mW
Storage temperature	T_{STG}	—	− 55	+ 125	°C

*1 : When mounted on a 76 mm × 76 mm × 1.6 mm FR-4 boards.

*2 : When mounted on a 117 mm × 84 mm × 0.8 mm FR-4 boards.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Start power supply voltage	V_{CC}	VCC, VCCO terminal (CH4, CH5)	1.7	—	11	V
Power supply voltage	V_{CC}	VCC, VCCO terminal (CH1 to CH5)	2.5	4	11	V
Reference voltage output current	I_{REF}	VREF terminal	− 1	—	0	mA
Input voltage	V_{INE}	− INE1 to − INE5 terminal	0	—	V_{CC} − 0.9	V
		− INS terminal	0	—	V_{REF}	V
	V_{DTC}	DTC2 to DTC5 terminal	0	—	V_{REF}	V
Control input voltage	V_{CTL}	CTL, CTL3 to CTL5 terminal	0	—	11	V
Output current	I_O	OUT1 to OUT5 terminal	− 15	—	+ 15	mA
Oscillation frequency	f_{OSC}	*	0.2	0.97	2.0	MHz
Timing capacitor	C_T	—	27	100	680	pF
Timing resistor	R_T	—	3.0	6.8	39	kΩ
Soft-start capacitor	C_S	CS1 to CS5 terminal	—	0.1	1.0	μF
Short-circuit detection capacitor	C_{SCP}	—	—	0.1	1.0	μF
Reference voltage output capacitor	C_{REF}	—	—	0.1	1.0	μF
Operating ambient temperature	Ta	—	− 30	+ 25	+ 85	°C

* : Refer to "■ SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY".

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = VCCO = 4 V, Ta = + 25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Reference voltage block [VREF]	Output voltage	V_{REF1}	11	VREF = 0 mA	1.98	2.00	2.02	V
		V_{REF2}	11	V_{CC} = 2.5 V to 11 V	1.975	2.000	2.025	V
		V_{REF3}	11	VREF = 0 mA to − 1 mA	1.975	2.000	2.025	V
	Input stability	Line	11	V_{CC} = 2.5 V to 11 V	—	2*	—	mV
	Load stability	Load	11	VREF = 0 mA to − 1 mA	—	2*	—	mV
	Temperature stability	$\Delta V_{REF}/V_{REF}$	11	Ta = 0 °C to + 85 °C	—	0.20*	—	%
	Short-circuit output current	I_{OS}	11	VREF = 0 V	—	− 130*	—	mA
Under voltage lockout protection circuit block (CH1 to CH3) [UVLO1_3]	Threshold voltage	V_{TH}	34	VCC = ↗	1.7	1.8	1.9	V
	Hysteresis width	V_H	34	—	0.05	0.1	0.2	V
	Reset voltage	V_{RST}	34	VCC = ↘	1.55	1.7	1.85	V
Under voltage lockout protection circuit block (CH4, CH5) [UVLO4_5]	Threshold voltage	V_{TH}	30	VCC = ↗	1.35	1.5	1.65	V
	Hysteresis width	V_H	30	—	0.02	0.05	0.1	V
	Reset voltage	V_{RST}	30	VCC = ↘	1.27	1.45	1.63	V
Short-circuit detection block [SCP]	Threshold voltage	V_{TH}	15	—	0.65	0.70	0.75	V
	Input source current	I_{CSCP}	15	—	− 1.4	− 1.0	− 0.6	µA
Triangular wave oscillator block [OSC]	Oscillation frequency	f_{OSC1}	29 to 34	C_T = 100 pF, R_T = 6.8 kΩ	0.92	0.97	1.02	MHz
		f_{OSC2}	29 to 34	C_T = 100 pF, R_T = 6.8 kΩ V_{CC} = 2.5 V to 11 V	0.917	0.97	1.023	MHz
	Frequency input stability	$\Delta f_{OSC}/f_{OSC}$	29 to 34	C_T = 100 pF, R_T = 6.8 kΩ V_{CC} = 2.5 V to 11 V	—	1.0*	—	%
	Frequency temperature stability	$\Delta f_{OSC}/f_{OSC}$	29 to 34	C_T = 100 pF, R_T = 6.8 kΩ Ta = 0 °C to + 85 °C	—	1.0*	—	%
Soft-start block (CH1, CH2) [CS1, CS2]	Charge current	I_{CS}	1, 38	CS1, CS2 = 0 V	− 13	− 10	− 7	µA
Soft-start block (CH3 to CH5) [CS3 to CS5]	Charge current	I_{CS}	19, 20, 27	CS3 to CS5 = 0 V	− 1.3	− 1.0	− 0.7	µA

* : Standard design value

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(VCC = VCCO = 4 V, Ta = + 25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Error amp block (CH1) [Error Amp1]	Threshold voltage	V_{TH1}	37	V_{CC} = 2.5 V to 11 V Ta = + 25 °C	0.990	1.000	1.010	V
		V_{TH2}	37	V_{CC} = 2.5 V to 11 V Ta = 0 °C to + 85 °C	0.988	1.000	1.012	V
	Temperature stability	$\Delta V_{TH}/V_{TH}$	37	Ta = 0 °C to + 85 °C	—	0.1*	—	%
	Input bias current	I_B	37	− INE1 = 0 V	− 120	− 30	—	nA
	Voltage gain	A_V	36	DC	—	100*	—	dB
	Frequency bandwidth	BW	36	Av = 0 dB	—	1.4*	—	MHz
	Output voltage	V_{OH}	36	—	1.7	1.9	—	V
		V_{OL}	36	—	—	40	200	mV
	Output source current	I_{SOURCE}	36	FB1 = 0.65 V	—	− 2	− 1	mA
	Output sink current	I_{SINK}	36	FB1 = 0.65 V	150	200	—	µA
Error amp block (CH2 to CH5) [Error Amp2 to Error Amp5]	Threshold voltage	V_{TH1}	2, 18, 21, 26	V_{CC} = 2.5 V to 11 V Ta = + 25 °C	1.217	1.230	1.243	V
		V_{TH2}	2, 18, 21, 26	V_{CC} = 2.5 V to 11 V Ta = 0 °C to + 85 °C	1.215	1.230	1.245	V
	Temperature stability	$\Delta V_{TH}/V_{TH}$	2, 18, 21, 26	Ta = 0 °C to + 85 °C	—	0.1*	—	%
	Input bias current	I_B	2, 18, 21, 26	− INE2 to − INE5 = 0 V	− 120	− 30	—	nA
	Voltage gain	A_V	3, 17, 22, 25	DC	—	100*	—	dB
	Frequency bandwidth	BW	3, 17, 22, 25	A_V = 0 dB	—	1.4*	—	MHz
	Output voltage	V_{OH}	3, 17, 22, 25	—	1.7	1.9	—	V
		V_{OL}	3, 17, 22, 25	—	—	40	200	mV
	Output source current	I_{SOURCE}	3, 17, 22, 25	FB2 to FB5 = 0.65 V	—	− 2	− 1	mA
	Output sink current	I_{SINK}	3, 17, 22, 25	FB2 to FB5 = 0.65 V	150	200	—	µA

* : Standard design value

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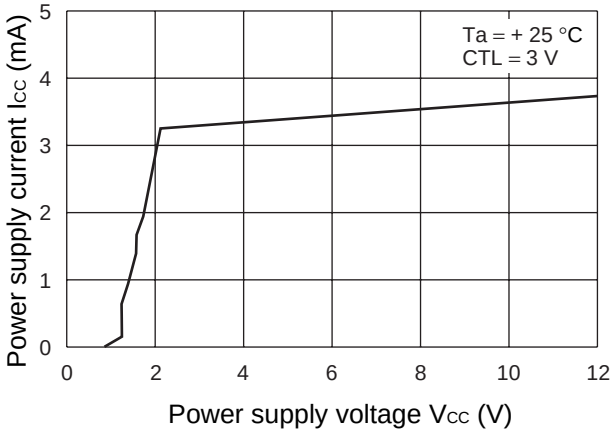
(VCC = VCCO = 4 V, Ta = + 25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
PWM comparator block (CH1) [PWM Comp.1]	Threshold voltage	V_{T0}	33, 34	Duty cycle = 0%	0.35	0.4	0.45	V
		V_{T100}	33, 34	Duty cycle = 100%	0.85	0.9	0.95	V
PWM comparator block (CH2 to CH5) [PWM Comp.2 to PWM Comp.5]	Threshold voltage	V_{T0}	29 to 32	Duty cycle = 0%	0.35	0.4	0.45	V
		V_{T100}	29 to 32	Duty cycle = 100%	0.85	0.9	0.95	V
	Maximum duty cycle	Dtr	29 to 32	C_T = 100 pF, R_T = 6.8 kΩ	85	90	95	%
Output block (CH1 to CH5) [Drive1 to Drive5]	Output source current	I_{SOURCE}	29 to 34	Duty ≤ 5% (t = 1/fosc × Duty) OUT = 0 V	—	– 130	– 75	mA
	Output sink current	I_{SINK}	29 to 34	Duty ≤ 5% (t = 1/fosc × Duty) OUT = 4 V	75	130	—	mA
	Output on resistor	R_{OH}	29 to 34	OUT = – 15 mA	—	18	27	Ω
		R_{OL}	29 to 34	OUT = 15 mA	—	18	27	Ω
	Dead time	t_{D1}	33, 34	OUT2 ↓ – OUT1 ↓	—	50*	—	ns
		t_{D2}	33, 34	OUT1 ↑ – OUT2 ↑	—	50*	—	ns
Short-circuit detection block [SCP Comp.]	Threshold voltage	V_{TH}	34	—	0.97	1.00	1.03	V
	Input bias current	I_B	10	– INS = 0 V	– 25	– 20	– 17	µA
Control block (CTL, CTL3 to CTL5) [CTL, CHCTL]	Output on condition	V_{IH}	6, 7 to 9	CTL, CTL3 to CTL5	1.5	—	11	V
	Output off condition	V_{IL}	6, 7 to 9	CTL, CTL3 to CTL5	0	—	0.5	V
	Input current	I_{CTLH}	6, 7 to 9	CTL, CTL3 to CTL5 = 3 V	5	30	60	µA
		I_{CTLL}	6, 7 to 9	CTL, CTL3 to CTL5 = 0 V	—	—	1	µA
General	Standby current	I_{CCS}	5	CTL, CTL3 to CTL5 = 0 V	—	0	2	µA
		I_{CCSO}	35	CTL = 0 V	—	0	1	µA
	Power supply current	I_{CC}	5	CTL = 3 V	—	4	6	mA

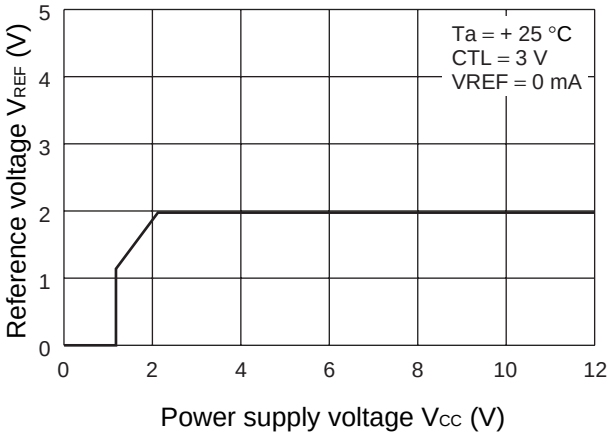
* : Standard design value

■ TYPICAL CHARACTERISTICS

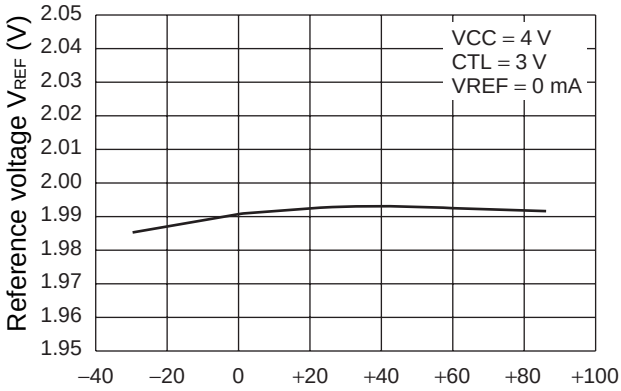
Power supply current vs. Power supply voltage



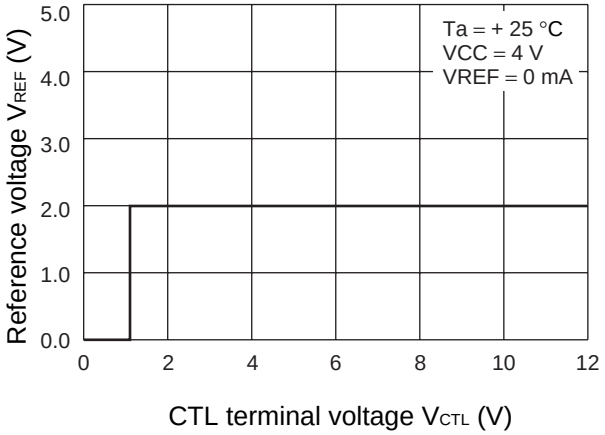
Reference voltage vs. Power supply voltage



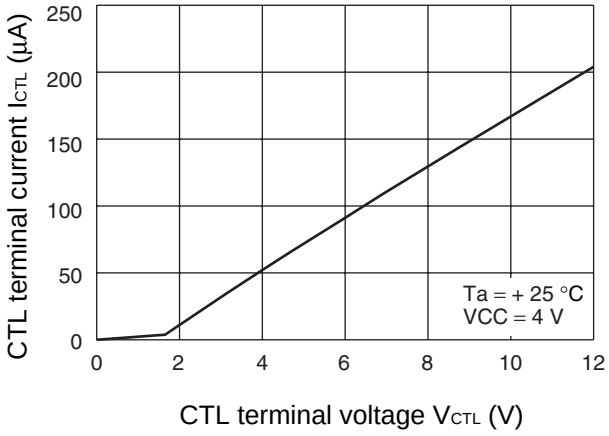
Reference voltage vs. Operating ambient temperature



Reference voltage vs. CTL terminal voltage



CTL terminal current vs. CTL terminal voltage



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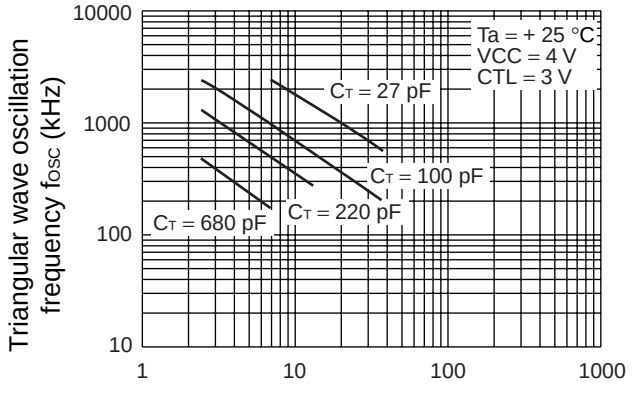
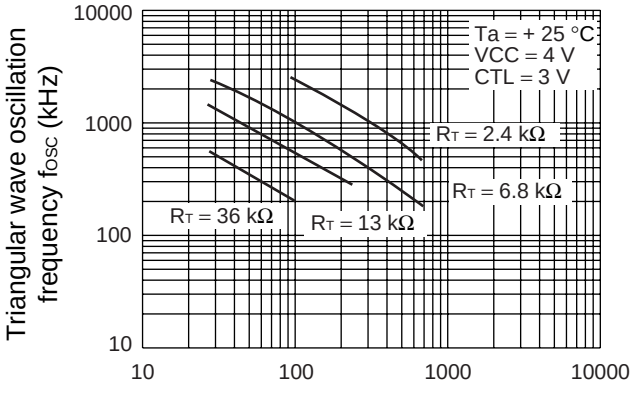
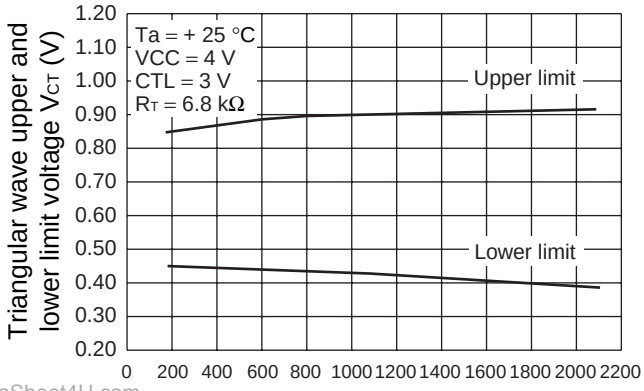
Triangular wave oscillation frequency vs. Timing resistor



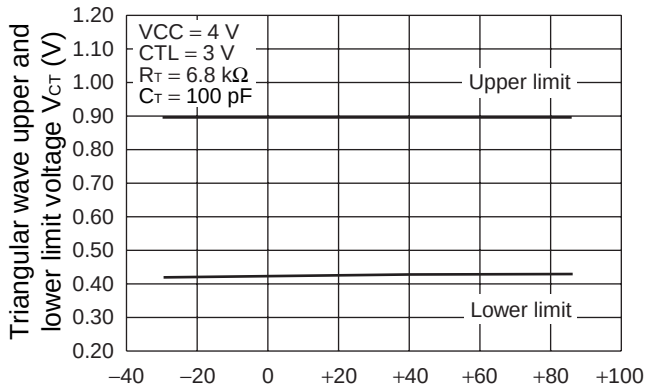
Triangular wave oscillation frequency vs. Timing capacitor



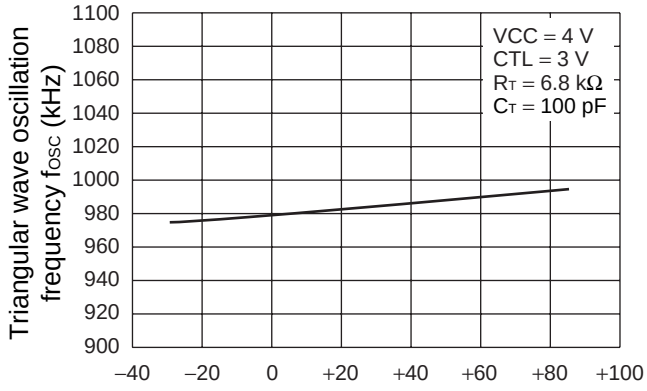
Triangular wave upper and lower limit voltage vs. Triangular wave oscillation frequency



Triangular wave upper and lower limit voltage vs. Operating ambient temperature



Triangular wave oscillation frequency vs. Operating ambient temperature



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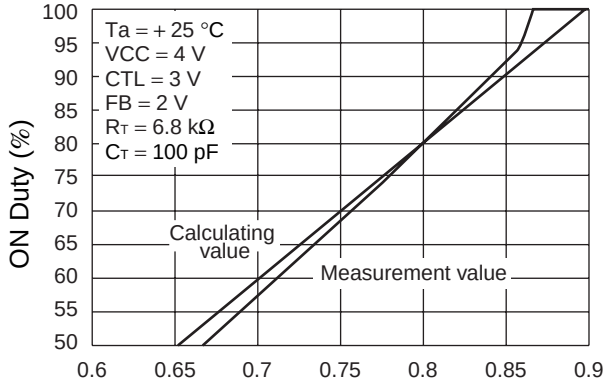
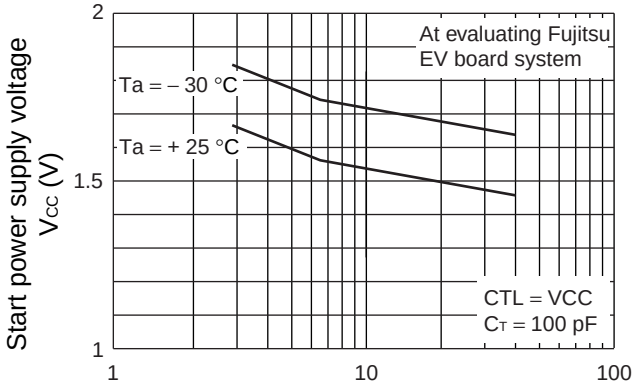
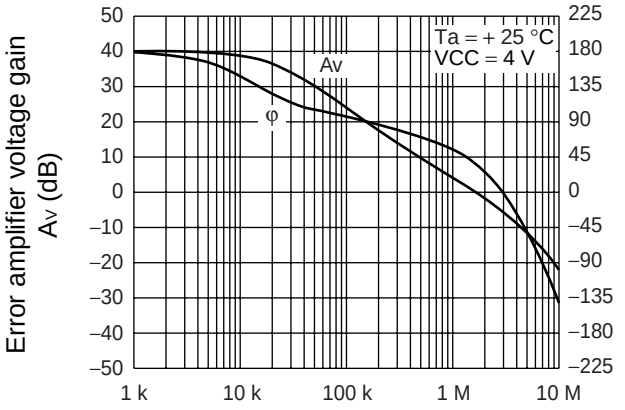
ON Duty vs. DTC terminal voltage

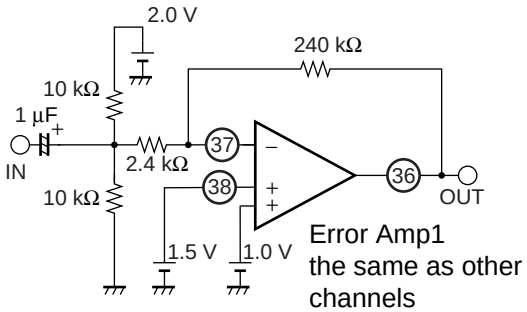


Start power supply voltage vs. Timing resistor

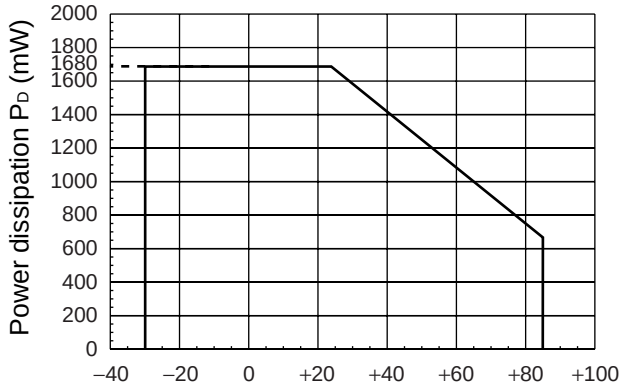


Error amplifier voltage gain and phase vs. Frequency

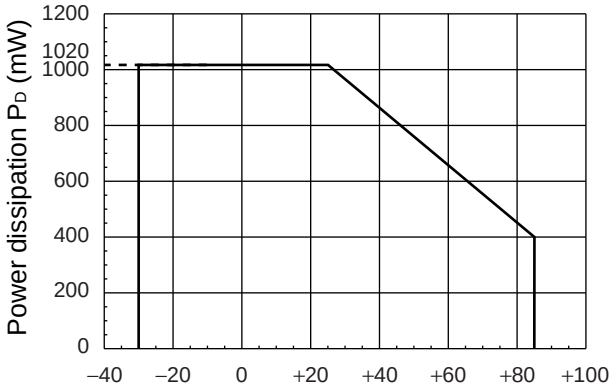




Power dissipation vs.
Operating ambient temperature (TSSOP-38P)



Power dissipation vs.
Operating ambient temperature (BCC-40P)



■ FUNCTIONAL DESCRIPTION

1. DC/DC Converter Function

(1) Reference voltage block (VREF)

The reference voltage circuit generates the reference voltage (2.0 V Typ) to which it makes amends for the temperature by the voltage supplied by the power supply terminal (pin 5). It is used as a reference in IC voltage.

It is also possible to supply the load current of up to 1 mA to external device as a output reference voltage through the VREF terminal (pin 11).

(2) Triangular wave oscillator block (OSC)

The triangular wave oscillator block generates the triangular wave oscillation waveforms of amplitude 0.4 V to 0.9 V by connecting the timing capacitor for and timing resistor to the CT terminal (pin 13) and RT terminal (pin 12) respectively.

The triangular wave is input to the PWM comparator in the IC.

(3) Error amplifier block (Error Amp1 to Error Amp5)

The error amplifier detects output voltage of DC/DC converter and outputs PWM control signals.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output terminal to inverted input terminal of the error amplifier, enabling stable phase compensation to the system.

The CS1 terminal (pin 38) to CS5 terminal (pin 27) that are non-inverted input terminal of error amplifier can prevent rush currents at power supply startup, by connecting a soft-start capacitor. The soft-start time is detected by the error amplifier, which provides a constant soft-start time independent of output load of DC/DC converter.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with CS1 terminal (pin 38) to CS5 terminal (pin 27) which are the non-inverted input terminal for Error Amp. The use of Error Amp for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load on the DC/DC converter.

(4) PWM comparator block (PWM Comp.1 to PWM Comp.5)

The PWM comparator block is a voltage-pulse width converter that controls the output duty depending on the input/output voltage.

When the error amplifier output voltage and DTC voltage remain higher than the triangular wave voltage, output transistor is turned on.

(5) Output block (Drive1 to Drive5)

The output block is in the totem-pole type, capable of driving an external P-ch MOS FET (CH1 main side, and CH2 and CH3) and N-ch MOS FET (CH1 synchronous rectification side, and CH4 and CH5).

2. Channel Control Function

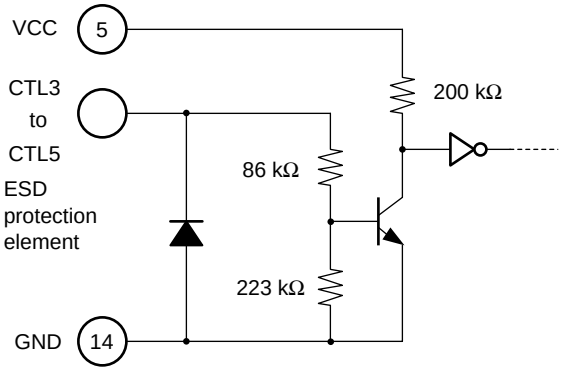
Main and each channel are set to ON/OFF by CTL terminal (pin 6) , CS1 terminal (pin 38) , CS2 terminal (pin 1) , CTL3 terminal (pin 7) , CTL4 terminal (pin 8) , and CTL5 terminal (pin 9) .

ON/OFF setting condition of each channel

CTL	CS1	CS2	CTL3	CTL4	CTL5	Power	CH1	CH2	CH3	CH4	CH5
L	X	X	X	X	X	OFF	Stops	Stops	Stops	Stops	Stops
H	GND	GND	L	L	L	ON	Stops	Stops	Stops	Stops	Stops
H	HiZ	GND	L	L	L	ON	Operation	Stops	Stops	Stops	Stops
H	GND	HiZ	L	L	L	ON	Stops	Operation	Stops	Stops	Stops
H	GND	GND	H	L	L	ON	Stops	Stops	Operation	Stops	Stops
H	GND	GND	L	H	L	ON	Stops	Stops	Stops	Operation	Stops
H	GND	GND	L	L	H	ON	Stops	Stops	Stops	Stops	Operation
H	HiZ	HiZ	H	H	H	ON	Operation	Operation	Operation	Operation	Operation

Note : Note that current over stand-by current flows into VCC terminal when the CTL terminal is in "L" level and one of terminals between CTL3 to CTL5 is set to "H" level (Refer to "• CTL3 to CTL5 terminal equivalent circuit").

• CTL3 to CTL5 terminal equivalent circuit



3. Protection Function

(1) Timer-latch short-circuit protection circuit (SCP, SCP Comp.)

The short-circuit detection comparator (SCP) detects the output voltage level of each channel, and if any channel output voltage becomes the short-circuit detection voltage or less, the timer circuits are actuated to start charging the external capacitor Cscp connected to the CSCP terminal (pin 15) .

When the capacitor (Cscp) voltage reaches about 0.7 V, the circuit is turned off the output transistor and sets the dead time to 100%.
In addition, the short-circuit detection from external input is capable by using –INS terminal (pin 10) on short-circuit detection comparator (SCP Comp.) .

To release the actuated protection circuit, either turn the power supply off and on again or set the CTL terminal (pin 6) to the “L” level to lower the VREF terminal (pin 11) voltage to 1.27 V (Min) or less (Refer to “■ SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT”) .

(2) Under voltage lockout protection circuit block (UVLO)

The transient state or a momentary decrease in the power supply voltage, which occurs when the power supply is turned on, may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, under voltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turned off the output transistor, and set the dead time to 100 % while holding the CSCP terminal (pin 15) at "L" level.

The circuit restores the output transistor to normal when the power supply voltage reaches the threshold voltage of the under-voltage lockout protection circuit.

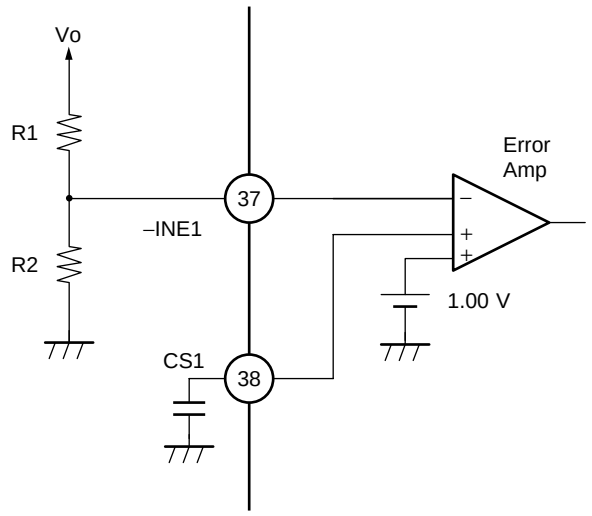
■ PROTECTION CIRCUIT OPERATING FUNCTION TABLE

This table refers to output condition when protection circuit is operating.

Operation circuit	OUT1-1	OUT1-2	OUT2	OUT3	OUT4	OUT5
Short-circuit protection circuit	H	L	H	H	L	L
Under voltage lockout protection circuit	H	L	H	H	L	L

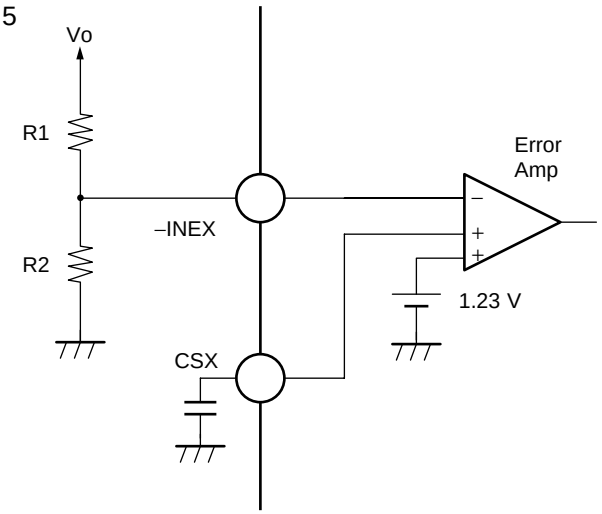
■ SETTING THE OUTPUT VOLTAGE

CH1



$$Vo = \frac{1.00\ V}{R2} (R1 + R2)$$

CH2 to CH5



$$Vo = \frac{1.23\ V}{R2} (R1 + R2)$$

X : Each channel No.

■ SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY

The triangular wave oscillation frequency can be set by the timing resistor (R_T) connected to the RT terminal (pin 12) and the timing capacitor (C_T) connected to the CT terminal (pin 13).

Triangular wave oscillation frequency : fosc

$$fosc\ (kHz) \fallingdotseq \frac{659600}{C_T\ (pF) \times R_T\ (k\Omega)}$$

■ SETTING THE SOFT-START TIME

To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors (C_{S1} to C_{S5}) to the CS1 terminal (pin 38) to CS5 terminal (pin 27) respectively.

As shown in the figure below, changing $\overline{CTLX}$ from “H” to “L” in the CH1 and CH2 circuits causes the external soft-start capacitors (C_{S1} and C_{S2}) connected to CS1 and CS2 terminals to start charging with a current approximately 10 μA.

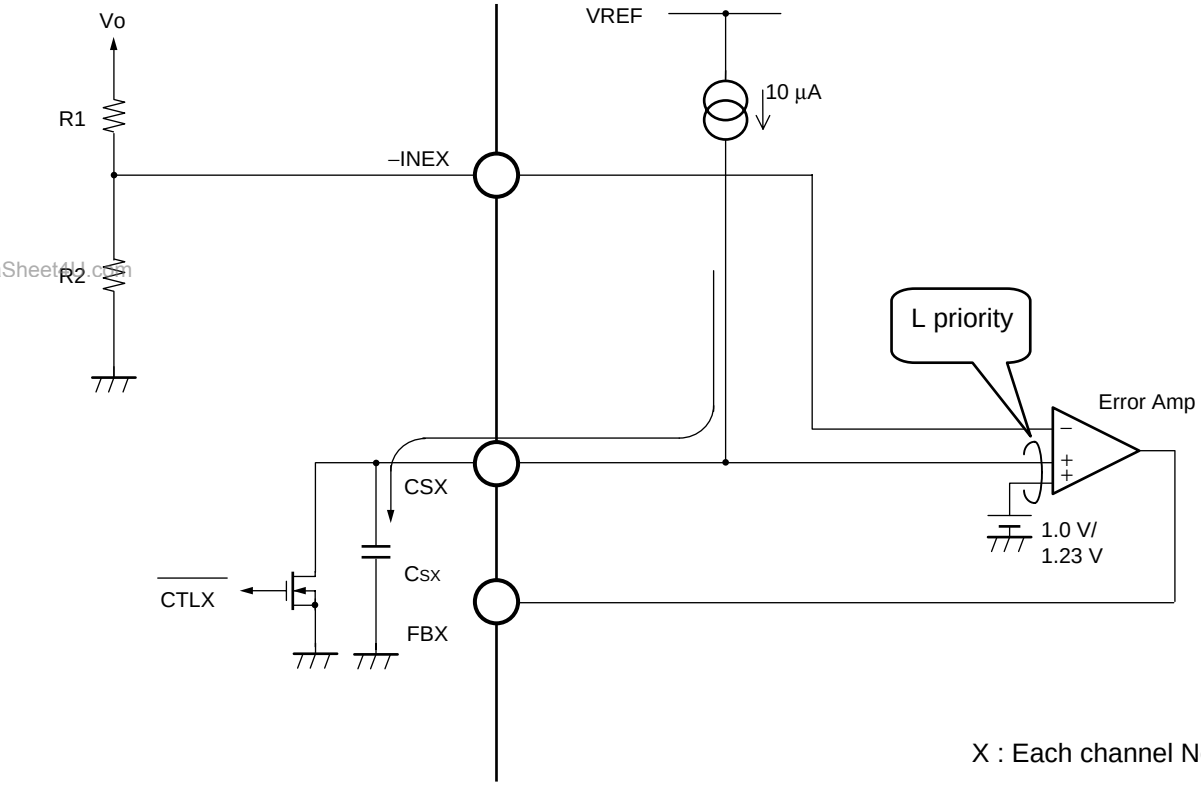
As shown in the figure on the next page, changing CTLX from “L” to “H” in the CH3 to CH5 circuits causes the external soft-start capacitors connected to CS3 to CS5 terminals to start charging with a current of approximately 1 μA.

The error amplifier output (FB1 to FB5) is determined by comparison between the lower voltage of the two non-inverted input terminal voltage (1.23 V (CH : 1.0 V), CS terminal voltages) and the inverted input terminal voltage (– INE1 to – INE5). The FB terminal voltage is decided for the soft-start period (CS terminal voltage < 1.23 V (CH1 : 1.0 V)) by the comparison between – INE terminal voltage and CS terminal voltage. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor externally connected to the CS terminal is charged. The soft-start time is obtained from the following formula :

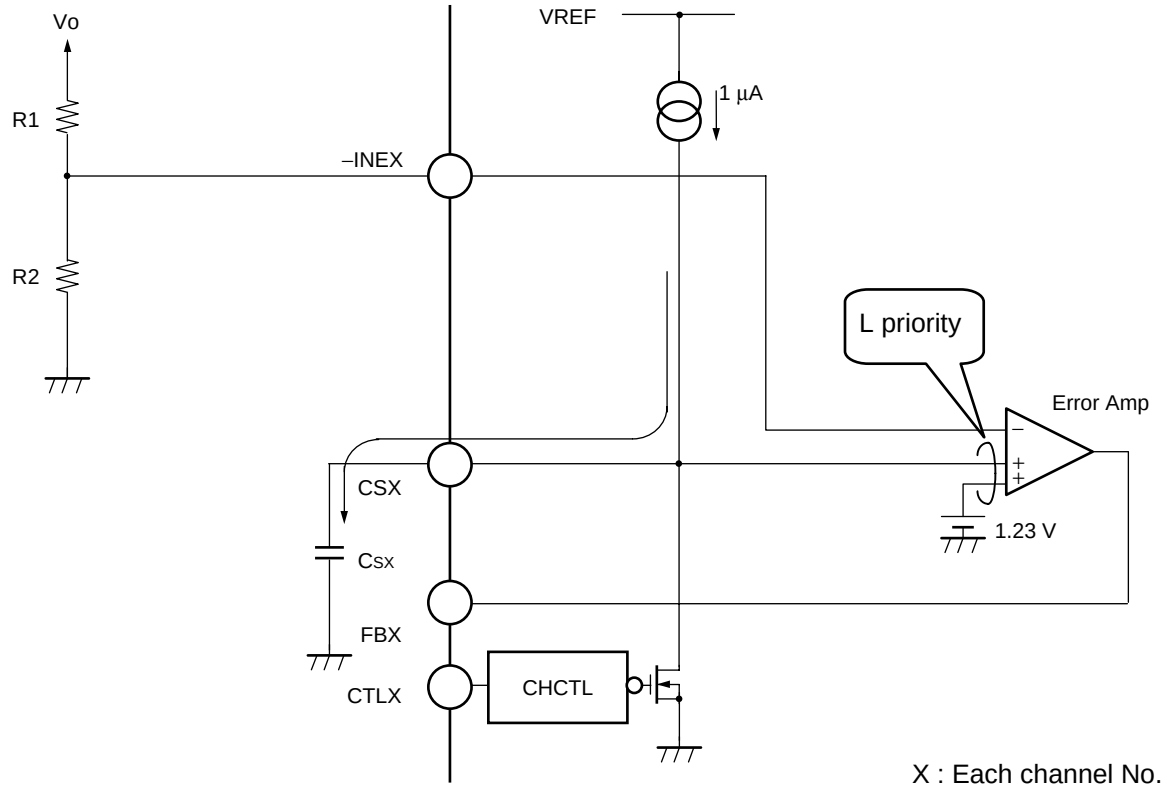
Soft-start time : ts(time to output 100%)

CH1 : ts (s) ≒ 0.100 × C_{SX} (μF)
CH2 : ts (s) ≒ 0.123 × C_{SX} (μF)
CH3 to CH5 : ts (s) ≒ 1.23 × C_{SX} (μF)

• Soft-start circuit (CH1, CH2)



- Soft-start circuit (CH3 to CH5)

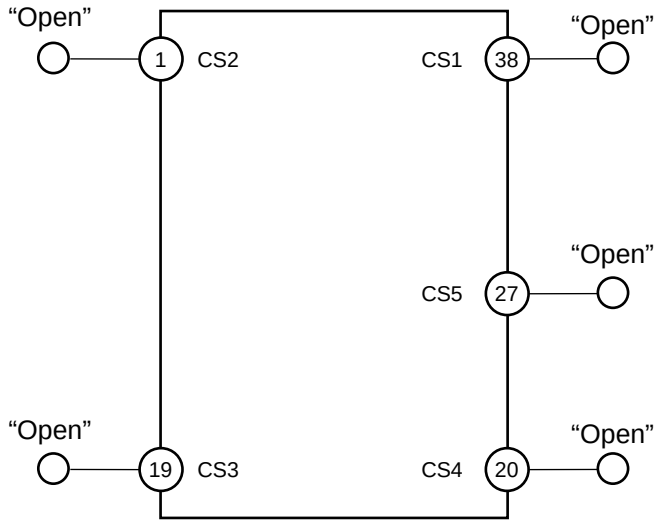


X : Each channel No.

■ PROCESSING WHEN NOT USING CS TERMINAL

When soft-start function is not used, leave the CS1 terminal (pin 38), CS2 terminal (pin 1), CS3 terminal (pin 19), CS4 terminal (pin 20), and CS5 terminal (pin 27) open.

- When not setting soft-start time



■ SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

Each channel uses the short-circuit detection comparator (SCP Comp.) to always compare the error amplifier's output level to the reference voltage.

While DC/DC converter load conditions are stable on all channels, the short-circuit detection comparator output remains at "L" level, and the CSCP terminal (pin 15) is held at "L" level.

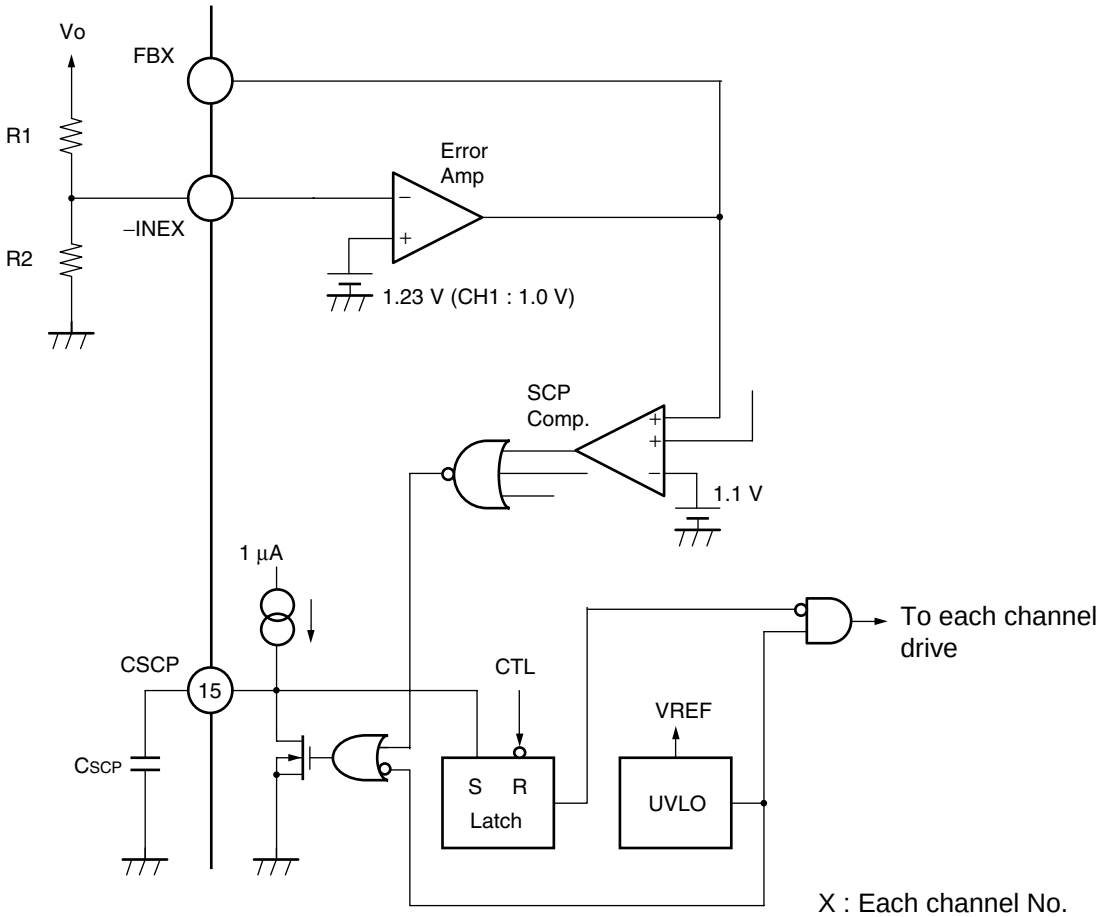
If the load condition on a channel changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the output of the short-circuit detection comparator on that channel goes to "H" level. This causes the external short-circuit protection capacitor Cscp connected to the CSCP terminal to be charged at 1 μA.

Short-circuit detection time : tcscp

$$tcscp\ (s) \fallingdotseq 0.70 \times Cscp\ (\mu F)$$

When the capacitor Cscp is charged to the threshold voltage ($V_{TH} \fallingdotseq 0.7V$), the latch is set to and the external FET is turned off (dead time is set to 100%). At this time, the latch input is closed and CSCP terminal (pin 15) is held at "L" level.
In addition, the short-circuit detection from external input is capable by using –INS terminal (pin 10) on the short-circuit detection comparator (SCP Comp.) . The short-circuit detection operation starts when –INS terminal voltage is less than threshold voltage ($V_{TH} \fallingdotseq 1$ V) .
When the power supply is turn off and on again or VREF terminal (pin 11) voltage is less than 1.27 V (Min) by setting CTL terminal (pin 6) to “L” level, the latch is released.

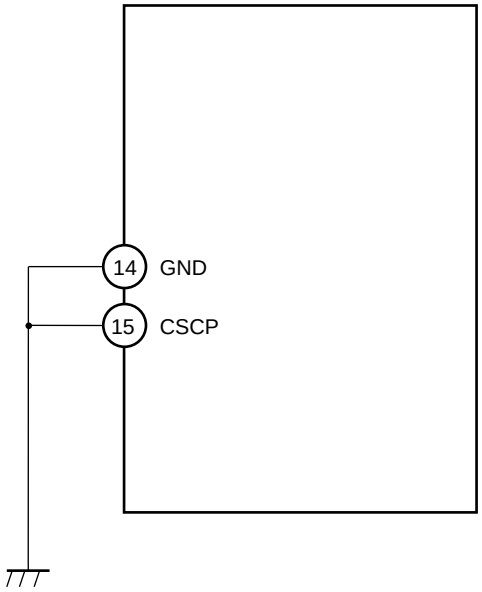
- Timer-latch short-circuit protection circuit



■ PROCESSING WHEN NOT USING CSCP TERMINAL

When not using the timer-latch short-circuit protection circuit, connect the CSCP terminal (pin 15) to GND with the shortest distance.

- When not using CSCP terminal



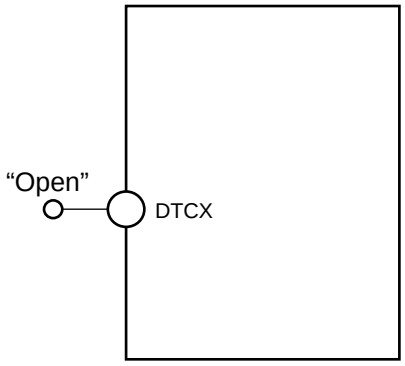
■ SETTING THE DEAD TIME

When the device is set for step-up or inverted output based on the step-up, step-up/down Zeta conversion, step-up/down Sepic conversion, or flyback conversion, the FB terminal voltage may reach and exceed the triangular wave voltage due to load fluctuation. If this is the case, the output transistor is fixed to a full-ON state (ON duty = 100 %). To prevent this, set the maximum duty of the output transistor.

When the DTC terminal is opened, the maximum duty is 90% (Typ) because of this IC built-in resistance which sets the DTC terminal voltage.

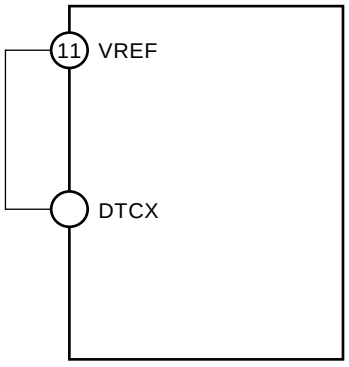
When the DTC terminal is not used, connect it directly to the VREF terminal (pin 11) as shown below (when no dead time is set).

• When dead time is set
(Setting by built-in resistance ≒ 90%)



X : Each channel No.

• When no dead time is set



X : Each channel No.

Set the DTC terminal voltage by resistance divider from VREF terminal voltage when you change the maximum duty by external resistance (Refer to "• When dead time is set (Setting by external resistance)").

When the DTC terminal voltage is higher than the triangular wave voltage, the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude : = 0.5 V and triangular wave lower voltage : = 0.4 V is given below.

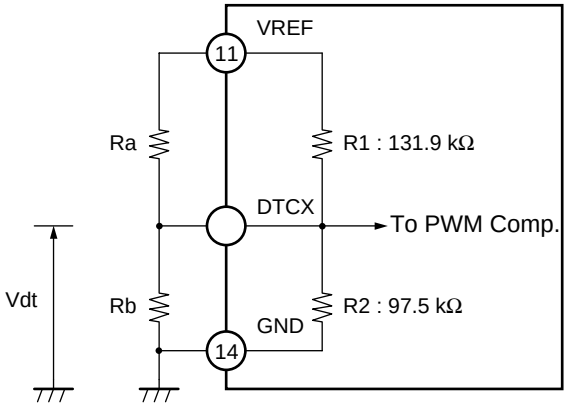
It is possible to set DTC terminal voltage (dead time) by disregarding built-in resistance (include the tolerance) by adjusting external resistance to 1/10 or less of built-in resistance. Set to become 1mA or less in total of each channel the load current of VREF terminal.

$$\text{DUTY (ON) Max} \fallingdotseq \frac{\text{Vdt} - 0.4\ \text{V}}{0.5\ \text{V}} \times 100\ (\%)^{*}$$

$$\text{Vdt} = \frac{\text{Rb}}{\text{Ra} + \text{Rb}} \times \text{VREF (condition : Ra} < \frac{\text{R1}}{10}\text{, Rb} < \frac{\text{R2}}{10}\text{)}$$

* : DUTY obtained by the above-mentioned formula is a calculated value. For setting, refer to "ON Duty vs. DTC terminal voltage" in ■ TYPICAL CHARACTERISTICS.

- When dead time is set
  (Setting by external resistance)



X : Each channel No.

Example setting : For an aim Max duty (ON) of 80% (Vdt = 0.8 V) with Ra = 13.7 kΩ and Rb = 9.1 kΩ

- Calculation using external resistors Ra and Rb only

$$Vdt = \frac{Rb}{Ra + Rb} \times VREF \fallingdotseq 0.80\ V$$

$$DUTY\ (ON)\ Max \fallingdotseq \frac{Vdt - 0.4\ V}{0.5\ V} \times 100\ (\%) \fallingdotseq 80\%^{*} \cdots [1]$$

- Calculation considering internal resistor (tolerance ± 20%) also

$$Vdt = \frac{(Rb\ \text{and}\ R2\ \text{combined resistance})}{(Ra\ \text{and}\ R1\ \text{combined resistance}) + (Rb\ \text{and}\ R2\ \text{combined resistance})} \times VREF \fallingdotseq 0.80\ V \pm 0.13\%$$

$$DUTY\ (ON)\ Max \fallingdotseq \frac{Vdt - 0.4\ V}{0.5\ V} \times 100\ (\%) \fallingdotseq 80\% \pm 0.2\%^{*} \cdots [2]$$

* : Based on [1] and [2] above, selecting external resistances of 1/10th or less of the built-in resistance enables the built-in resistance to be ignored.
As for the duty difference, please expect ± 5% (at f_{OSC} = 1 MHz) . It is because of being with the difference of a triangular wave amplitude.

■ OPERATION EXPLANATION WHEN CTL TURNING ON AND OFF

When CTL is turned on, internal reference voltage VR and VREF generate. When VREF exceeds each threshold voltage (VTH1,VTH2) of UVLO1 and UVLO2 (under voltage lockout protection circuit), UVLO1 and UVLO2 are released, and the operation of output drive circuit of each channel becomes possible.

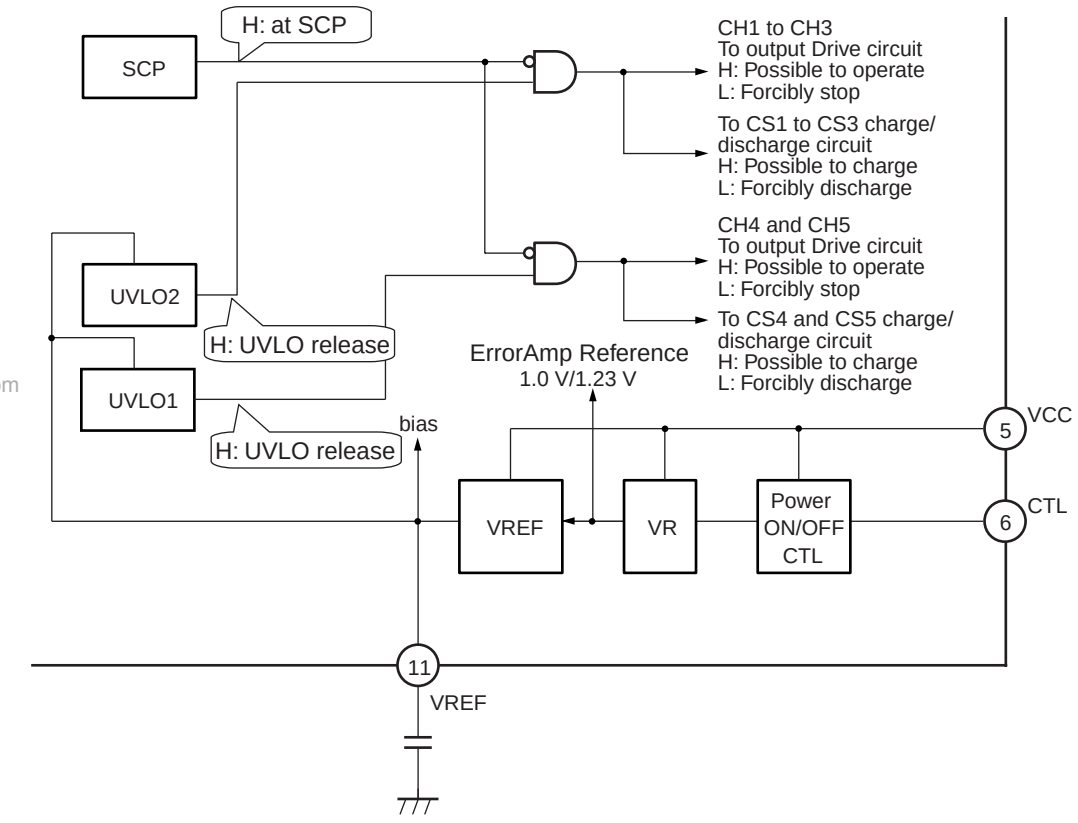
When CTL is off, VR and VREF fall. When VREF decreases and UVLO1 and UVLO2 fall below each reset voltage (VRST1,VRST2), UVLO operates and output Drive circuit of each channel is forcibly done the operation stop, and makes the output off state.

When period to reaching to 2.0 V by VREF voltage after UVLO1 and UVLO2 are released by turning on CTL (refer to a and b in "• Timing chart") and VREF decreases from 2.0 V after turning off CTL and the period until do the operation of UVLO1 and UVLO2(refer to a' and b' in "• Timing chart"), the bias voltage and the bias current in IC do not reach a prescribed value because VREF which is the reference voltage does not reach 2.0 V, and the speed of response for IC has decreased.

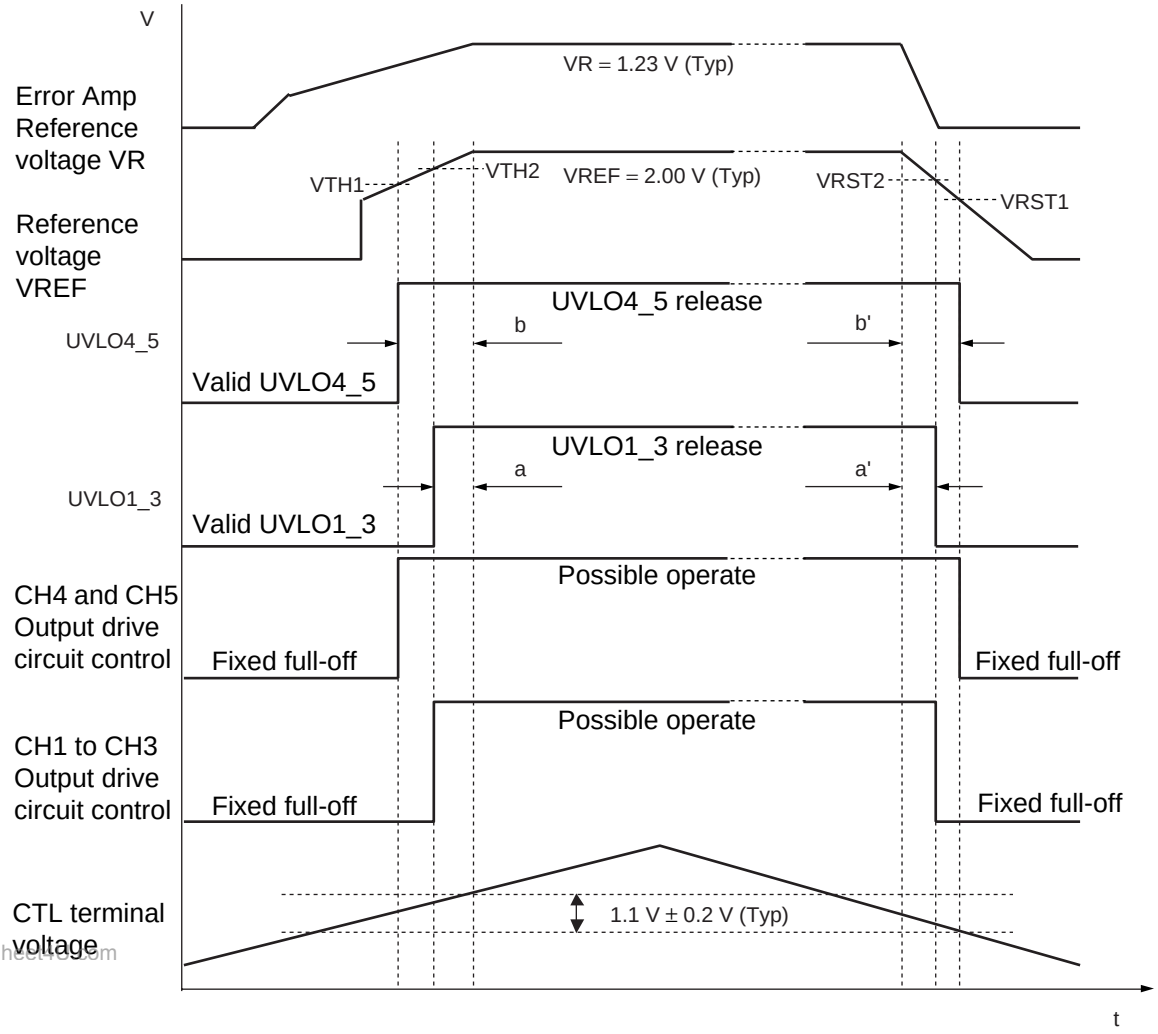
Moreover, when it does the turning on and off of the input sudden change, the load sudden change, and CTL3 to CTL5 in this period, IC cannot conform and the output might overshoot.

Therefore, impress the voltage to CTL terminal by which the VREF terminal voltage never stays in the above-mentioned period.

• CTL block equivalent circuit



• Timing chart



■ ABOUT THE LOW VOLTAGE OPERATION

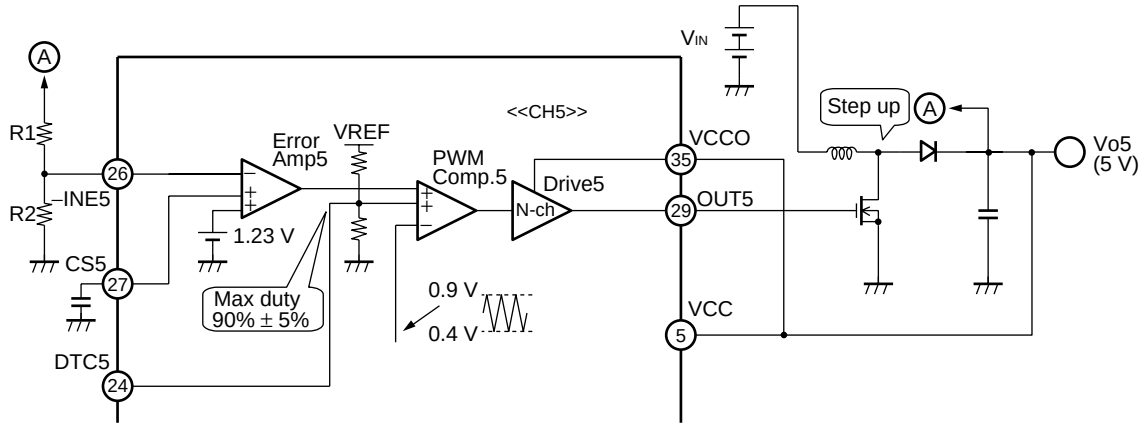
1.7 V or more is necessary for the VCC terminal and the VCCO terminal for the self-power supply type to use the step-up circuit as the start voltage.

Even if V_{IN} decreases up to 1.5 V afterwards, it is possible to operate if the VCC terminal voltage and the VCCO terminal voltage rise to 2.5 V or more after start-up.

However, it is necessary not to exceed the maximum duty set value by the duty due to the V_{IN} decrease.

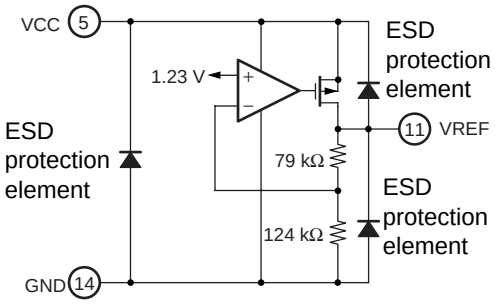
Include other channels, and confirm an enough operation margin when using it.

- Example of self-power supply method circuit

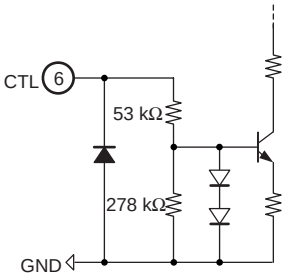


■ I/O EQUIVALENT CIRCUIT

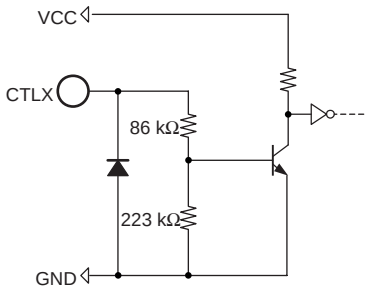
• Reference voltage block



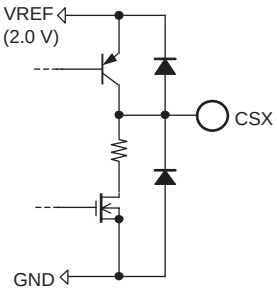
• Control block



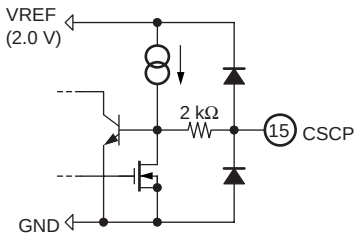
• Channel control block (CH3 to to CH5)



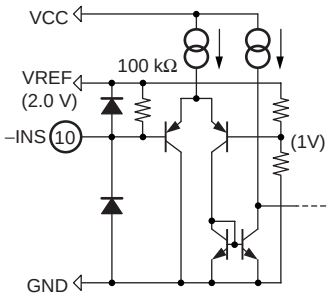
• Soft-start block



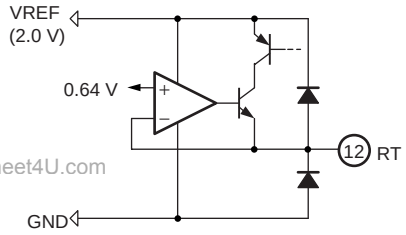
• Short-circuit detection block



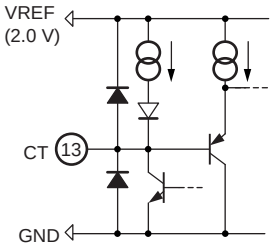
• Short-circuit detection comparator block



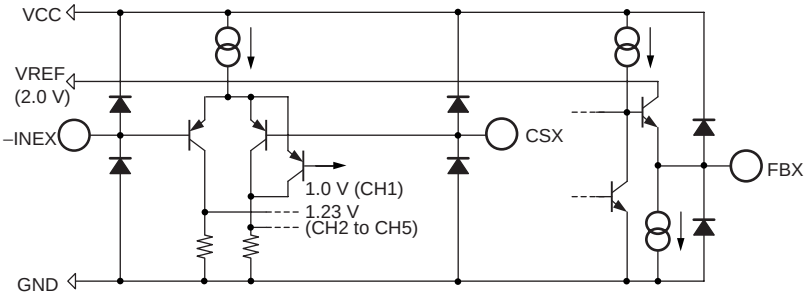
• Triangular wave oscillator block (RT)



• Triangular wave oscillator block (CT)



• Error amplifier block (CH1 to CH5)

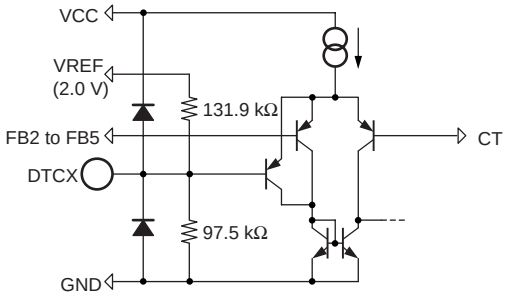


X : Each channel No.

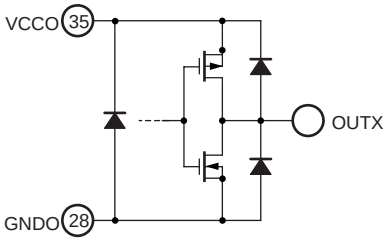
(Continued)

(Continued)

• PMW comparator block

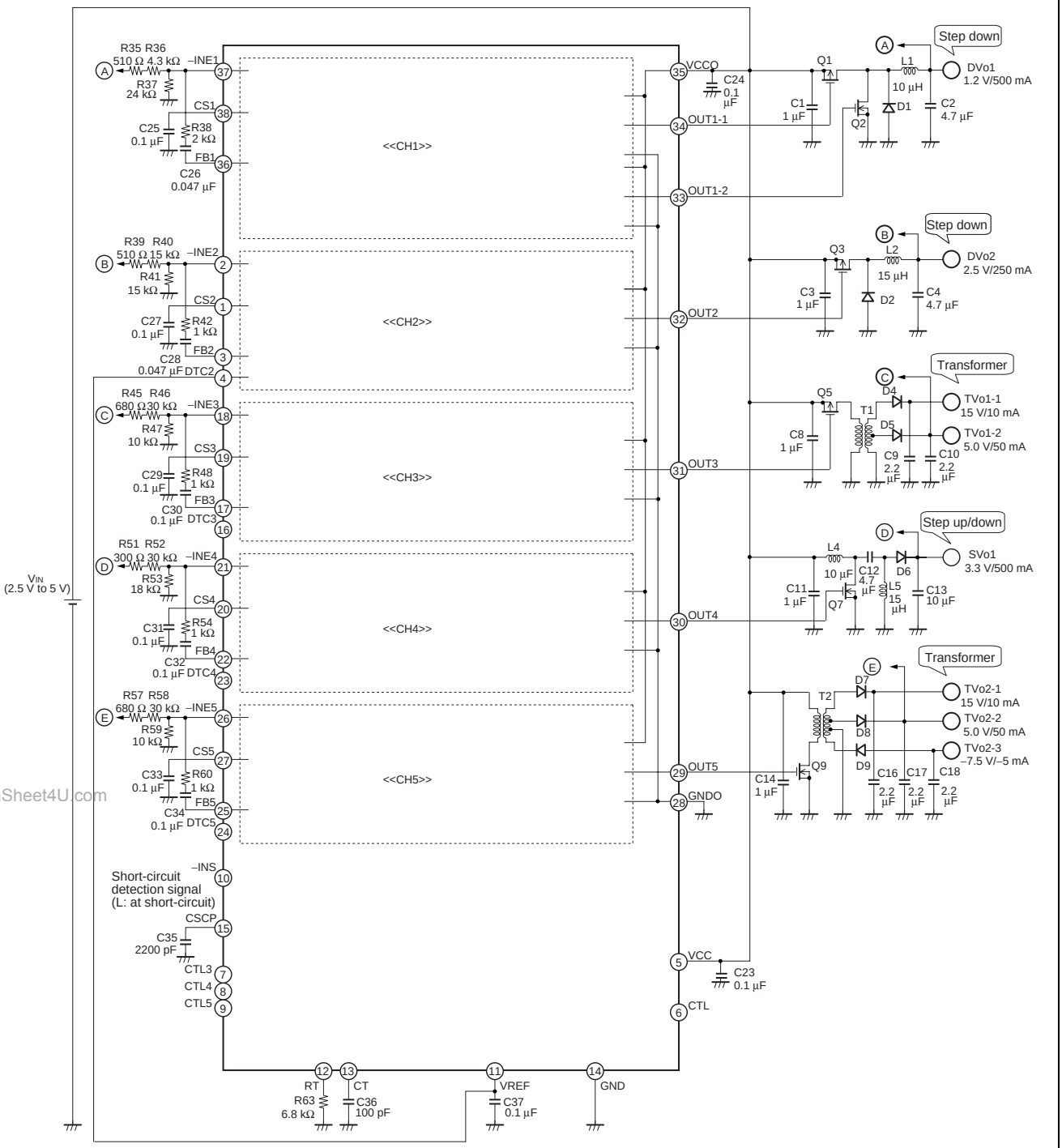


• Output block (CH1 to CH5)



X : Each channel No.

■ APPLICATION EXAMPLE



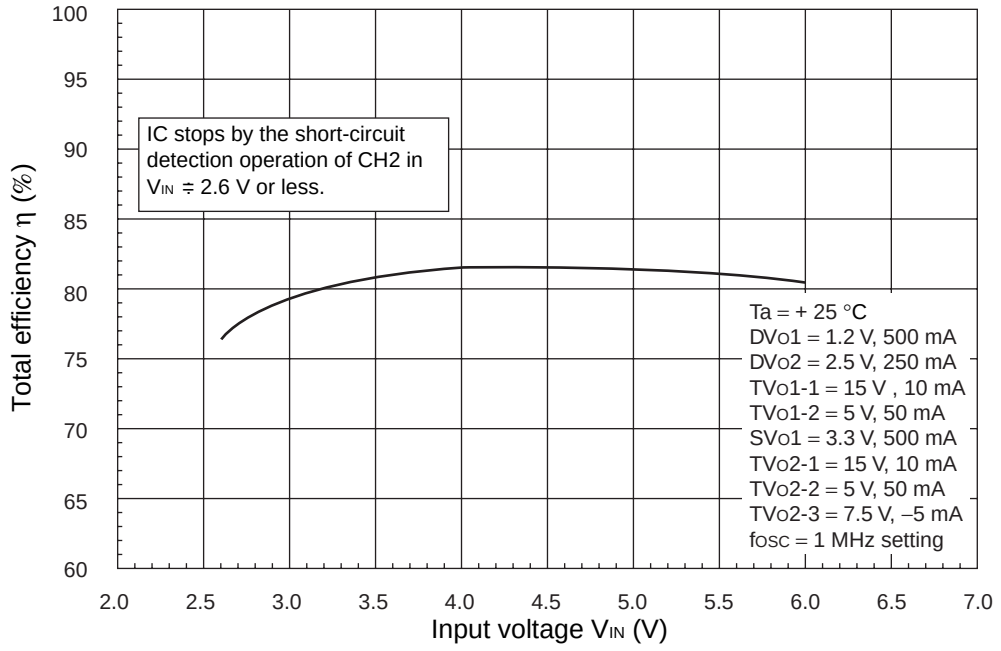
■ PARTS LIST

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q3	P-ch FET	VDS = − 12 V, ID = − 1.5 A		SANYO	MCH3317
Q2, Q7, Q9	N-ch FET	VDS = 20 V, ID = 1.8 A		SANYO	MCH3405
Q5	P-ch FET	VDS = − 20 V, ID = − 2 A		SANYO	MCH3306
D1, D2, D6	Diode	VF = 0.4 V (Max), at IF = 1 A		SANYO	SBS004
D4, D5, D7 to D9	Diode	VF = 0.55 V (Max), at IF = 0.5 A		SANYO	SB05-05CP
L1, L4	Inductor	10 µH	0.94 A, 56 mΩ	TDK	RLF5018T-100MR94
L2, L5	Inductor	15 µH	0.76 A, 97 mΩ	TDK	RLF5018T-150MR76
T1, T2	Transformer	—	—	SUMIDA	CLQ52 5388-T138
C1, C3	Ceramics Condenser	1 µF	25 V	TDK	C3216JB1E105K
C2, C4, C12	Ceramics Condenser	4.7 µF	16 V	TDK	C3216JB1C475K
C8, C11	Ceramics Condenser	1 µF	25 V	TDK	C3216JB1E105K
C9, C10	Ceramics Condenser	2.2 µF	25 V	TDK	C3216JB1E225K
C13	Ceramics Condenser	10 µF	6.3 V	TDK	C3216JB0J106K
C14	Ceramics Condenser	1 µF	25 V	TDK	C3216JB1E105K
C16 to C18	Ceramics Condenser	2.2 µF	25 V	TDK	C3216JB1E225K
C23 to C25, C27	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C26, C28	Ceramics Condenser	0.047 µF	50 V	TDK	C1608JB1H473K
C29 to C34	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C35	Ceramics Condenser	2200 pF	50 V	TDK	C1608JB1H222K
C36	Ceramics Condenser	100 pF	50 V	TDK	C1608CH1H101J
C37	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
R35, R39	Resistor	510 Ω	0.5%	ssm	RR0816P-511-D
R36	Resistor	4.3 kΩ	0.5%	ssm	RR0816P-432-D
R37	Resistor	24 kΩ	0.5%	ssm	RR0816P-243-D
R38	Resistor	2 kΩ	0.5%	ssm	RR0816P-202-D
R40, R41	Resistor	15 kΩ	0.5%	ssm	RR0816P-153-D
R42, R48, R54	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D
R45, R57	Resistor	680 Ω	0.5%	ssm	RR0816P-681-D
R46, R52, R58	Resistor	30 kΩ	0.5%	ssm	RR0816P-303-D
R47, R59	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R51	Resistor	300 Ω	0.5%	ssm	RR0816P-301-D
R53	Resistor	18 kΩ	0.5%	ssm	RR0816P-183-D
R60	Resistor	1 kΩ	0.5%	ssm	RR0816P-102-D
R63	Resistor	6.8 kΩ	0.5%	ssm	RR0816P-682-D

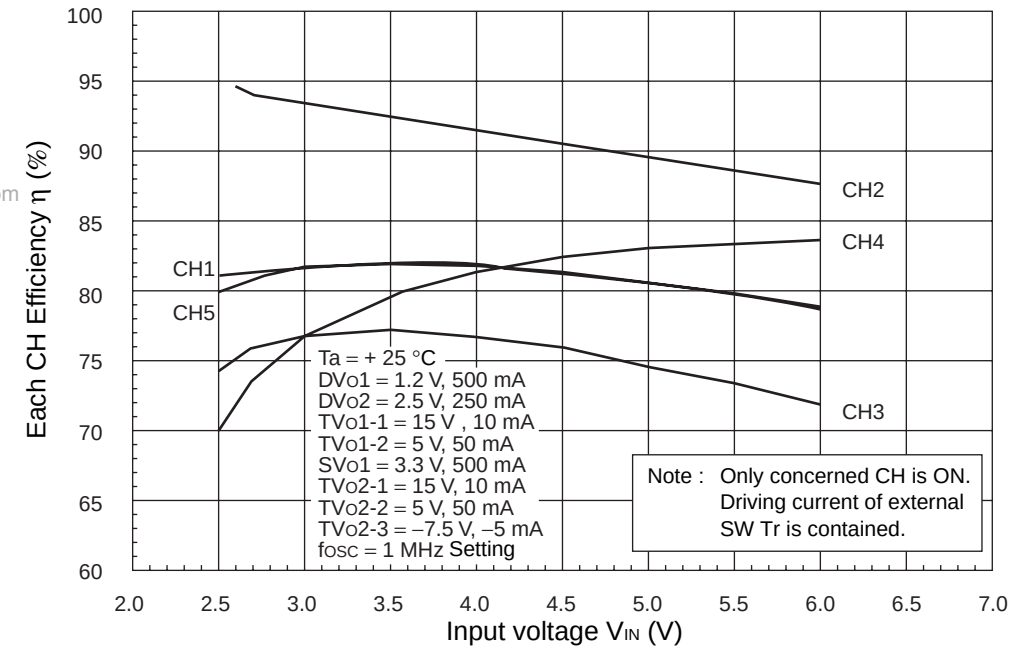
Note : SANYO : SANYO Electric Co., Ltd.
TDK : TDK Corporation
SUMIDA : Sumida Corporation
ssm : SUSUMU CO., LTD.

■ REFERENCE DATA

Total efficiency vs. Input voltage

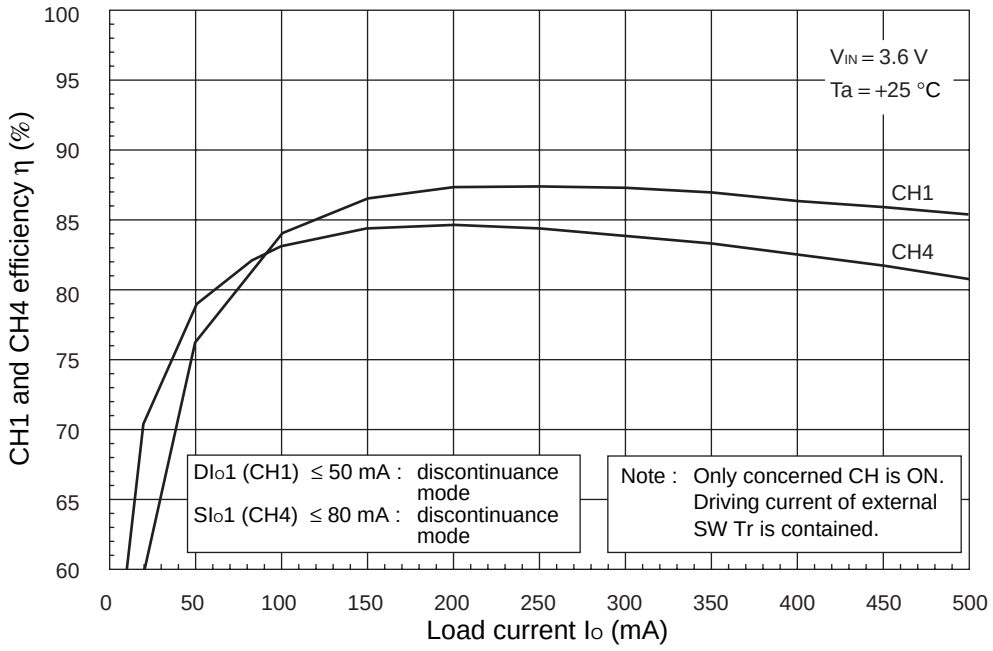


Each CH efficiency vs. Input voltage

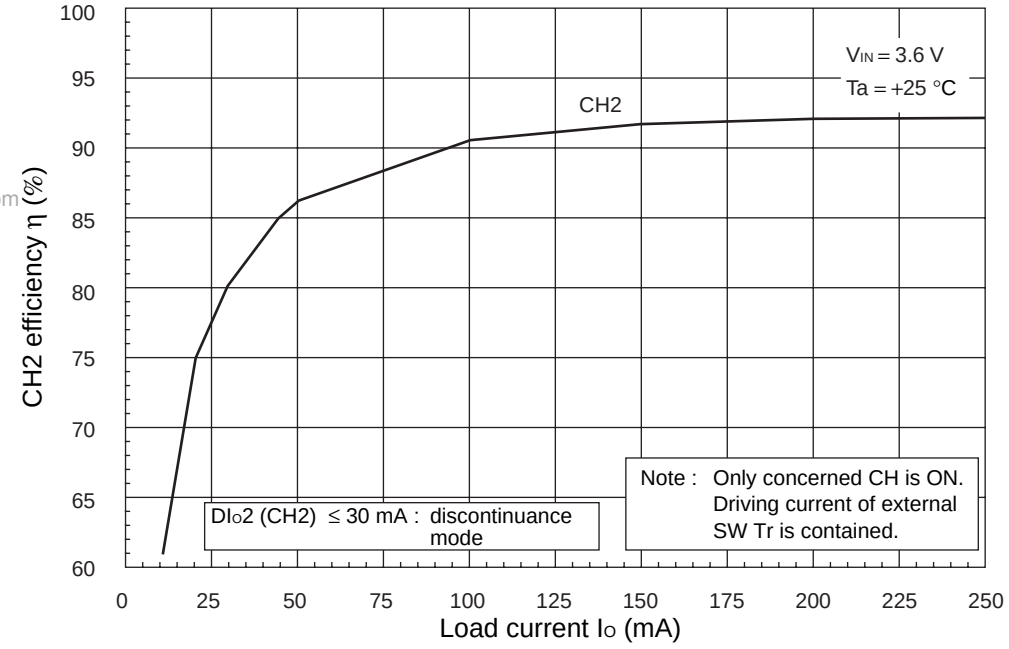


(Continued)

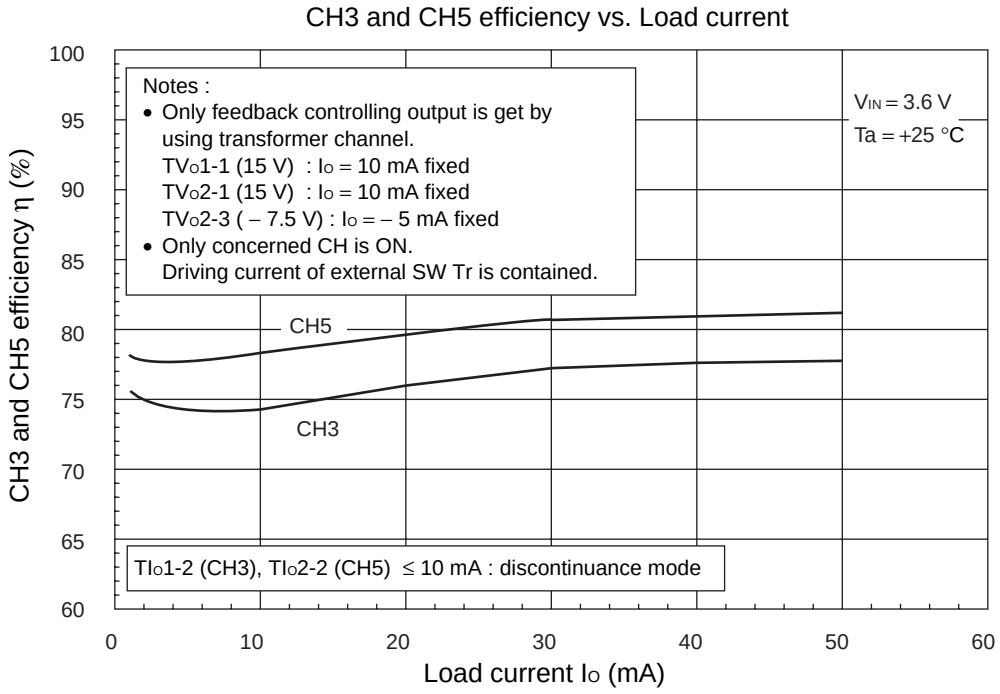
CH1 and CH4 efficiency vs. Load current



CH2 efficiency vs. Load current



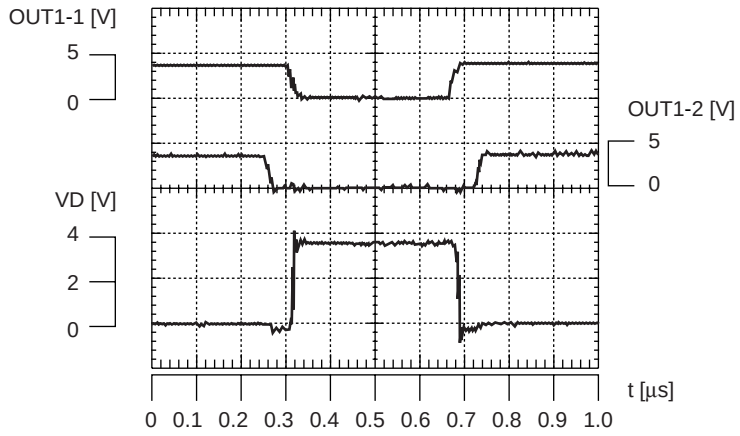
(Continued)



(Continued)

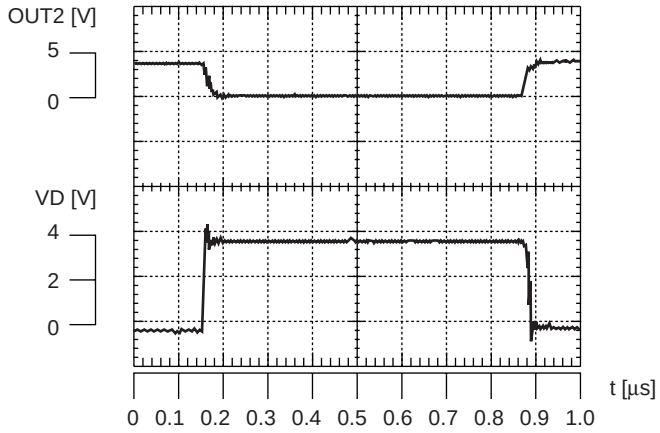
Switching waveform (CH1)

Ta = +25 °C
V_{IN} = 3.6 V
DVo1 = 1.2 V
Io1 = 500 mA



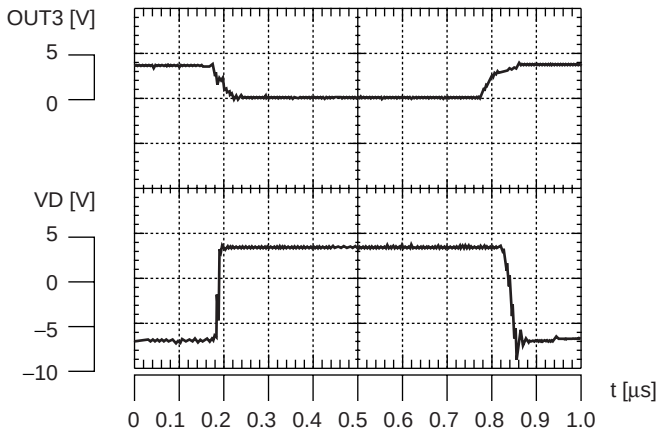
Switching waveform (CH2)

Ta = +25 °C
V_{IN} = 3.6 V
DVo2 = 2.5 V
Io2 = 250 mA



Switching waveform (CH3)

Ta = +25 °C
V_{IN} = 3.6 V
TVo1-1 = 15 V
Tlo1-1 = 10 mA
TVo1-2 = 5 V
TVo3 = 50 mA

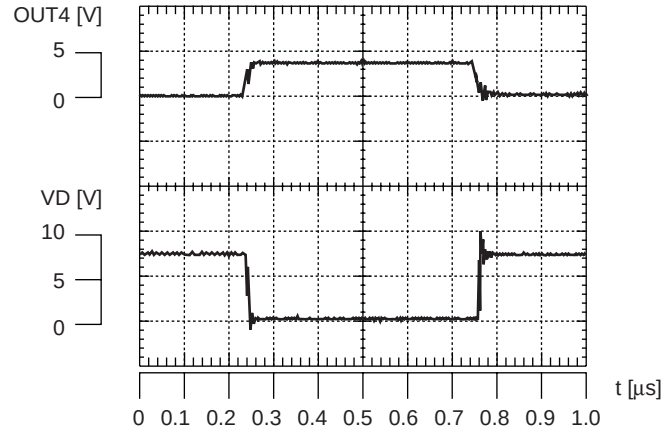


(Continued)

(Continued)

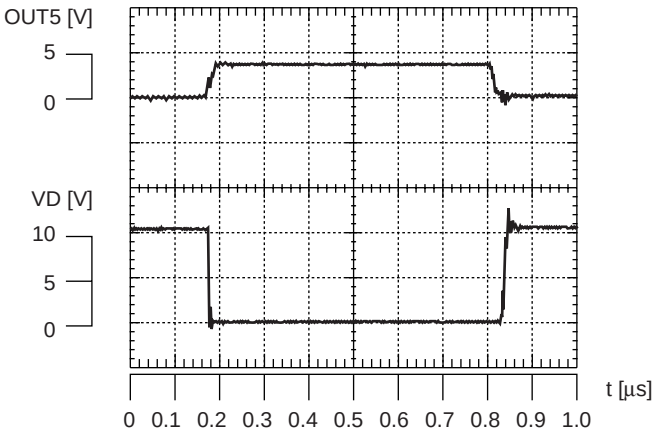
Switching waveform (CH4)

Ta = +25 °C
V_{IN} = 3.6 V
SVo1 = 3.3 V
Slo1 = 500 mA



Switching waveform (CH5)

Ta = +25 °C
V_{IN} = 3.6 V
TVo2-1 = 15 V
Tlo2-1 = 10 mA
TVo2-2 = 5 V
Tlo2-2 = 50 mA
TVo2-3 = –7.5 V
Tlo2-3 = –5 mA



■ USAGE PRECAUTIONS

- Printed circuit board ground lines should be set up with consideration for common impedance.

- Take appropriate static electricity measures.
  - Containers for semiconductor materials should have anti-static protection or be made of conductive material.
  - After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
  - Work platforms, tools, and instruments should be properly grounded.
  - Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

- Do not apply negative voltages.
  - The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause malfunction.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A108PFT-❑❑❑E1	38-pin plastic TSSOP (FPT-38P-M03)	Lead Free version
MB39A108PV2-❑❑❑E1	40-pin plastic BCC (LCC-40P-M07)	Lead Free version

■ EV BOARD ORDERING INFORMATION

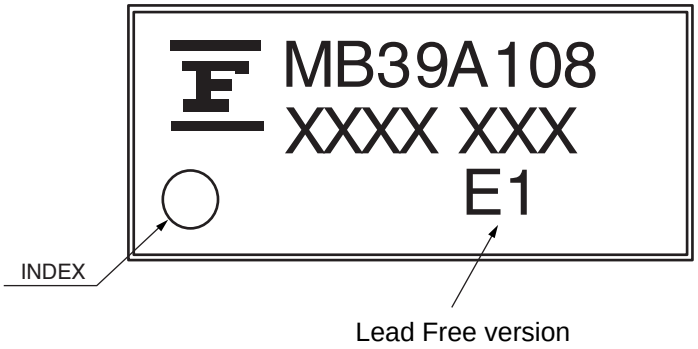
EV board part No.	EV board version No.	Remarks
MB39A108EVB-01	Board Rev. 1.0	TSSOP-38P

■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

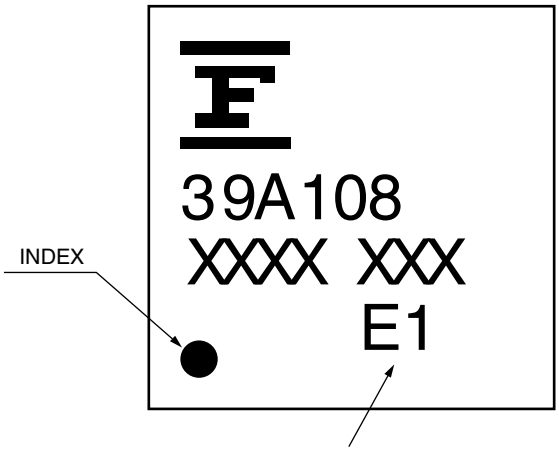
The LSI products of Fujitsu with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

The product that conforms to this standard is added “E1” at the end of the part number.

■ MARKING FORMAT (LEAD FREE VERSION)

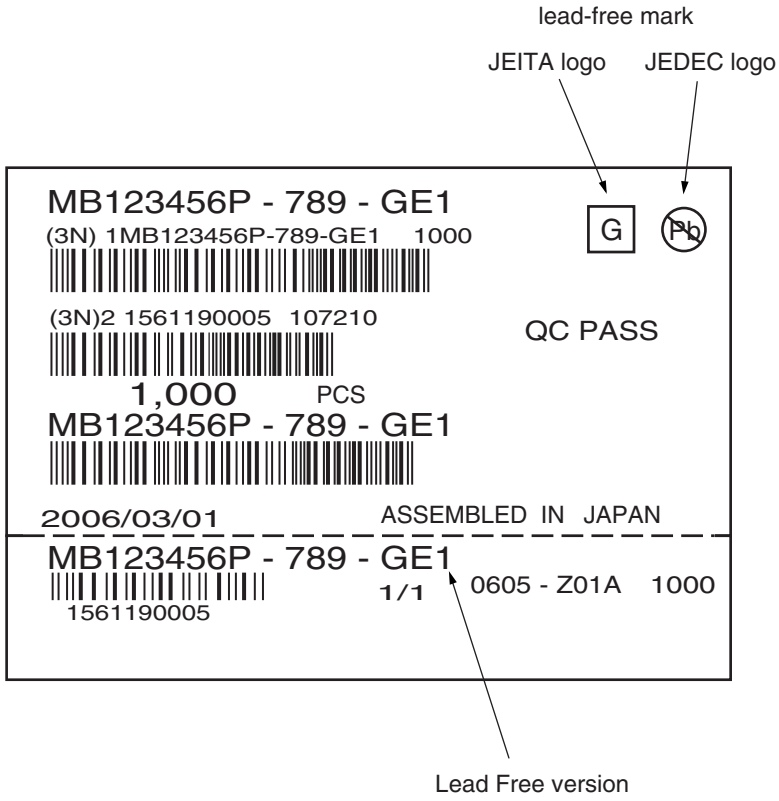


TSSOP-38P
(FPT-38P-M03)



BCC-40
(LCC-40P-M07)

■ LABELING SAMPLE (LEAD FREE VERSION)



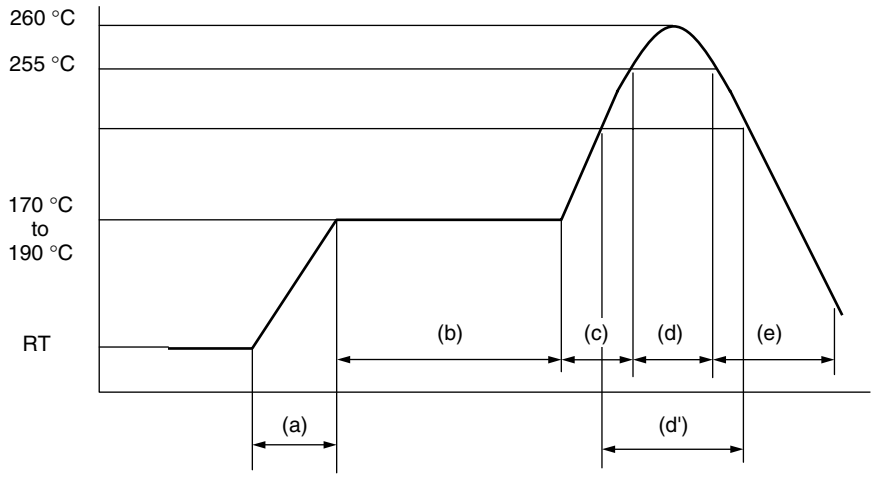
■ MB39A108PFT-❑❑❑E1 (TSSOP-38P)
RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

Item	Condition	
Mounting Method	IR (infrared reflow) , Manual soldering (partial heating method)	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after Manufacture.
	From opening to the 2nd reflow	Less than 8 days
	When the storage period after opening was exceeded	Please processes within 8 days after baking (125 °C, 24H)
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	

[Temperature Profile for FJ Standard IR Reflow]

(1) IR (infrared reflow)

H rank : 260 °C Max



(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60 s to 180 s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Actual heating : Temperature 260 °C Max; 255 °C or more, 10 s or less
(d') : Temperature 230 °C or more, 40 s or less
or
Temperature 225 °C or more, 60 s or less
or
Temperature 220 °C or more, 80 s or less
(e) Cooling : Natural cooling or forced cooling

Note : Temperature : the top of the package body

(2) Manual soldering (partial heating method)

Conditions : Temperature 400 °C Max
Times : 5 s max/pin

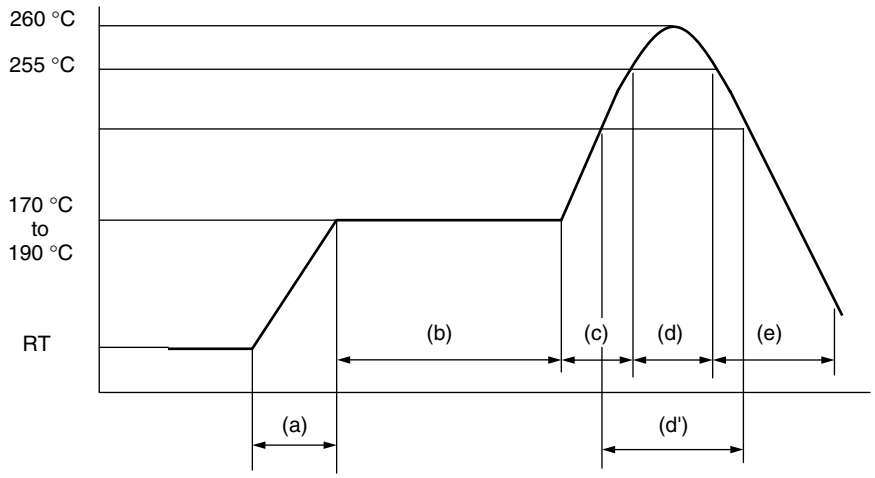
■ MB39A108PV2-❑❑❑E1 (BCC-40)
RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

Item	Condition	
Mounting Method	IR (infrared reflow) , Manual soldering (partial heating method)	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after Manufacture.
	From opening to the reflow	
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	

[Temperature Profile for FJ Standard IR Reflow]

(1) IR (infrared reflow)

H rank : 260 °C Max



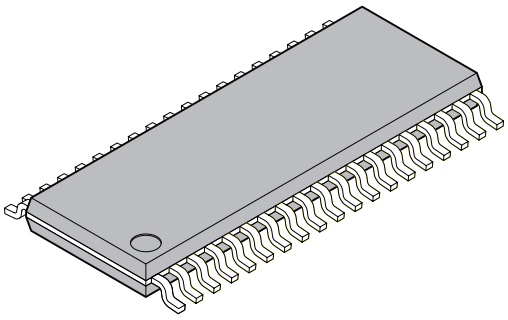
(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60 s to 180 s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Actual heating : Temperature 260 °C Max; 255 °C or more, 10 s or less
(d') : Temperature 230 °C or more, 40 s or less
or
Temperature 225 °C or more, 60 s or less
or
Temperature 220 °C or more, 80 s or less
(e) Cooling : Natural cooling or forced cooling

Note : Temperature : the top of the package body

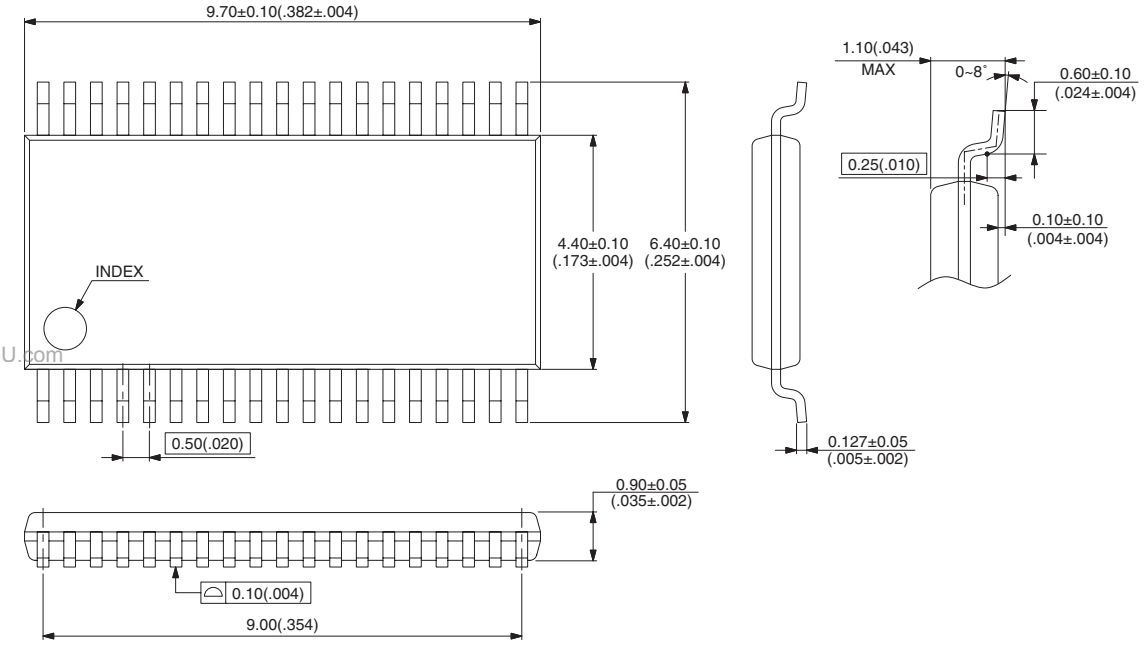
(2) Manual soldering (partial heating method)

Conditions : Temperature 400 °C Max
Times : 5 s max/pin

■ PACKAGE DIMENSION

38-pin plastic TSSOP		
	Lead pitch	0.50 mm
	Package width × package length	4.40 × 9.70 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.10 mm MAX
(FPT-38P-M03)		

38-pin plastic TSSOP
(FPT-38P-M03)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

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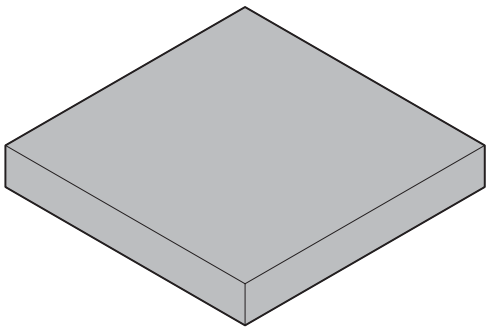
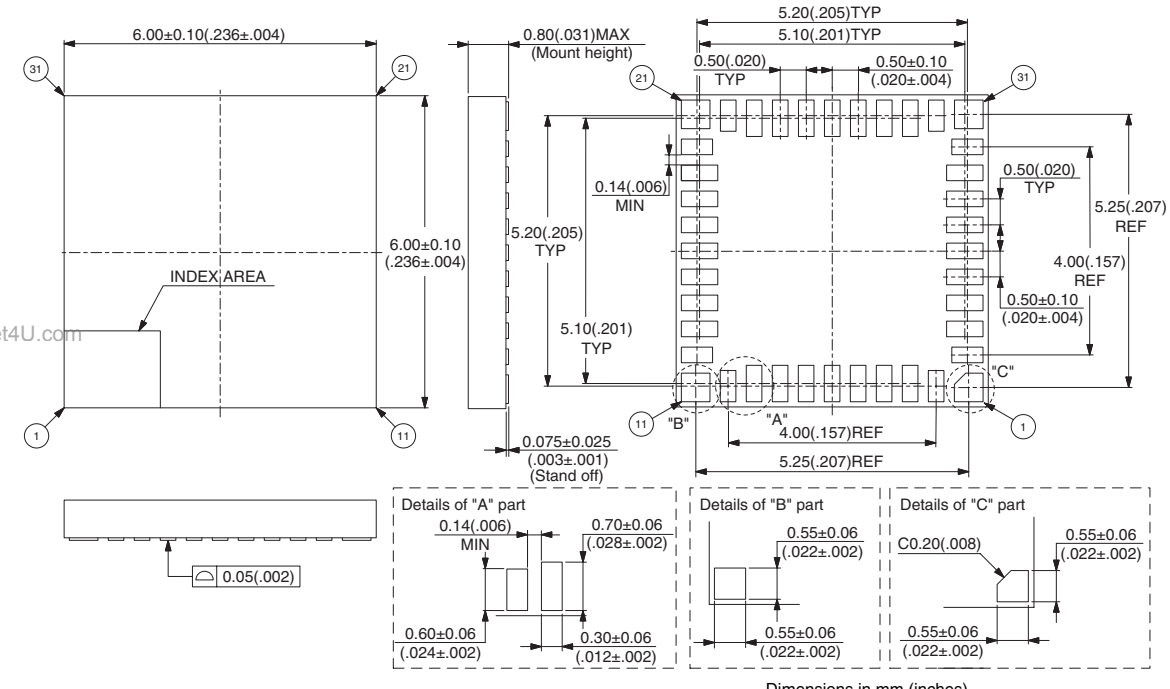
40-pin plastic BCC		
	Lead pitch	0.50 mm
	Package width × package length	6.00 mm × 6.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.05 g
(LCC-40P-M07)		

40-pin plastic BCC
(LCC-40P-M07)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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