TPS61163 Dual-Channel WLED Driver for Smart Phones

1 Features

- 2.7-V to 6.5-V Input Voltage
- Integrated 1.5-A, 40-V MOSFET
- 1.2-MHz Switching Frequency
- Dual Current Sinks of up to 30 mA Current Each
- 1% Typical Current Matching and Accuracy
- 37.5-V Overvoltage Protection (OVP) Threshold
- Adaptive Boost Output to WLED Voltages
- Very Low Voltage Headroom Control (90 mV)
- Flexible Digital and PWM Brightness Control
- One-Wire Control Interface (EasyScale™)
- PWM Dimming Control Interface
- Up to 100:1 PWM Dimming Ratio
- Up to 10-bit Dimming Resolution
- Up to 90% Efficiency
- Overvoltage Protection
- Built-in Soft Start
- Built-in WLED Open and Short Protection
- Thermal Shutdown
- Supports 4.7-µH Inductor Application

2 Applications

- Smart Phones
- PDAs, Handheld Computers
- GPS Receivers
- Backlight for Small and Media Form-Factor LCD Display With Single-Cell Battery Input

3 Description

The TPS61163 is a dual-channel WLED driver that provides highly integrated solutions for single-cell Li-ion battery-powered smartphone backlights. The device has a built-in high-efficiency boost regulator with integrated 1.5-A, 40-V power MOSFET and supports a voltage as low as 2.7 V. With two high current-matching-capability current-sink regulators, the device can drive up to 10s2p WLED diodes. The boost output can automatically adjust to the WLED forward voltage and allows very low voltage-headroom control, thus effectively improving the efficiency of the LED strings.

The TPS61163 supports both a PWM dimming interface and a one-wire digital EasyScale™ dimming interface, either which can achieve 9-bit dimming control.

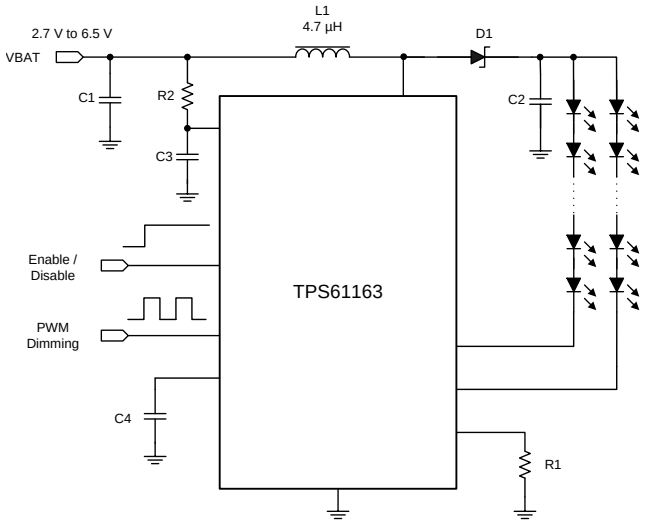
The TPS61163 integrates built-in soft start, overvoltage and overcurrent protection, and thermal shutdown protections.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
TPS61163	DSBGA (9)	1.336 mm × 1.336 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2013) to Revision D — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; reformatted *Thermal Information* notes ... 1
- Changed wording of second paragraph in *Boost Converter* subsection ... 10

Changes from Revision B (March 2013) to Revision C — **Page**

- Deleted TPS61162 from data sheet ... 1
- Changed PWM FREQ = 20kHz to PWM FREQ = 40kHz in Figure 3 ... 7
- Changed PWM FREQ = 20kHz to PWM FREQ = 40kHz in Figure 5 ... 7
- Changed PWM Freq = 20kHz to PWM Freq = 40kHz in the descriptions of Figure 16 - Figure 1, Figure 22, Figure 3, and Figure 5 in ... 20
- Changed PWM FREQ = 20kHz to PWM FREQ = 40kHz in Figure 22 ... 20

Changes from Revision A (February 2013) to Revision B — **Page**

- Initial release of the device ... 1

Changes from Original (January 2013) to Revision A — **Page**

- Changes to the Product Preview device ... 1

5 Device Comparison Table

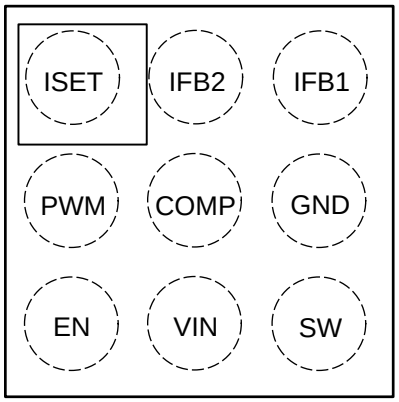
See(1)

T_A	PART NUMBER	OPEN LED PROTECTION	PACKAGE	ORDERING	PACKAGE MARKING
–40°C to +85°C	TPS61163	37.5 V (typical)	9-pin DSBGA	TPS61163YFF	TPS 61163

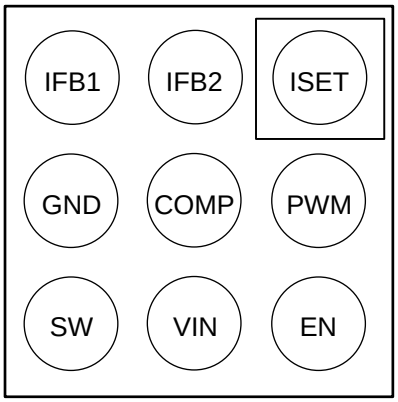
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

6 Pin Configuration and Functions

YFF Package
9-Pin DSBGA
Top View



YFF Package
9-Pin DSBGA
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
A1	ISET	I	Full-scale LED current set pin. Connecting a resistor to the pin programs the full-scale LED current
A2	IFB2	I	Regulated current sink input pin
A3	IFB1	I	Regulated current sink input pin
B1	PWM	I	PWM dimming signal input
B2	COMP	O	Output of the transconductance error amplifier. Connect external capacitor to this pin to compensate the boost loop
B3	GND	O	Ground
C1	EN	I	Enable control and one-wire digital signal input
C2	VIN	I	Supply input pin
C3	SW	I	Drain connection of the internal power MOSFET

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, PWM, IFB1, IFB2	–0.3	7	V
	COMP, ISET	–0.3	3	
	SW	–0.3	40	
P_D	Continuous power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	
		Machine model (MM)	200 (max)	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		6.5	V
V_{OUT}	Output voltage	V_{IN}		38	V
L	Inductor	4.7		10	µH
C_I	Input capacitor	1			µF
C_O	Output capacitor	1		2.2	µF
C_{COMP}	Compensation capacitor		330		nF
F_{PWM}	PWM dimming signal frequency	10		100	kHz
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61163 YFF (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	40	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 3.6 V, EN = high, PWM = high, IFB current = 20 mA, typical values are at T_A = 25°C, and minimum and maximum values are at T_A = –40°C to +85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		6.5	V
V_{VIN_UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.2	2.3	V
		V_{IN} rising			2.45	
V_{VIN_HYS}	VIN UVLO hysteresis			100		mV
I_Q	Operating quiescent current into VIN	Device enable, switching 1.2 MHz and no load V_{IN} = 3.6 V		1.2	2	mA
I_{SD}	Shutdown current	EN = low		1	2	µA
EN and PWM						
V_H	EN Logic high		1.2			V
V_L	EN Logic Low				0.4	V
V_H	PWM logic high		1.2			V
V_L	PWM logic low				0.4	V
R_{PD}	EN pin and PWM pin internal pulldown resistor		400	800	1600	kΩ
t_{PWM_SD}	PWM logic low width to shutdown	PWM high to low	20			ms
t_{EN_SD}	EN logic low width to shutdown	EN high to low	2.5			ms
CURRENT REGULATION						
V_{ISET_full}	ISET pin voltage	Full brightness	1.204	1.229	1.253	V
K_{ISET_full}	Current multiplier	Full brightness		1030		
I_{FB_avg}	Current accuracy	I_{ISET} = 20 µA, D = 100%, 0°C to 70°C	–2%		2%	
		I_{ISET} = 20 µA, D = 100%, –40°C to 85°C	–2.3%		2.3%	
K_M	$(I_{MAX} – I_{AVG}) / I_{AVG}$	D = 100%		1%	2%	
		D = 25%		1%		
I_{IFB_max}	Current sink max output current	I_{ISET} = 35 µA, each IFBx pin	30			mA
POWER SWITCH						
$R_{DS(on)}$	Switch MOSFET on resistance	V_{IN} = 3.6 V		0.25		Ω
		V_{IN} = 3 V		0.3		
I_{LEAK_SW}	Switch MOSFET leakage current	V_{SW} = 35 V, T_A = 25°C			1	µA
OSCILLATOR						
f_{SW}	Oscillator frequency		1000	1200	1500	kHz
D_{max}	Maximum duty cycle	Measured on the drive signal of switch MOSFET	91%	95%		
BOOST VOLTAGE CONTROL						
V_{IFB_reg}	IFBx feedback regulation voltage	I_{IFBx} = 20 mA, measured on IFBx pin which has a lower voltage		90		mV
I_{sink}	COMP pin sink current			12		µA
I_{source}	COMP pin source current			5		µA
G_{ea}	Error amplifier transconductance		30	55	80	µmho
R_{ea}	Error amplifier output resistance			45.5		MΩ
f_{ea}	Error amplifier crossover frequency	5 pF connected to COMP pin		1.65		MHz

Electrical Characteristics (continued)

V_{IN} = 3.6 V, EN = high, PWM = high, IFB current = 20 mA, typical values are at T_A = 25°C, and minimum and maximum values are at T_A = –40°C to +85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION						
I_{LIM}	Switch MOSFET current limit	D = D_{max}, 0°C to 70°C	1	1.5	2	A
I_{LIM_Start}	Switch MOSFET start up current limit	D = D_{max}		0.7		A
t_{Half_LIM}	Time window for half current limit			5		ms
V_{OVP_SW}	SW pin over voltage threshold		36	37.5	39	V
V_{OVP_IFB}	IFBx pin over voltage threshold	Measured on IFBx pin	4.2	4.5	4.8	V
V_{ACKNL}	Acknowledge output voltage low Open drain, R_{pullup} = 15 kΩ to V_{IN} (1)				0.4	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown hysteresis			15		°C

(1) Acknowledge condition active 0, this condition is only applied when the RFA bit is set to 1. To use this feature, master must have an open drain output, and the data line must be pulled up by the master with a resistor load.

7.6 EasyScale Timing Requirements

		MIN	NOM	MAX	UNIT
t_{es_delay}	EasyScale detection delay, measured from EN low to high	100			µs
t_{es_det}	EasyScale detection time, EN pin low time	260			µs
t_{es_win}	EasyScale detection window, easured from EN low to high (1)	1			ms
t_{start}	Start time of program stream	2			µs
t_{EOS}	End time of program stream	2		360	µs
t_{H_LB}	High time of low bit (Logic 0)	2		180	µs
t_{L_LB}	Low time of low bit (Logic 0)	2 × t_{H_LB}		360	µs
t_{H_HB}	High time of high bit (Logic 1)	2 × t_{L_HB}		360	µs
t_{L_HB}	Low time high bit (Logic 1)	2		180	µs
$t_{valACKN}$	Acknowledge valid time			2	µs
t_{ACKN}	Duration of acknowledge condition			512	µs

(1) To select EasyScale interface, after t_{es_delay} delay from EN low to high, drive EN pin to low for more than t_{es_det} before t_{es_win} expires.

7.7 Typical Characteristics

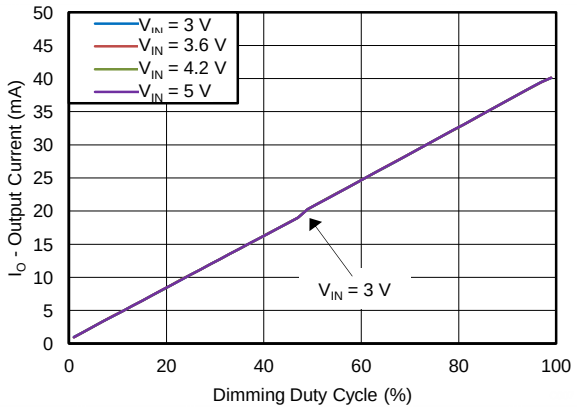


Figure 1. Dimming Linearity

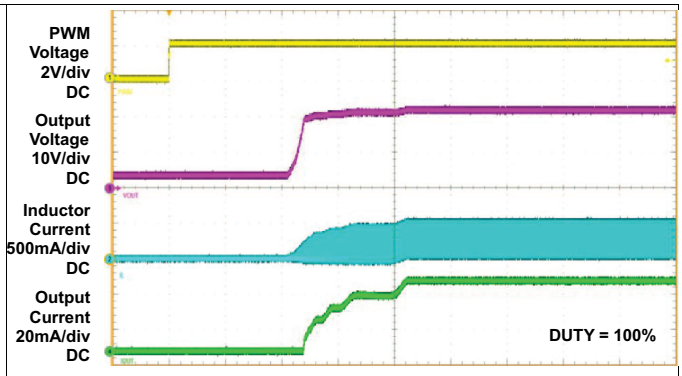


Figure 2. Start-Up Waveform

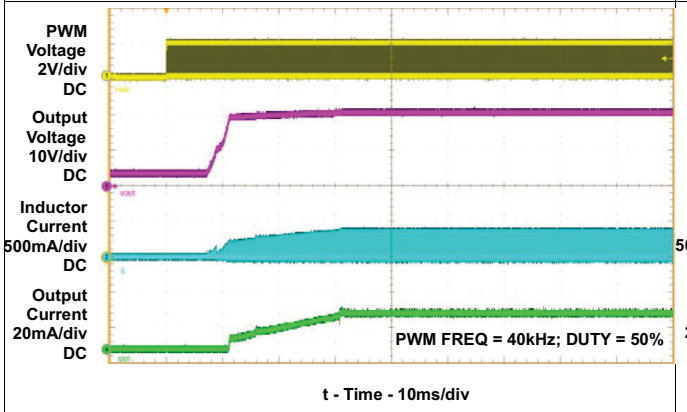


Figure 3. Start-Up Waveform

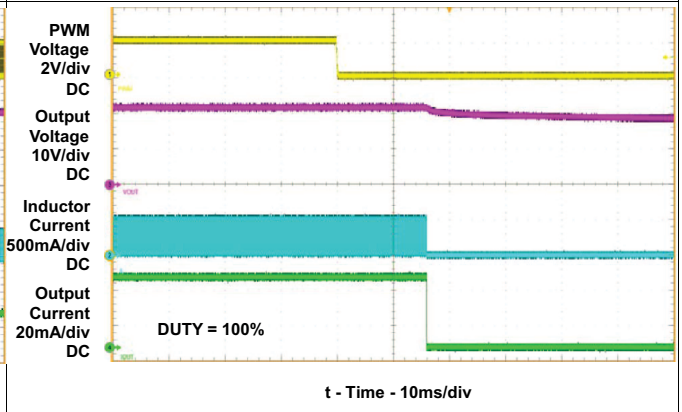


Figure 4. Shutdown Waveform

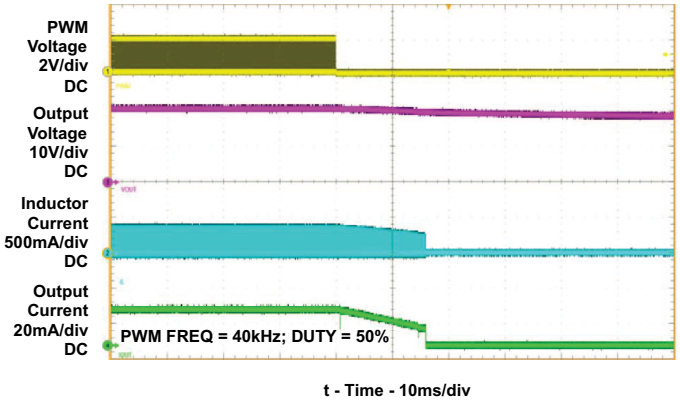


Figure 5. Shutdown Waveform

8 Detailed Description

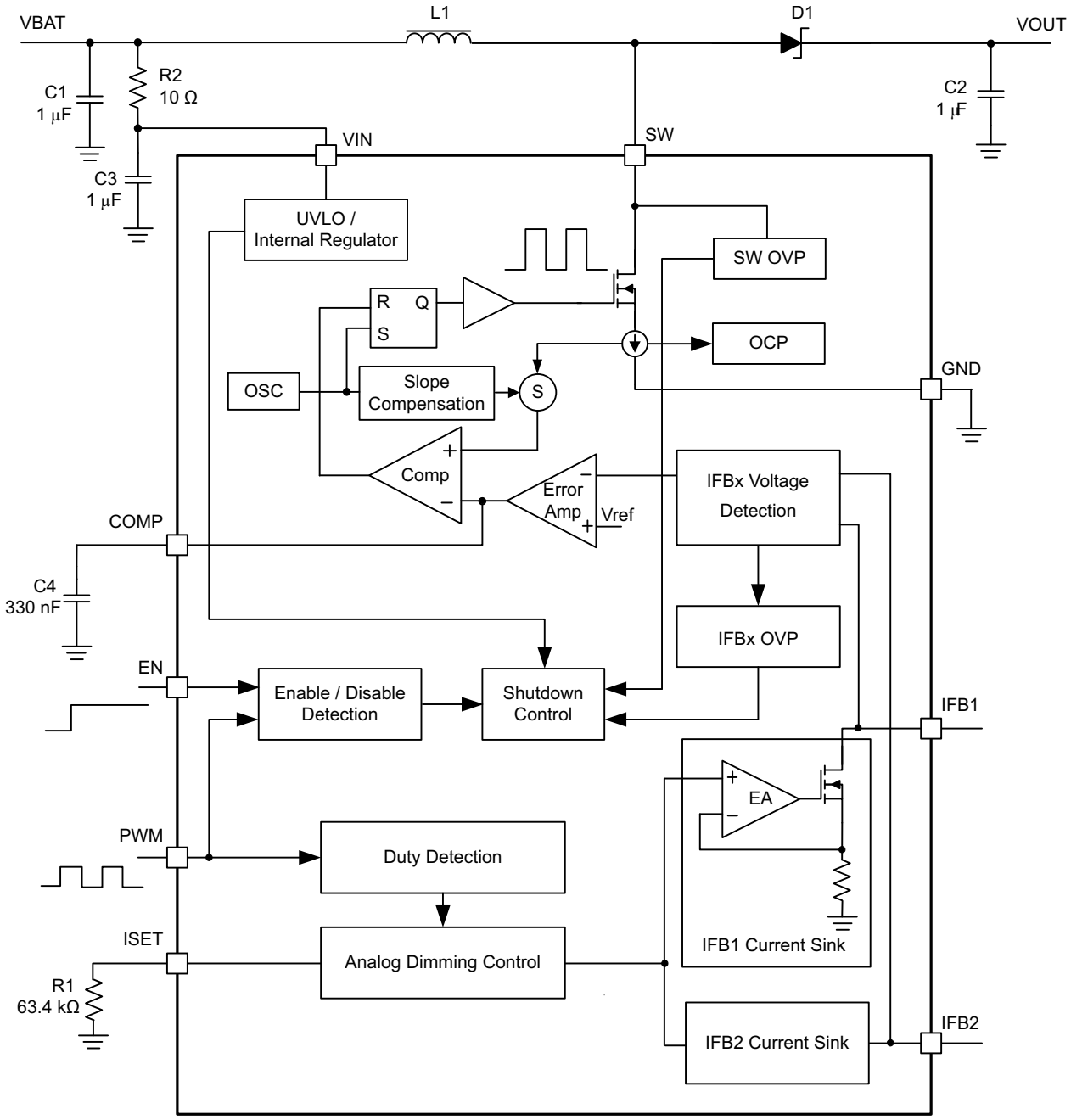
8.1 Overview

The TPS61163 is a high efficiency, dual-channel white LED driver for smart phone backlighting applications. Two current sink regulators of high current-matching capability are integrated in the TPS61163 to support dual LED strings connection, to improve the current balance and protect the LED diodes when either LED string is open or short.

The TPS61163 integrates all of the key function blocks to power and control up to 20 white LED diodes. It includes a 40-V/1.5-A boost converter, two current sink regulators, and protection circuit for overcurrent, overvoltage and thermal shutdown protection.

In order to provide high brightness backlighting for big size or high resolution smartphone panels, a greater quantity of white LED diodes are used. Having all LED diodes in a string improves overall current matching; however, the output voltage of a boost converter is limited when input voltage is low, and normally the efficiency drops when output voltage goes very high. Thus, the LED diodes are arranged in two parallel strings.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Boost Converter

The boost converter of the TPS61163 integrates a 40-V, 1.5-A low-side switch MOSFET and has a fixed switching frequency of 1.2 MHz. The control architecture is based on traditional current-mode PWM control. For operation see the block diagram. Two current sinks regulate the dual-channel current and the boost output is automatically set by regulating voltage of the IFBx pin. The output of error amplifier and the sensed current of switch MOSFET are applied to a control comparator to generate the boost switching duty cycle; slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%.

In order to ensure that both current sinks remain in regulation whenever there is a mismatch in string voltages while the power dissipation of the current sink regulators is minimized, the minimum headroom voltage between IFB1 and IFB2 becomes the regulation point for the boost converter. For example, if the LEDs connected to IFB1 require 20 V, and the LEDs connected to IFB2 require 20.5 V at the programmed current, then the voltage at IFB2 is about 90 mV, and the voltage at IFB1 is about 0.59 V. In other words, the boost makes the cathode of the highest voltage LED string the regulation point.

8.3.2 IFBX Pin Unused

If only one channel is needed, a user can easily disable the unused channel by connecting its IFBx pin to ground. If both IFBx pins are connected to ground, the device does not start up.

8.3.3 Enable and Start-up

In order to enable the device from shutdown mode, three conditions have to be met:

1. Power-on reset (POR) (that is, V_{IN} voltage is higher than UVLO threshold);
2. Logic high on EN pin; and
3. PWM signal (logic high or PWM pulses) on PWM pin.

The TPS61163 supports two dimming interfaces: one-wire digital interface (EasyScale interface) and PWM interface. The TPS61163 begins an EasyScale detection window after start-up to detect which interface is selected. If the EasyScale interface is needed, signals of a specific pattern must be input into EN pin during the EasyScale detection window; otherwise, PWM dimming interface is enabled (see details in *One-Wire Digital Interface (Easyscale Interface)*).

After the EasyScale detection window, the TPS61163 checks the status of IFBx pins. If one IFBx pin is detected as connected to ground, the corresponding channel is disabled and removed from the control loop. Then the soft start begins, and the boost converter starts switching. If both IFBx pins are shorted to ground, the TPS61163 does not start up.

Either pulling EN pin low for more than 2.5 ms or pulling PWM pin low for more than 20 ms can disable the device, and the TPS61163 enters into shutdown mode.

8.3.4 Soft Start

Soft start is implemented internally to prevent voltage overshoot and in-rush current. After the IFBx pin status detection, the COMP pin voltage starts ramp up, and the boost starts switching. During the beginning 5 ms (t_{Half_LIM}) of the switching, the peak current of the switch MOSFET is limited at I_{LIM_Start} (0.7 A typical) to avoid the input inrush current. After the first 5 ms, the current limit is changed to I_{LIM} (1.5 A typical) to allow the normal operation of the boost converter.

Feature Description (continued)

8.3.5 Full-Scale Current Program

The dual channels of the TPS61163 can provide up to 30 mA current each. It does not matter whether either the EasyScale interface or the PWM interface is selected — the full-scale current (current when dimming duty cycle is 100%) of each channel must be programmed by an external resistor R_{ISET} at the ISET pin according to Equation 1.

$$I_{FB\_full} = \frac{V_{ISET\_full}}{R_{ISET}} \times K_{ISET\_full} \quad (1)$$

where

- I_{FB_full}, full-scale current of each channel
- K_{ISET_full} = 1030 (current multiple when dimming duty cycle = 100%)
- V_{ISET_full} = 1.229 V (ISET pin voltage when dimming duty cycle = 100%)
- R_{ISET} = ISET pin resistor

8.3.6 Brightness Control

The TPS61163 controls the DC current of the dual channels to realize the brightness dimming. The DC current control is normally referred to as analog dimming mode. When the DC current of LED diode is reduced, the brightness is dimmed.

The TPS61163 can receive either the PWM signals at the PWM pin (PWM interface) or digital commands at the EN pin (EasyScale interface) for brightness dimming. If the EasyScale interface is selected, the PWM pin must be kept high; if PWM interface is selected, the EN pin must be kept high.

8.3.7 Undervoltage Lockout

An undervoltage lockout circuit prevents the operation of the device at input voltages below undervoltage threshold (2.2 V typical). When the input voltage is below the threshold, the device is shut down. If the input voltage rises by undervoltage lockout hysteresis, the device restarts.

8.3.8 Overvoltage Protection

Overvoltage protection circuitry prevents device damage as the result of white LED string disconnection or shortage.

The TPS61163 monitors the voltages at SW pin and IFBx pin during each switching cycle. No matter either SW OVP threshold V_{OVP_SW} or IFBx OVP threshold V_{OVP_FB} is reached due to the LED string open or short issue, the protection circuitry is triggered. Refer to Figure 6 and Figure 7 for the protection actions.

If one LED string is open, its IFBx pin voltage drops, and the boost output voltage is increased by the control loop as it tries to regulate this lower IFBx voltage to the target value (90 mV typical). For the normal string, its current is still under regulation but its IFBx voltage increases along with the output voltage. During the process, either the SW voltage reaches its OVP threshold V_{OVP_SW} or the voltage of the IFBx normal string reaches the IFBx OVP threshold V_{OVP_FB}, then the protection circuitry is triggered accordingly.

If both LED strings are open, the voltages of both IFBx pins drop to ground, the boost output voltage is increased by the control loop until reaching the SW OVP threshold V_{OVP_SW}, the SW OVP protection circuitry is triggered, and the device is latched off. Only VIN POR or EN/PWM pin toggling can restart the device.

One LED diode short in a string is allowed for the TPS61163. If one LED diode in a string is short, the IFBx voltage of the normal string is regulated to about 90 mV, and the IFBx pin voltage of the abnormal string is higher. Normally with only one diode short, the higher IFBx pin voltage does not reach the IFBx OVP threshold V_{OVP_FB}, so the protection circuitry is not triggered.

If more than one LED diodes are short in a string, as the boost loop regulates the IFBx voltage of the normal string to 90 mV, the IFBx pin voltage of the abnormal string is much higher and reaches V_{OVP_FB}; the protection circuitry is then triggered.

The SW OVP protection is also triggered when the forward voltage drop of an LED string exceeds the SW OVP threshold. In this case, the device turns off the switch FET and shuts down.

Feature Description (continued)

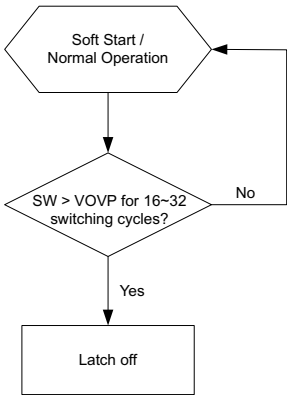


Figure 6. SW OVP Protection Action

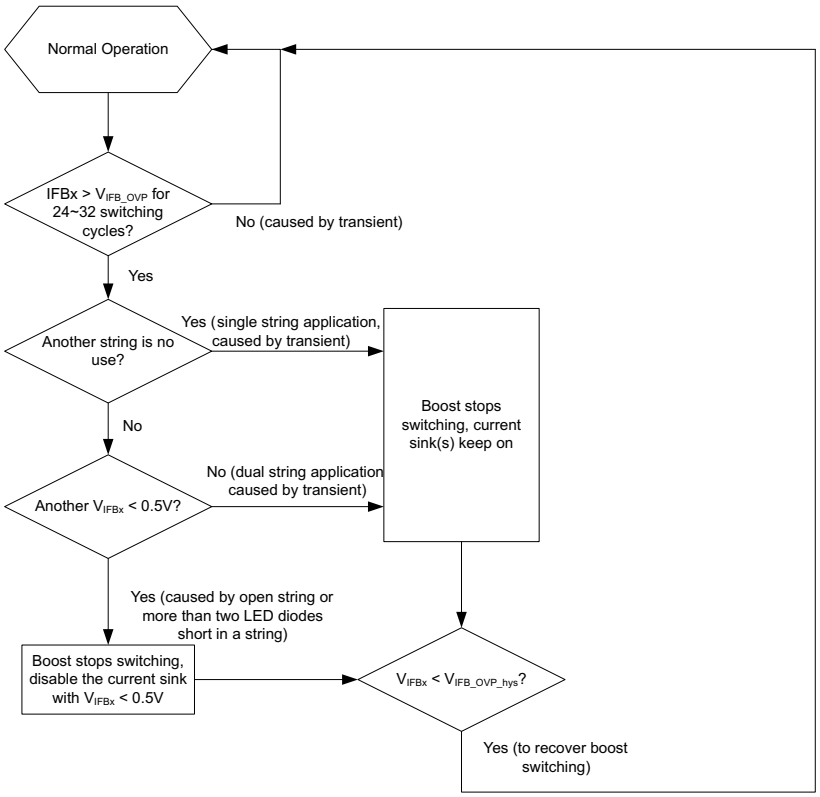


Figure 7. V_{IFBX} OVP Protection Action

8.3.9 Overcurrent Protection

The TPS61163 has a pulse-by-pulse overcurrent limit. The boost switch turns off when the inductor current reaches this current threshold, and it remains off until the beginning of the next switching cycle. This protects the TPS61163 and external component under overload conditions.

8.3.10 Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

8.4 Device Functional Modes

8.4.1 One-Wire Digital Interface (Easyscale Interface)

The EN pin features a simple digital interface to allow digital brightness control. The digital dimming interface can save the processor power and battery life as it does not require PWM signals all the time, and the processor can enter idle mode if possible. In order to enable the EasyScale interface, the following conditions must be satisfied and the specific digital pattern on the EN pin must be recognized by the device every time the TPS61163 starts up from shutdown mode.

1. VIN voltage is higher than UVLO threshold, and the PWM pin is pulled high.
2. Pull the EN pin from low to high to enable the TPS61163. At this moment, the EasyScale detection window starts.
3. After EasyScale detection delay time (t_{es_delay}, 100 µs), drive EN to low for more than EasyScale detection time (t_{es_detect}, 260 µs).

The third step must be finished before the EasyScale detection window (t_{es_win}, 1 ms) expires and, once this step is finished, the EasyScale interface is enabled, and the EasyScale communication can start. See Figure 8.

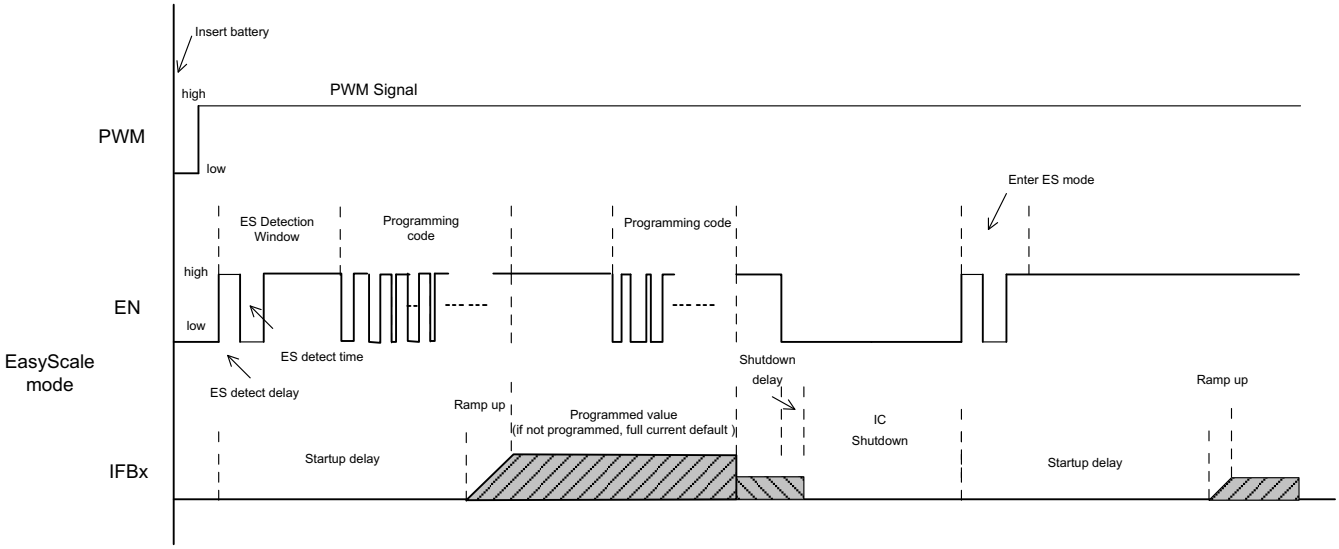


Figure 8. Easyscale Interface Detection

The TPS61163 supports 9-bit brightness code programming. By the EasyScale interface, a master can program the 9-bit code D8(MSB) to D0(LSB) to any of 511 steps with a single command. The default code value of D8-D0 is 111111111 when the device is first enabled, and the programmed value is stored in an internal register and set the dual-channel current according to Equation 2. The code is reset to default value when the deviceis shut down or disabled.

$$I_{FBx} = I_{FB\_full} \times \frac{Code}{511} \quad (2)$$

where

- I_{FB_full}: the full-scale LED current set by the R_{ISET} at ISET pin
- Code: the 9-bit brightness code D8~D0 programmed by EasyScale interface

When the one-wire digital interface at the EN pin is selected, the PWM pin can be connected to either the VIN pin or a GPIO (refer to *Additional Application Circuits*). If the PWM pin is connected to the VIN pin, the EN pin alone can enable and disable the device: pulling the EN pin low for more than 2.5 ms disables the device. If the PWM pin is connected to a GPIO, both the PWM and EN signals must be high to enable the device, and either pulling EN pin low for more than 2.5 ms or pulling the PWM pin low for more than 20 ms disables the device.

Device Functional Modes (continued)

8.4.2 PWM Control Interface

The PWM control interface is automatically enabled if the EasyScale interface fails to be enabled during start-up. In this case, the TPS61163 receives PWM dimming signals on the PWM pin to control the backlight brightness. When using PWM interface, the EN pin can be connected to VIN pin or a GPIO (refer to *Additional Application Circuits*). If the EN pin is connected to the VIN pin, the PWM pin alone is used to enable and disable the device: pull the PWM pin high or apply PWM signals at the PWM pin to enable the device; pull the PWM pin low for more than 20 ms to disable the device. If the EN pin is connected to a GPIO, either pull the EN pin low for more than 2.5 ms or pull the PWM pin low for more than 20 ms to disable the device. The TPS61163 device can start up only after both EN and PWM signals are applied. See Figure 9.

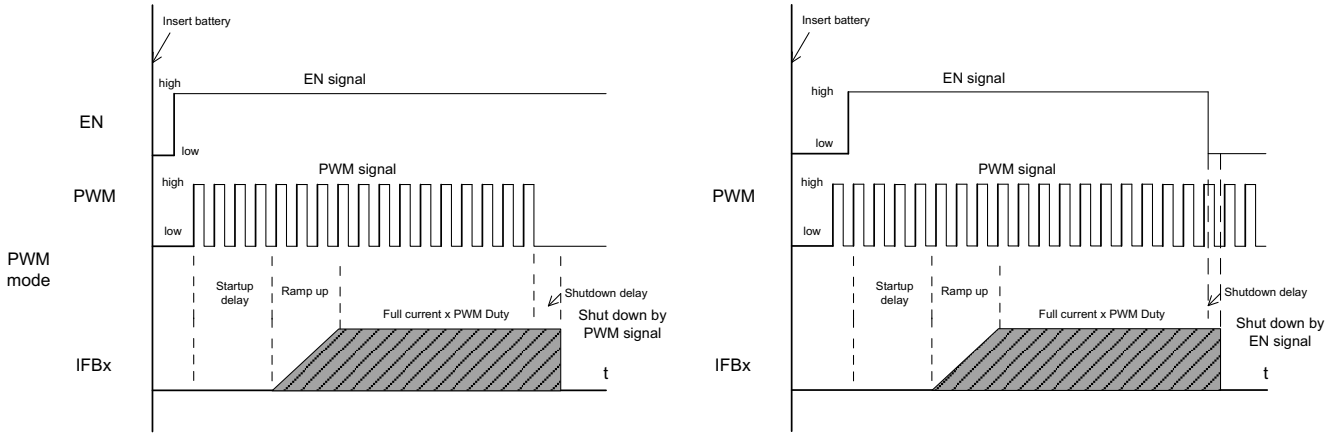


Figure 9. PWM Control Interface Detection

When the PWM pin is constantly high, the dual channel current is regulated to full-scale according to Equation 1. The PWM pin allows PWM signals to reduce this regulation current according to the PWM duty cycle; therefore, it achieves LED brightness dimming. The relationship between the PWM duty cycle and IFBx current is given by Equation 3.

$$I_{FBx} = I_{FB\_full} \times Duty \quad (3)$$

where

- I_{FBx} is the current of each current sink
- I_{FB_full} is the full-scale LED current
- Duty is the duty cycle information detected from the PWM signals

8.5 Programming

8.5.1 Easyscale Programming

EasyScale is a simple, but flexible, one-pin interface to configure the current of the dual channels. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor and the deviceis the slave. Figure 10 and Table 1 give an overview of the protocol used by TPS61163. A command consists of 24 bits, including an 8-bit device address byte and a 16-bit data byte. All of the 24 bits must be transmitted together each time, and the LSB bit must be transmitted first. The device address byte D7(MSB)~D0(LSB) is fixed to 0x8F. The data byte includes 9 bits D8(MSB)~D0(LSB) for brightness information and an RFA bit. The RFA bit set to 1 indicates the request for acknowledge condition. The acknowledge condition is only applied when the protocol is received correctly. The advantage of EasyScale compared with other one pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7 kBit/sec and up to 160 kBit/sec.

Programming (continued)

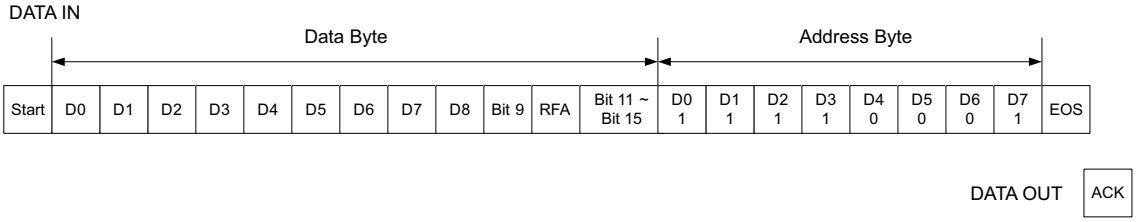


Figure 10. Easyscale Protocol Overview

Table 1. Easyscale Bits Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte (0x8F)	23 (MSB)	DA7	IN	DA7 = 1, MSB of device address
	22	DA6		DA6 = 0
	21	DA5		DA5 = 0
	20	DA4		DA4 = 0
	19	DA3		DA3 = 1
	18	DA2		DA2 = 1
	17	DA1		DA1 = 1
	16	DA0		DA0 = 1, LSB of device address
Data Byte	15	Bit 15	IN	No information. Write 0 to this bit.
	14	Bit 14		No information. Write 0 to this bit.
	13	Bit 13		No information. Write 0 to this bit.
	12	Bit 12		No information. Write 0 to this bit.
	11	Bit 11		No information. Write 0 to this bit.
	10	RFA		Request for acknowledge. If set to 1, device pulls low the data line when it receives the command well. This feature can only be used when the master has an open drain output stage and the data line must be pulled high by the master with a pullup resistor; otherwise, acknowledge condition is not allowed and don't set this bit to 1.
	9	Bit 9		No information. Write 0 to this bit.
	8	D8		Data bit 8, MSB of brightness code
	7	D7		Data bit 7
	6	D6		Data bit 6
	5	D5		Data bit 5
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0, LSB of brightness code

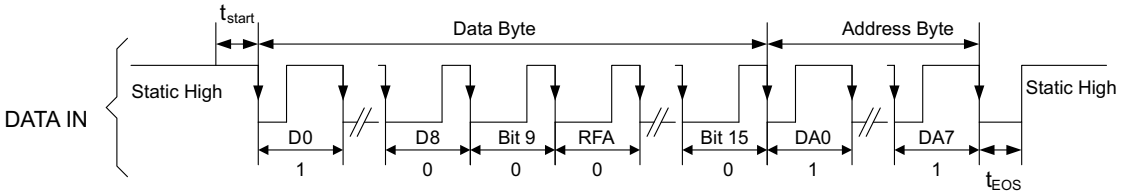


Figure 11. Easyscale Timing With RFA = 0

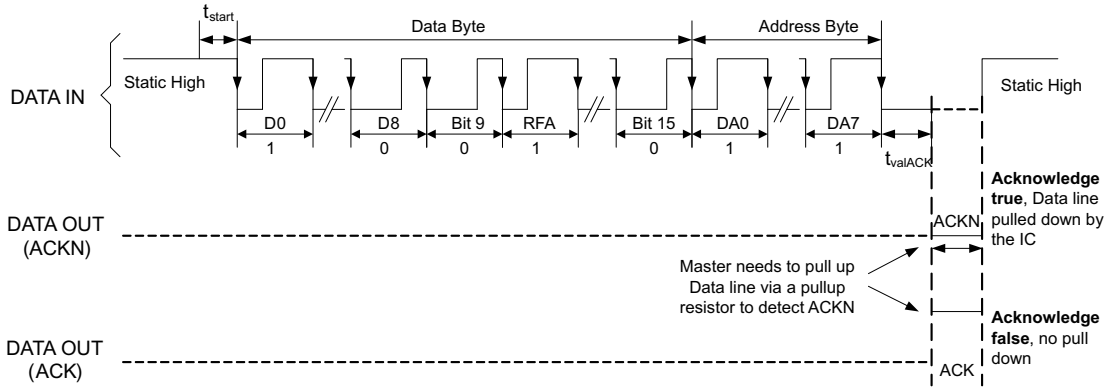


Figure 12. Easyscale Timing With RFA = 1

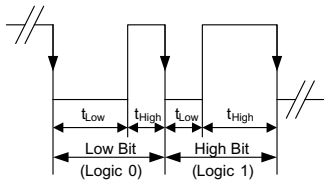


Figure 13. Easyscale — Bit Coding

The 24-bit command must be transmitted with LSB first and MSB last. Figure 11 shows the protocol without acknowledge request (Bit RFA = 0), Figure 12 with acknowledge request (Bit RFA = 1). Before the command transmission, a start condition must be applied. For this, the EN pin must be pulled high for at least t_{start} (2µs) before the bit transmission starts with the falling edge. If the EN pin is already at high level, no start condition is needed. The transmission of each command is closed with an end-of-stream (EOS) condition for at least t_{EOS} (2 µs).

The bit detection is based on a logic detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH} (refer to Figure 13). It can be simplified to:

Low Bit (Logic 0): $t_{LOW} \geq 2 \times t_{HIGH}$

High Bit (Logic 1): $t_{HIGH} \geq 2 \times t_{LOW}$

The bit detection starts with a falling edge on the EN pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by setting RFA bit to 1.
- The transmitted device address matches with the device address of the device.
- Total 24 bits are received correctly.

If previous conditions are met, after t_{valACK} delay from the moment when the last falling edge of the protocol is detected, an internal ACKN-MOSFET is turned on to pull the EN pin low for the time t_{ACKN}, which is 512 µs maximum, then the acknowledge condition is valid. During the t_{valACK} delay, the master controller keeps the line low; after the delay, it must release the line by outputting high impedance and then detect the acknowledge condition. If it reads back a logic 0, it means the device has received the command correctly. The EN pin can be used again by the master when the acknowledge condition ends after t_{ACKN} time.

Note that the acknowledge condition can only be requested when the master device has an open drain output. For a push-pull output stage, the use of a series resistor in the EN line to limit the current to 500 µA is recommended to for such cases as:

- An accidentally requested acknowledge, or
- To protect the internal ACKN-MOSFET.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS61163 device provides a complete high-performance LED lighting solution for mobile handsets. They can drive up to 2 strings of white LEDs with up to 10 LEDs per string. A boost converter generates the high voltage required for the LEDs. LED brightness can be controlled either by the PWM dimming interface or by the single-wire EasyScale dimming interface.

9.2 Typical Application

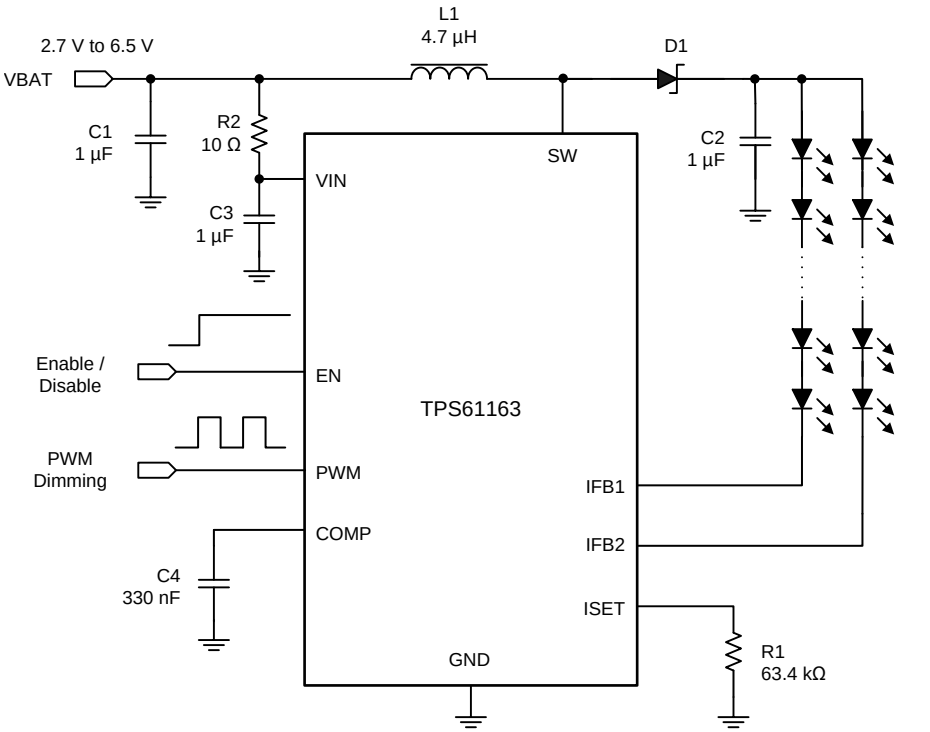


Figure 14. TPS61163 Typical Application

9.2.1 Design Requirements

For TPS61163 typical applications, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.7 V to 6.5 V
Boost switching frequency	1.2 MHz
Efficiency	up to 90%

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

Because the selection of inductor affects the steady-state operation of the power supply, transient behavior, loop stability, and the boost converter efficiency, the inductor is one of the most important components in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance (DCR), and saturation current. The TPS61163 is designed to work with inductor values from 4.7 µH to 10 µH to support all applications. A 4.7-µH inductor is typically available in a smaller or lower profile package, while a 10-µH inductor produces lower inductor ripple. If the boost output current is limited by the overcurrent protection of the device, using a 10-µH inductor may maximize the output current capability of controller. A 22-µH inductor can also be used for some applications, such as 6s2p and 7s2p, but may cause stability issue when more than eight WLED diodes are connected per string. Therefore, TI recommends customers verify the inductor in their application if it is different from the values in *Recommended Operating Conditions*.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation 4 to Equation 6 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage and maximum load current of the application. In order to leave enough design margin, the minimum switching frequency, the inductor value with –30% tolerance, and a low power conversion efficiency, such as 80% or lower are recommended for the calculation.

In a boost regulator, the inductor DC current can be calculated as Equation 4.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (4)$$

where

- V_{OUT} = boost output voltage
- I_{OUT} = boost output current
- V_{IN} = boost input voltage
- η = boost power conversion efficiency

The inductor current peak to peak ripple can be calculated as Equation 5.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times F_S} \quad (5)$$

where

- I_{PP} = inductor peak-to-peak ripple
- L = inductor value
- F_S = boost switching frequency
- V_{OUT} = boost output voltage
- V_{IN} = boost input voltage

Therefore, the peak current I_P seen by the inductor is calculated with Equation 6.

$$I_P = I_{DC} + \frac{I_{PP}}{2} \quad (6)$$

Select an inductor with saturation current over the calculated peak current. If the calculated peak current is larger than the switch MOSFET current limit I_{LIM}, use a larger inductor, such as 10 µH, and make sure its peak current is below I_{LIM}.

Boost converter efficiency is dependent on the resistance of its current path, the switching losses associated with the switch MOSFET and power diode and the inductor's core loss. The TPS61163 has optimized the internal switch resistance, however, the overall efficiency is affected a lot by the DCR of the inductor, equivalent series resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR/ESR conduction losses as well as higher core loss. Normally a datasheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, an inductor with lower DCR/ESR is recommended for TPS61163 application. However, there is a trade-off between the inductance, DCR/ESR resistance, and footprint of the inductor; furthermore, shielded inductors typically have higher DCR than unshielded ones. Table 3 lists some recommended inductors for the TPS61163. Verify whether the recommended inductor can support the target application by using the previous calculations as well as bench validation.

Table 3. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L x W x H mm)	VENDOR
LPS4018-472ML	4.7	125	1.9	4 × 4 × 1.8	Coilcraft
LPS4018-682ML	6.8	150	1.3	4 × 4 × 1.8	Coilcraft
LPS4018-103ML	10	200	1.3	4 × 4 × 1.8	Coilcraft
PIMB051B-4R7M	4.7	163	2.7	5.4 × 5.2 × 1.2	Cyntec
PIMB051B-6R8M	6.8	250	2.3	5.4 × 5.2 × 1.2	Cyntec

9.2.2.2 Compensation Capacitor Selection

The compensation capacitor C4 (refer to *Additional Application Circuits*) connected from the COMP pin to GND, is used to stabilize the feedback loop of the TPS61163. A 330-nF ceramic capacitor for C4 is suitable for most applications. A 470-nF capacitor also works for some applications, and it is suggested that customers verify it in their applications.

9.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirement for the output ripple and loop stability. A 1-µF to 2.2-µF capacitor is recommended for the loop stability consideration. This ripple voltage is related to the capacitor's capacitance and its ESR. Due to its low ESR, V_{ripple_ESR} could be neglected for ceramic capacitors. Assuming a capacitor with zero ESR, the output ripple can be calculated with Equation 7.

$$V_{ripple} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times C_{OUT}} \quad (7)$$

where

- V_{ripple} = peak-to-peak output ripple.

The additional part of ripple caused by the ESR is calculated using $V_{ripple\_ESR} = I_{OUT} \times R_{ESR}$ and can be ignored for ceramic capacitors.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50-V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

9.2.2.4 Schottky Diode Selection

The TPS61163 demands a low forward voltage, high-speed and low capacitance schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the reverse breakdown voltage of the diode must exceed the open LED protection voltage. TI recommends ONSemi MBR0540 and NSR05F40, and Vishay MSS1P4 for the TPS61163.

9.2.3 Application Curves

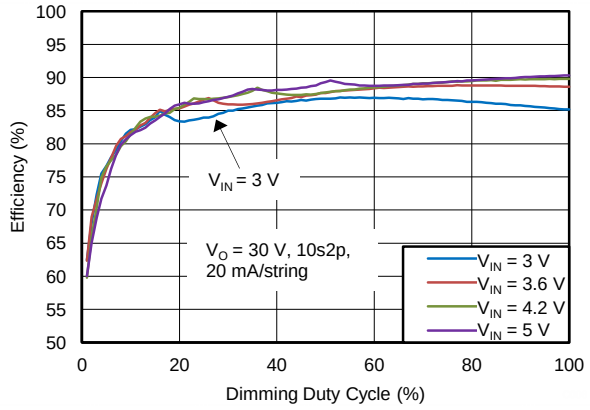


Figure 15. Efficiency vs Dimming Duty Cycle

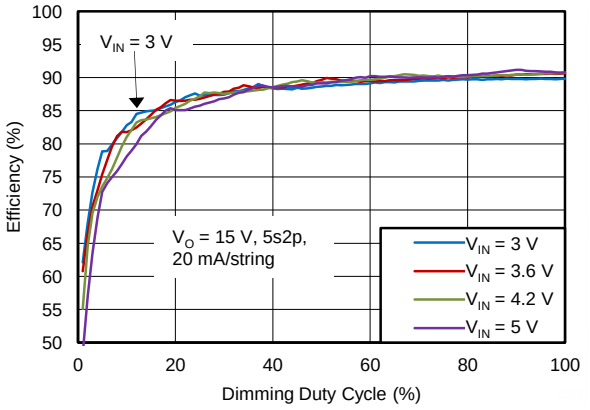


Figure 16. Efficiency vs Dimming Duty Cycle

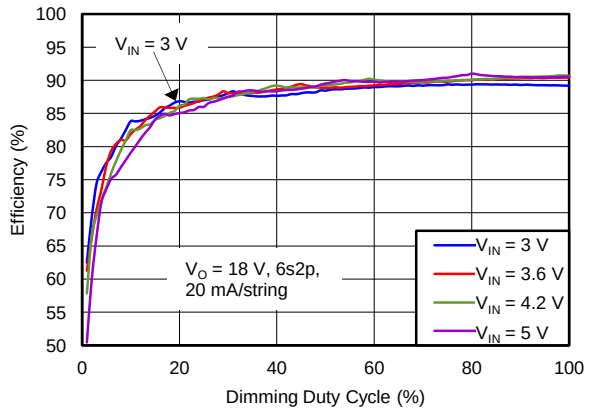


Figure 17. Efficiency vs Dimming Duty Cycle

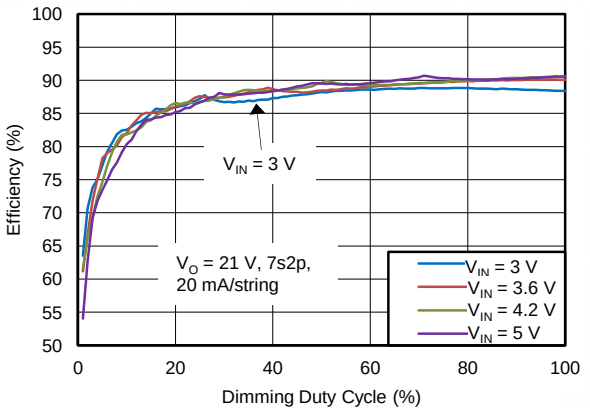


Figure 18. Efficiency vs Dimming Duty Cycle

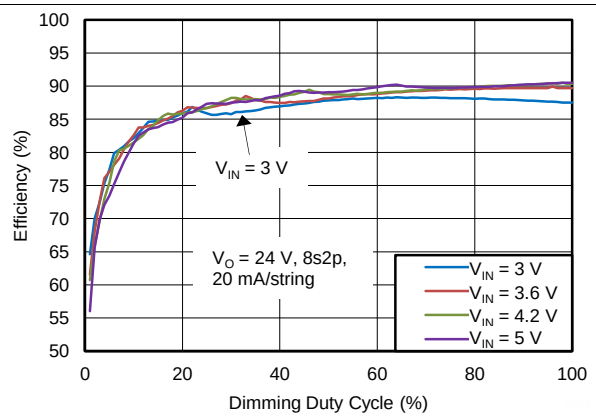


Figure 19. Efficiency vs Dimming Duty Cycle

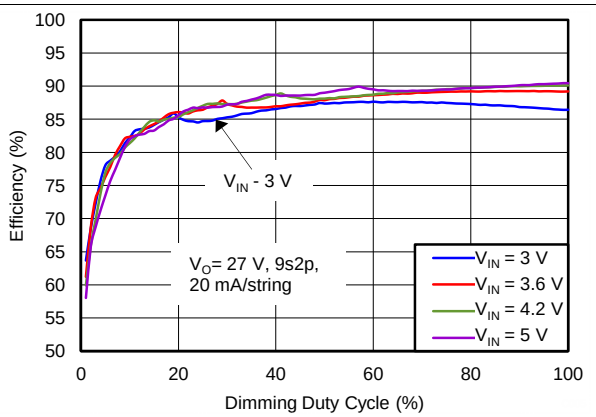


Figure 20. Efficiency vs Dimming Duty Cycle

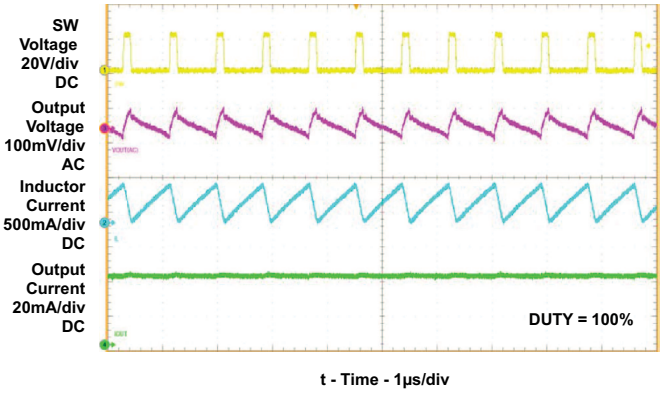


Figure 21. Switching Waveform

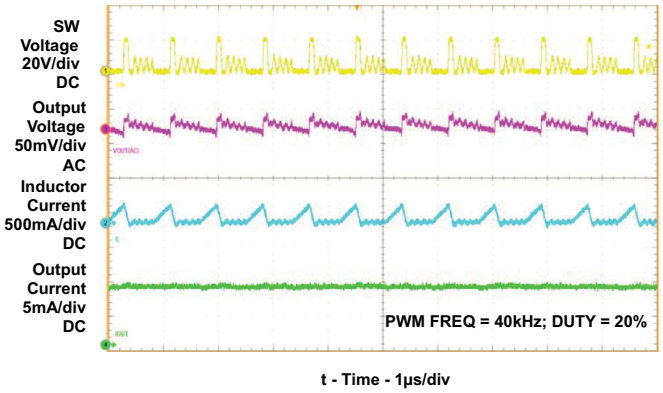
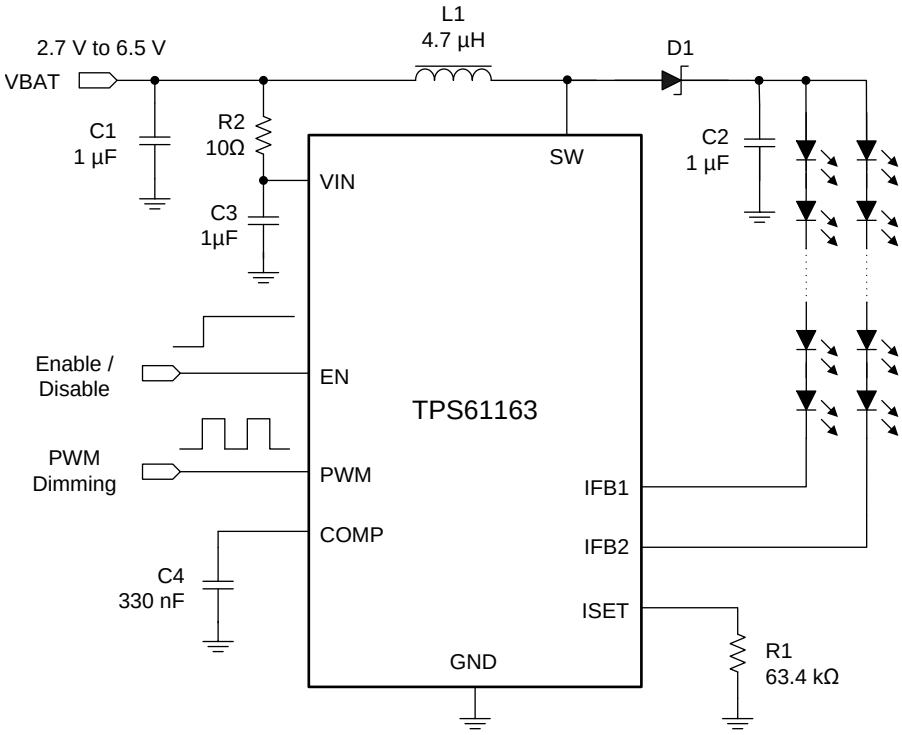


Figure 22. Switching Waveform

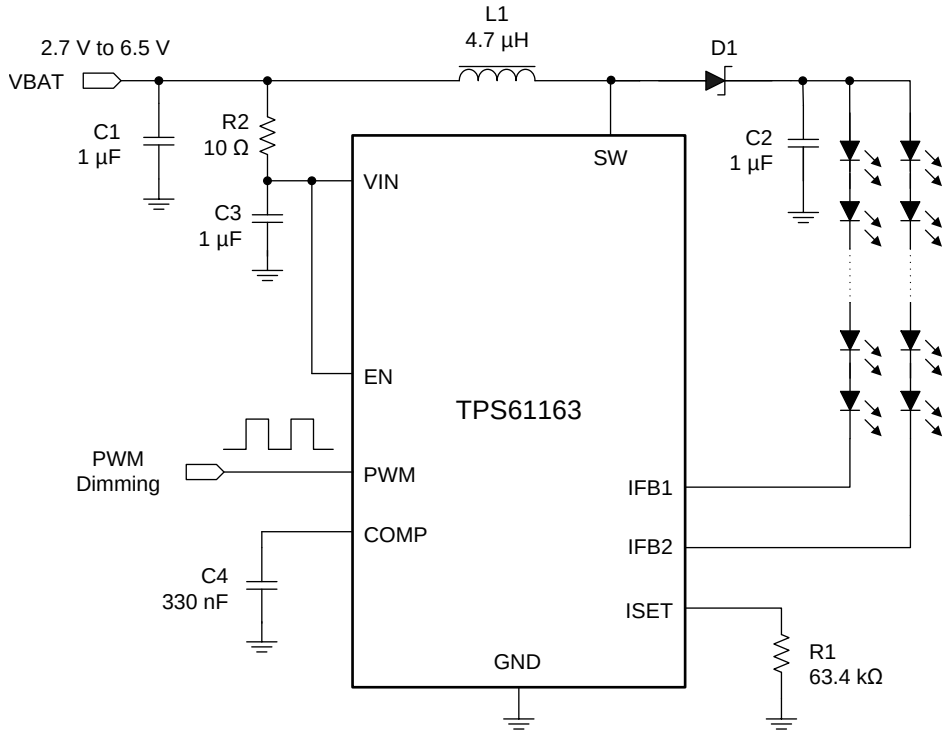
9.3 Additional Application Circuits



The EN pin can be used to enable or disable the device.

Figure 23. TPS61163 Typical Application - PWM Interface Enabled

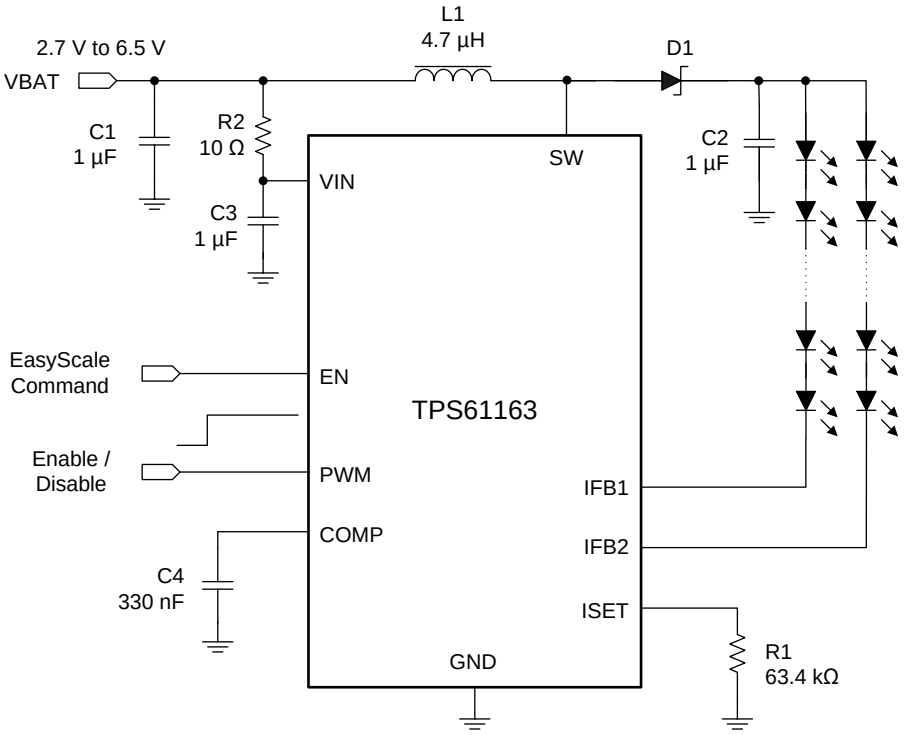
Additional Application Circuits (continued)



The EN pin is connected to VIN,; only the PWM signal is used to enable or disable the device.

Figure 24. TPS61163 Typical Application – PWM Interface Enabled

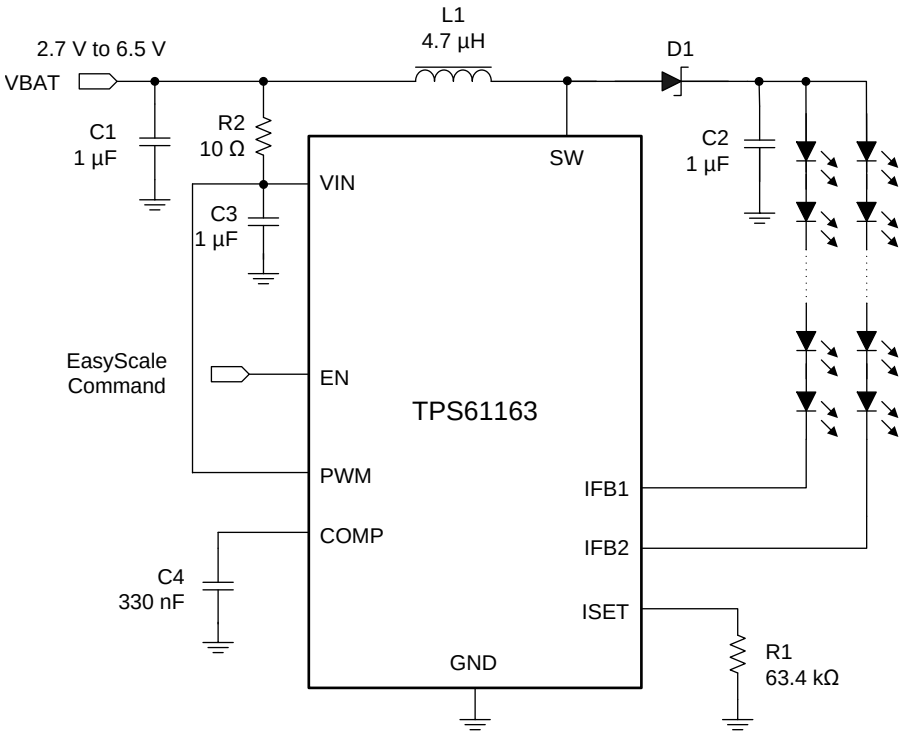
Additional Application Circuits (continued)



The PWM pin can be used to enable or disable the device.

Figure 25. TPS61163 Typical Application – One-Wire Digital Interface Enabled

Additional Application Circuits (continued)



The PWM pin is connected to VIN; only the EN signal is used to enable or disable the device.

Figure 26. TPS61163 Typical Application – One-Wire Digital Interface Enabled

10 Power Supply Recommendations

The TPS61163 is designed to operate from an input supply range of 2.7 V to 6.5 V. This input supply must be well regulated and be able to provide the peak current required by the LED configuration and inductor selected without voltage drop under load transients (start-up or rapid brightness change). If the input supply is located far from the device additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in *Additional Application Circuits*, must be close to the inductor, as well as to the VIN and GND pins in order to reduce the input ripple seen by the device. If possible, choose a higher capacitance value for C1. If the ripple seen at the VIN pin is so large that it affects the boost loop stability or internal circuits operation, TI recommends using R2 and C3 to filter and decouple the noise. In this case, C3 must be placed as close as possible to the VIN and GND pins.

The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor and Schottky diode must be kept as short and wide as possible. The trace between Schottky diode and the output capacitor C2 must also be as short and wide as possible. It is beneficial to have the ground of the output capacitor C2 close to the GND pin because there is a large ground return current flowing between them. When laying out signal grounds, TI recommends using short traces separated from power ground traces, and connected together at a single point close to the GND pin.

11.2 Layout Example

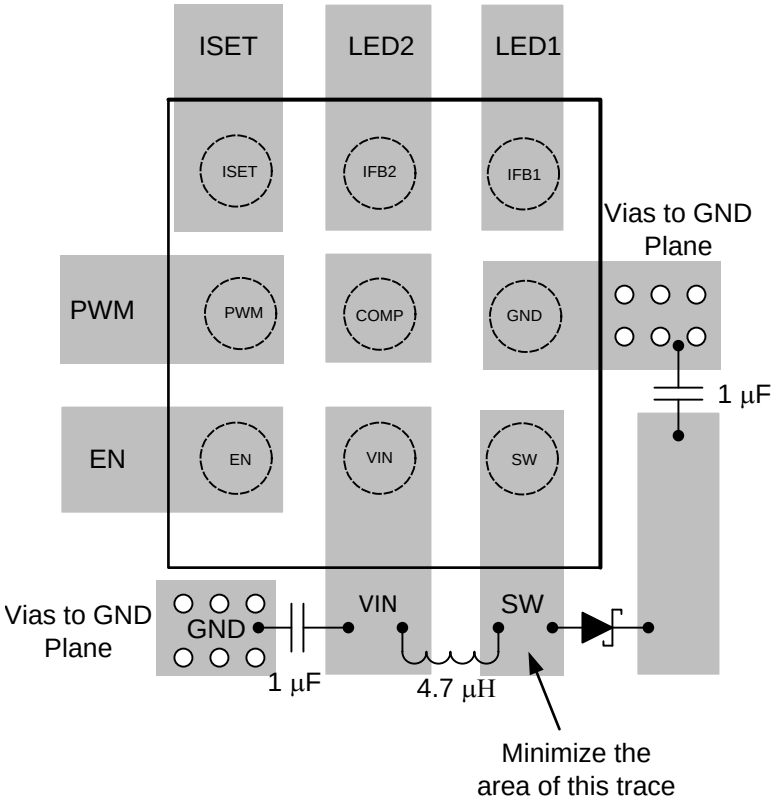


Figure 27. TPS61163 Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

EasyScale, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61163YFFR	NRND	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 150	TPS 61163	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

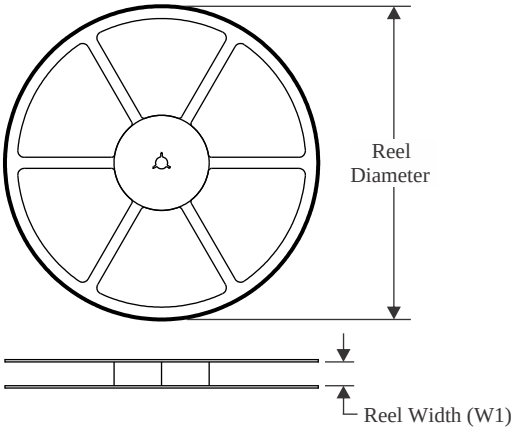
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

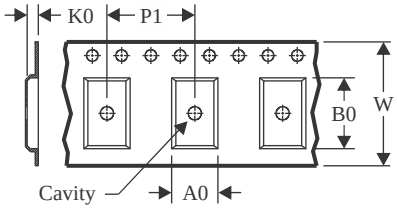
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

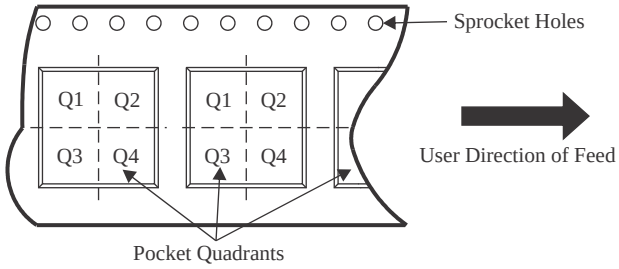


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

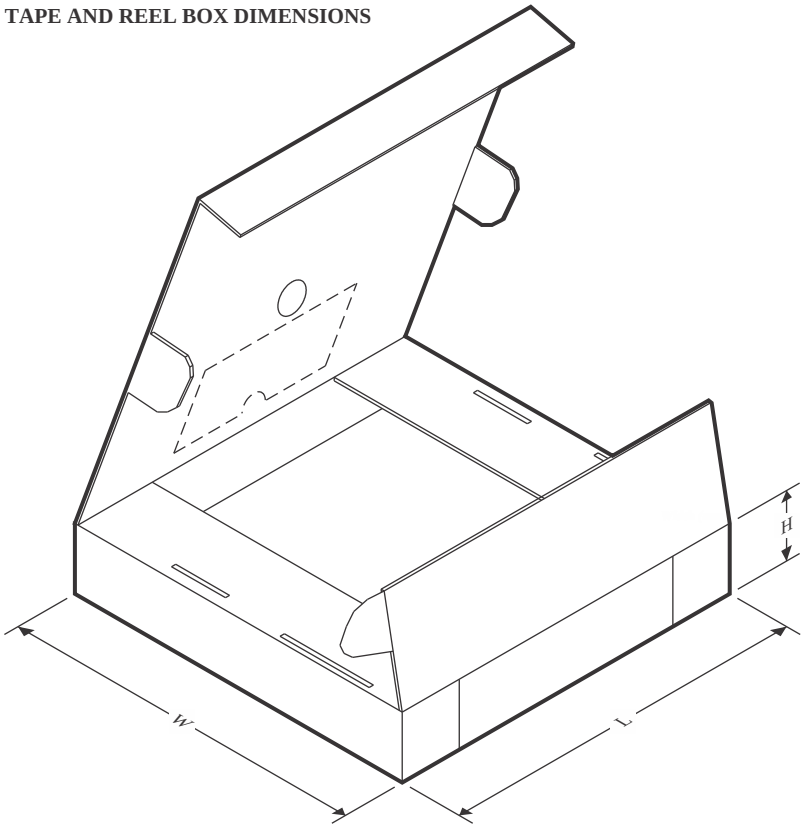
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61163YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

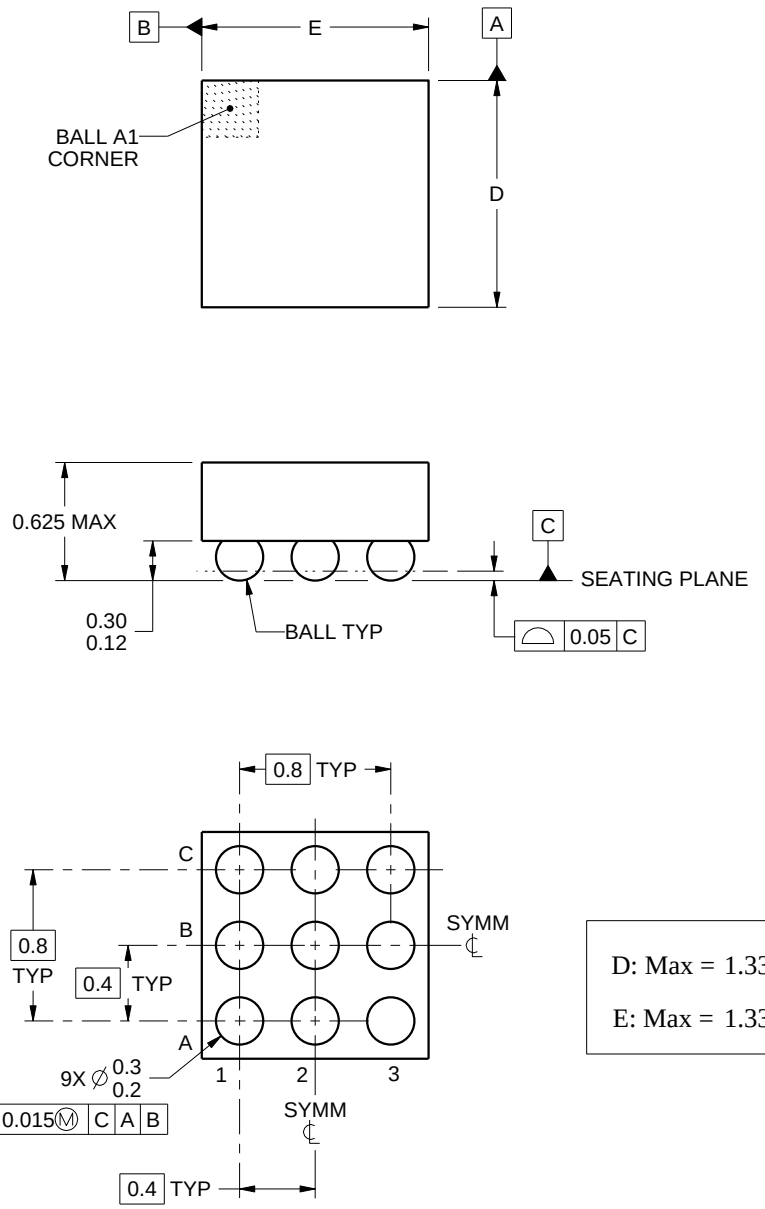
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61163YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.336 mm, Min =1.276 mm

E: Max = 1.336 mm, Min =1.276 mm

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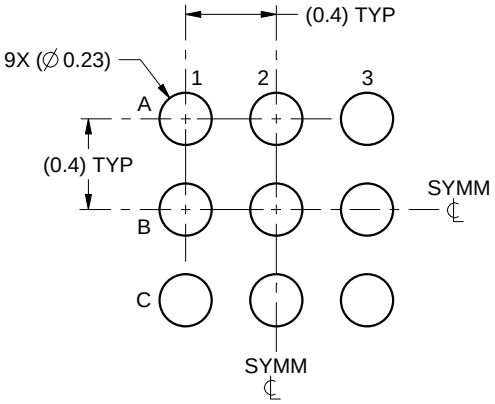
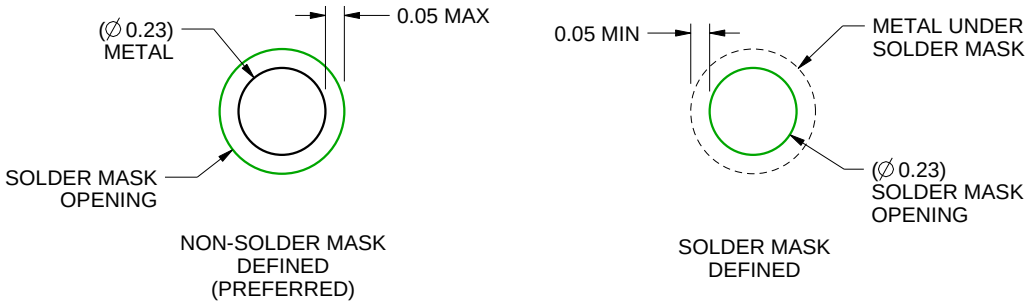
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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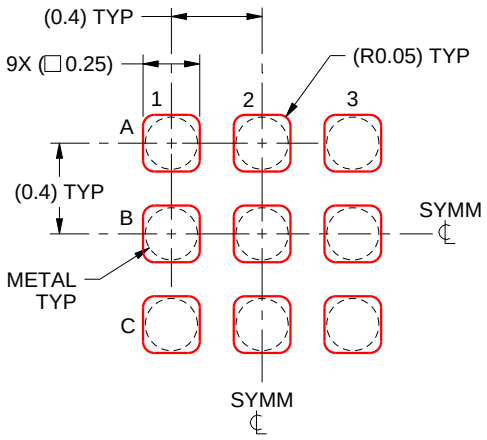
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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