National Semiconductor

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DS92UT16TUF
UTOPIA-LVDS Bridge for 1.6 Gbps Bi-directional Data Transfers

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1.0 General Description

The DS92UT16 is a flexible UTOPIA to LVDS Bridge device. The LVDS Bridge transparently transports the UTOPIA bus over a high speed LVDS serial link. The device includes many reliability features such as an optional 1:1 protection and built in bit error rate checking.

The parallel interface is user programmable for maximum flexibility. The user can choose between UTOPIA Level Level 2 ATM layer (master) of PHY layer (slave). The UTOPIA-LVDS Bridge supports a special MPHY (multi-PHY layer) operation mode. The MPHY operation supports up to 248 standard UTOPIA Level 2 PHY ports without adding external circuitry.

The serial interface uses LVDS Serializer and Deserializer technology. The 16:1 bit serialization allows conveying the full-duplex parallel bus over two differential transmission pairs. This enables low cost backplanes and cables. Cable transmission length can be as long 16 meters.

The serial link carries Flow control information (back pressure) in both directions. The Bridge device applies back pressure on a per queue basis over the 31 internal FIFO queues. In addition, the serial link includes an OAM (Operations and Maintenance) channel that does not detract from link performance.

There are many applications where the UTOPIA-LVDS Bridge simplifies designs. Box-to-box connections can use DS29UT16 devices across cables. Access multiplexor applications can use the devices across a PCB backplane for point-to-point and lightly loaded multidrop configurations.

2.0 Features

- 832 Mbps LVDS 16-bit serializer and deserializer interface
  - — Suitable for cable, printed circuit board, and backplane transmission paths
  - — 10m cable at max LVDS data rate and greater than 16m at min LVDS data rate
  - — Embedded clock with random data lock capability for clock recovery
  - — PRBS ($x^{31} + x^{28} + 1$) based LVDS link BER test facility
  - — Two independent LVDS receiver serial ports for optional 1:1 protection
  - — Main and redundant LVDS transmit ports
  - — Loop timing capability enables LVDS recovered clock to internally drive LVDS transmit clock
  - — Internal buffers allow maximum LVDS serial bit rate independent of UTOPIA clock rate
- Programmable UTOPIA interface
  - — UTOPIA Level 2 up to 52 MHz
  - — ATM layer or PHY layer interface
  - — ATM layer interface can support up to 248 standard Level 2 PHY ports with no additional external circuitry. Configured as 31 MPHY's, each with up to 8 sub-ports
  - — Supports extended cell size up to 64 bytes
  - — Supports 16- or 8-bit data buses with parity
- Embedded bidirectional, non-blocking flow control over serial link for per MPHY back pressure
- No external memories required
- Embedded OAM channel over serial link
  - — Remote Alarm/Status Indications
  - — Link Trace Label
  - — Embedded Control Channel with flow control for software communication
  - — BIP16 based error performance monitoring
  - — In protected systems, the standby link OAM channel is available for embedded communications and performance/alarm monitoring
- Multiple loop-back options
- Standard microprocessor interface (Intel and Motorola compatible)
- IEEE 1149.1 JTAG port
- Temperature range: –40˚C to +85˚C
- CMOS technology for low power
- LVDS transceiver section uses 3.3V power supply. Digital UTOPIA section uses 2.5V power supply. All I/O are 3.3V tolerant.
- 196 LBGA package, 15x15x1.37 mm, 1.0 mm ball pitch

3.0 Ordering Information

Order Number	Package Information	Package Number
DS92UT16TUF	196 LBGA package, 15x15x1.37 mm, 1.0 mm ball pitch	NUJB0196

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4.0 Block Diagram

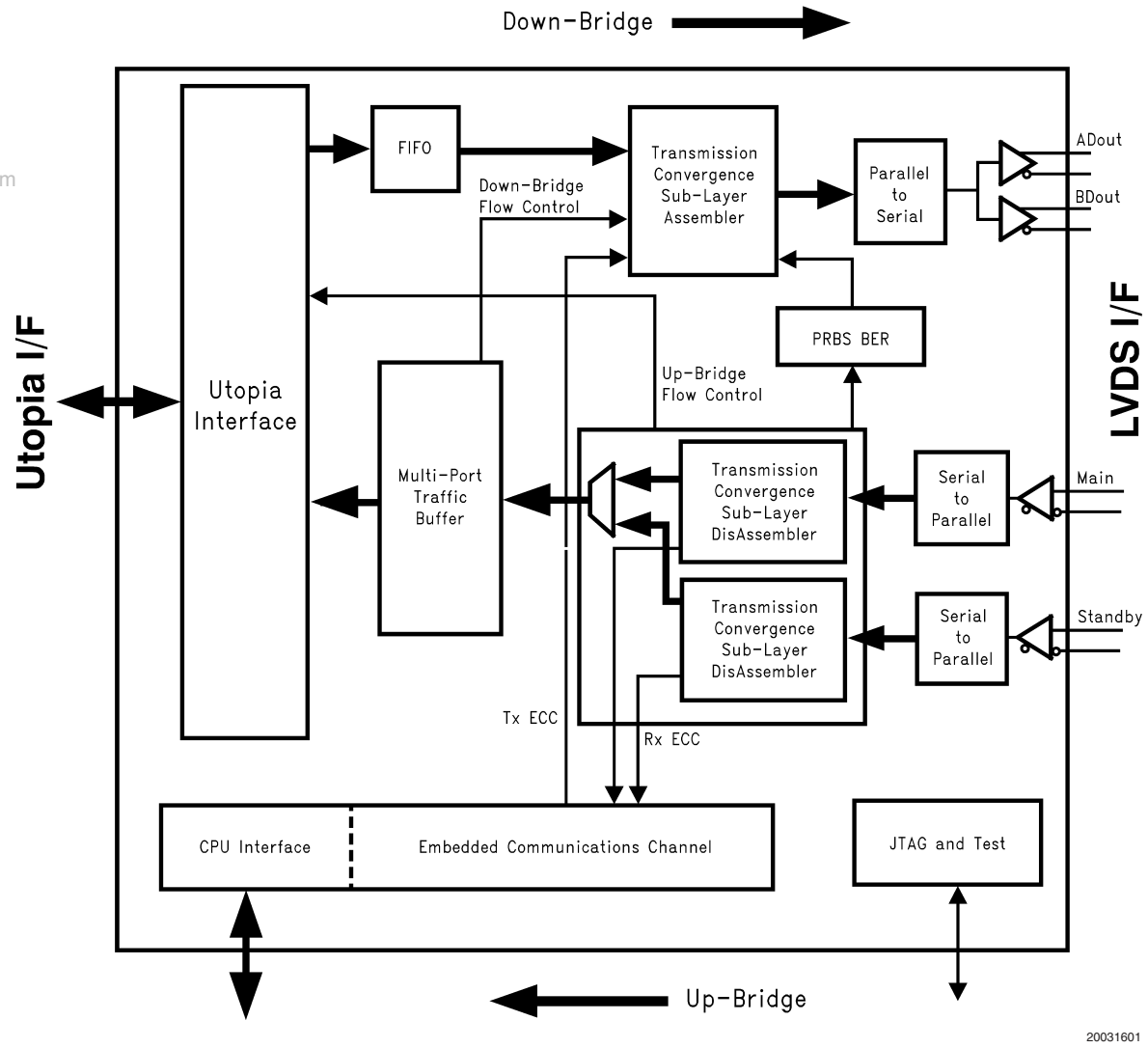

FIGURE 1. DS92UT16 Block Diagram

5.0 Application Overview

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5.0 Application Overview (Continued)

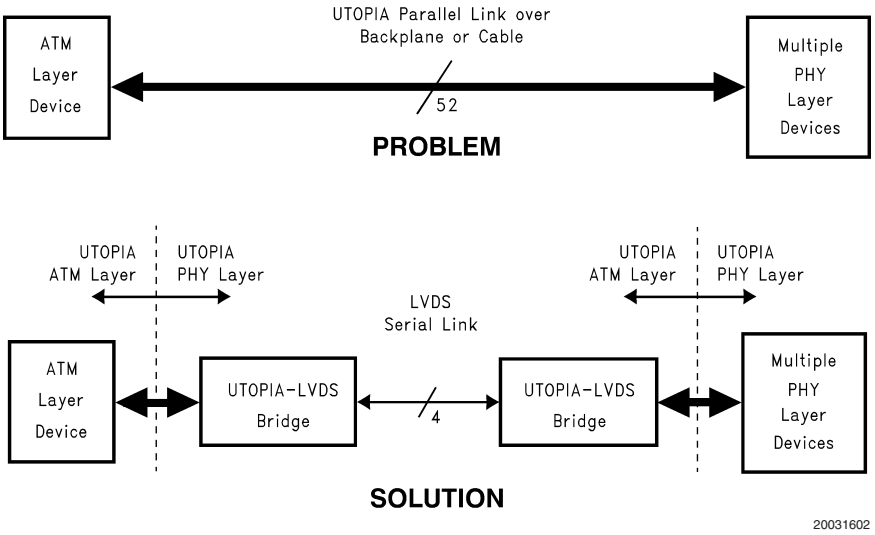

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FIGURE 2. Application Example

The UTOPIA interface [1. See *Section 21.0 References*] is an established standard for connecting Physical Layer devices to ATM Layer devices. However, when the ATM Layer device and the Physical Layer device(s) are on separate cards within a piece of equipment, or even on separate equipment, then the parallel nature of this standard becomes a limiting factor. See *Figure 2*.

The solution is to use the DS92UT16, which is a transparent bridge that extends the UTOPIA bus over a serial LVDS interface, and is suitable for backplanes and cables. Full bidirectional flow control is incorporated, allowing back-pressure to be applied to the source of the ATM cells. The 31 PHY ports available with standard UTOPIA Level 2 may be extended to 248 ports without additional external circuitry. The DS92UT16 achieves this by providing as many as 8 ENB and CLAV signals in both receive and transmit directions when acting as the ATM Layer device. This allows addressing 248 PHYs that are configured as up to 31 ports that each have as many as 8 sub-ports.

To aid equipment management and maintenance, the DS92UT16 passes an embedded 'Operations, Administration and Maintenance' (OAM) channel over the serial link. In addition, the device provides a number of loopback options that are both traffic affecting (line loopbacks) and non-traffic affecting (cell loopbacks), which simplify testing and diagnostic activities.

The DS92UT16 has a modified Bus LVDS serial output for driving cables in point-to-point applications. The cable length depends on the quality of the cable and the data rate. Increasing the cable quality, or lowering the LVDS data rate, increases the maximum possible cable length the device will drive.

When examining the trade-offs that determine the DS92UT16 maximum cable drive capability, it is important to understand that the LVDS data rate on the cable is 18 times (16 bits plus 2 embedded clock bits) the LVDS_TxClk rate. For example, a 35 MHz LVDS_TxClk will produce a 630 Mbps data rate, and a 52 MHz clock will produce a 936 Mbps data rate. When using twinaxial grade differential cable, the cable length can be as long as 16m for the 35 MHz clock and approximately 10m for the 52 MHz clock.

6.0 Functional Description

6.1 UTOPIA INTERFACE

The DS92UT16 has an industry standard UTOPIA interface [1.] supporting Level 2 and Extended Level 2 operation. Depending on its position in the bridge link, it may operate as either the ATM layer or the physical layer in the UTOPIA protocol.

In Level 2 mode, this interface can be either a 16-bit or an 8-bit wide data path, with both octet and cell level handshaking and operating at a frequency as high as 52 MHz, facilitating 622 Mbps (STM4/OC12) line rates.

In UTOPIA Level 2 mode, the device supports Multi-PHY (MPHY) operation, whereby up to 31 PHY ports may be connected to an ATM device. The presence of cells and availability of buffer space is indicated using the CLAV signals.

UTOPIA Level 2 defines 1 ENB and 1 CLAV signal in each direction. The DS92UT16 has extended this to 8 ENB and 8 CLAV signals, which enables up to 248 PHY ports to be connected to an ATM device without additional external circuitry as shown in *Figure 3*.

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6.0 Functional Description (Continued)

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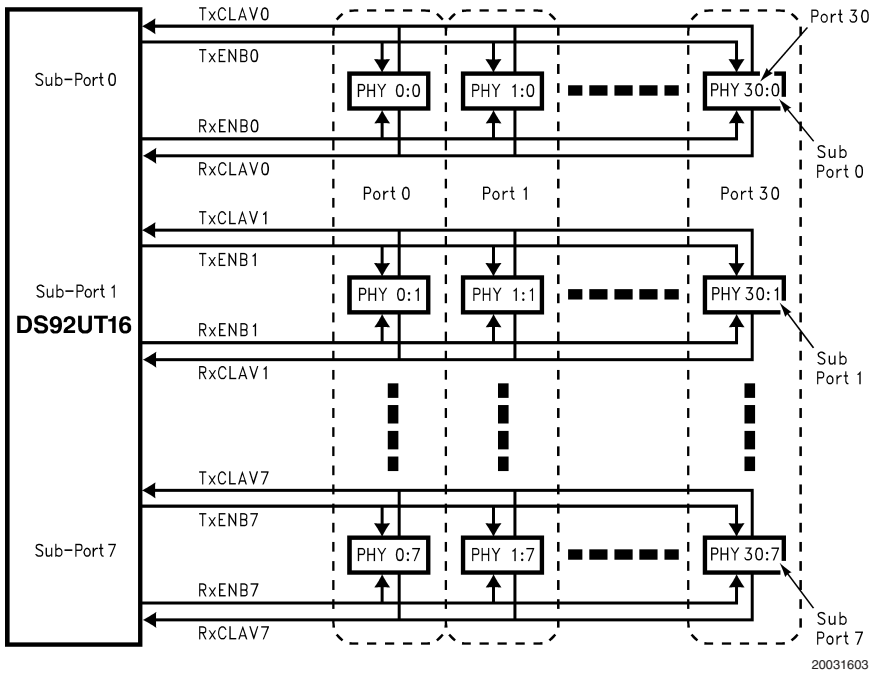

Note: The full connections for a single sub-port are shown in *Figure 4.*

FIGURE 3. Extended UTOPIA Level 2 for 248 PHY Ports

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6.0 Functional Description (Continued)

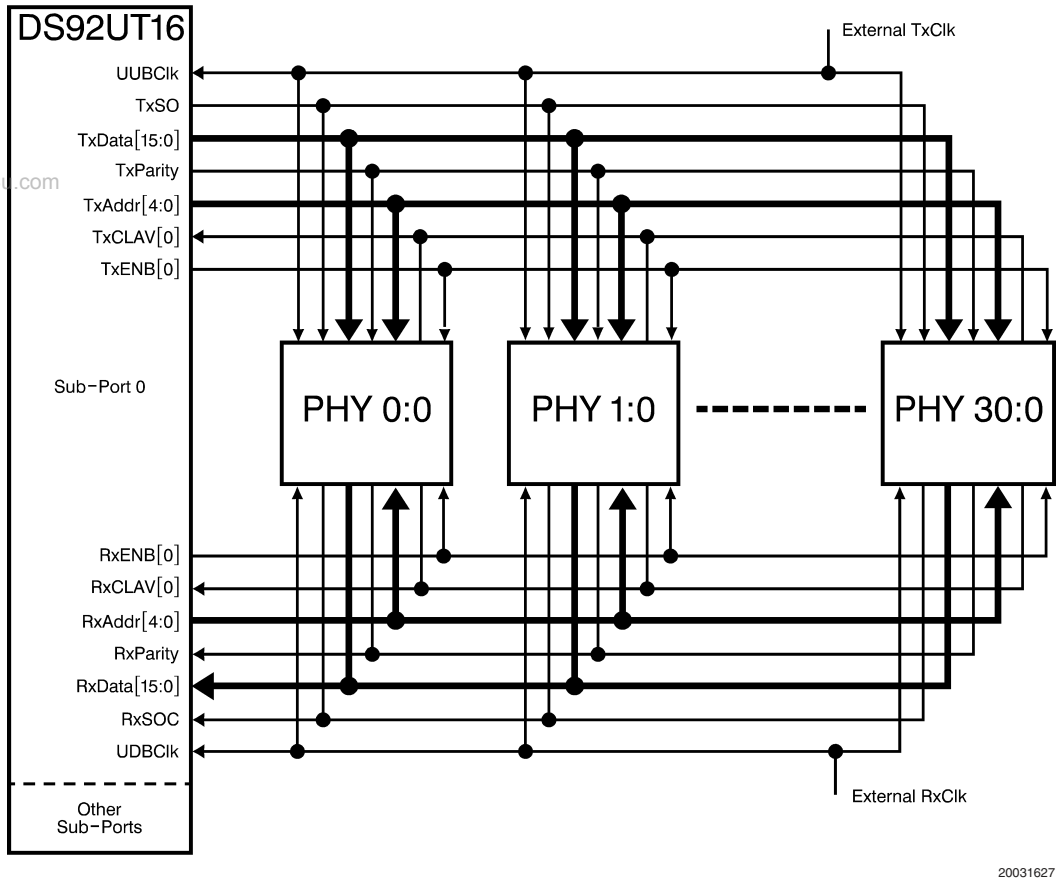

FIGURE 4. Detailed Connection of One Sub-Port for Extended UTOPIA Level 2

For the purposes of queueing, the 248 PHY ports are configured as sub-ports of the standard 31 ports so each port/queue has 8 sub-ports as discussed in *Section 6.2.2 Up-Bridge Multi-Port Traffic Buffer*. Each MPHY address corresponds to a port.

The 5 bit MPHY can address up to 31 PHY ports. At least 3 additional bits are required to give the total of 8 bits necessary for addressing 248 PHY ports. These additional address bits can be provided by the user in any of the User Prepend, Cell Header or UDF1/2 bytes of the cell as shown in *Figure 6*. The DS92UT16 is configured to extract/insert the extra address bits from/to any of these bytes.

PHY polling may be carried out as follows:

- Standard UTOPIA Level 2 with 1 CLAV signal.
  - — One CLAV polling 31 PHY ports.
- DS92UT16 Extended UTOPIA Level 2 with up to 8 CLAV signals.
  - — Each CLAV can poll 31 PHY ports giving a total of 248 PHY ports.

Multiple UTOPIA-LVDS bridge devices can be used in parallel to share up to 31 PHY ports among PHYs that are on separate line cards *Figure 5*. Each of these ports may have up to 8 sub-ports. There are constraints on the number of port addresses used per bridge in such a configuration. See *Section 9.2 MULTIPLE BRIDGE MTB CONFIGURATION*

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6.0 Functional Description (Continued)

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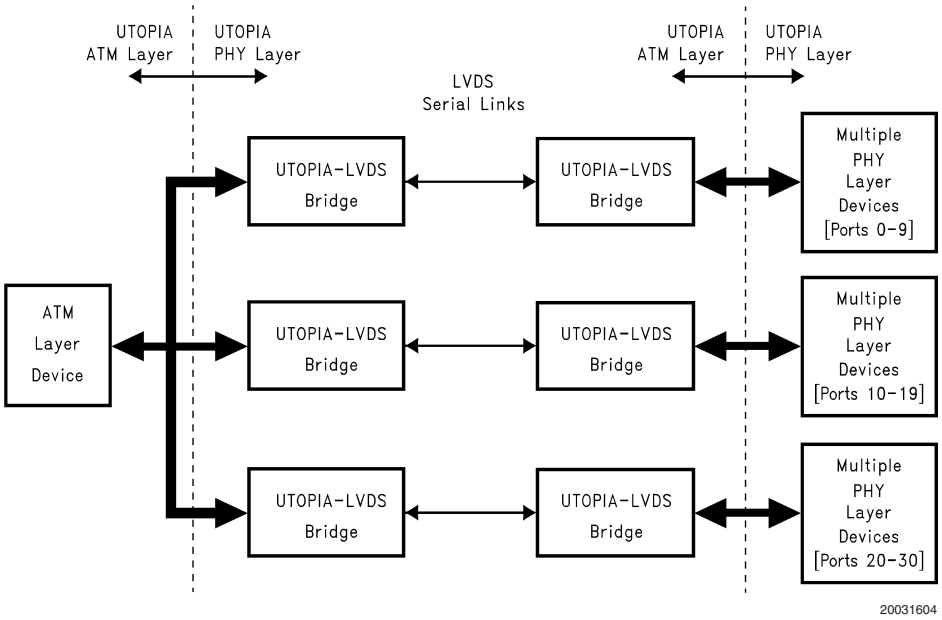

Note: Default MTB queue thresholds must be changed to use this configuration. See *Section 9.2 MULTIPLE BRIDGE MTB CONFIGURATION*

FIGURE 5. Multi-Bridge System Example

Parity generation and checking is available in all modes.

To support systems where routing tags and/or padding are added to the ATM cells at a previous device, the UTOPIA interface on DS92UT16 may be programmed to handle non-standard ATM cells of length 52 bytes up to 64 bytes. See *Figure 6*. In all cases, the Start Of Cell (SOC) signal must correspond to the first byte or word of the extended cell.

Back-to-back cell transfer is supported in all modes.

When configured as an ATM layer device, receive polling and transmit polling of those Ports with queued cells is Round-Robin. The DS92UT16 will only poll those PHY ports configured as active.

6.2 TRAFFIC BUFFERS

6.2.1 Down-Bridge FIFO

In the down-bridge direction, a simple 3 cell FIFO (with 30 cell overhead) is used to rate adapt the data from the UTOPIA clock domain to the LVDS clock domain for transmission. Per port queuing and back pressure/flow control is handled by the corresponding up-bridge Multi-port Traffic Buffer in the far end DS92UT16 device as described in *Section 6.2.2 Up-Bridge Multi-Port Traffic Buffer* and *Section 6.3.5 Flow Control*.

6.2.2 Up-Bridge Multi-Port Traffic Buffer

In the up-bridge direction, a 160 cell linked list buffer is shared across up to 31 port queues. This is called the Multi-port Traffic Buffer. Although each MPHY may be connected to 8 sub-ports/PHY's, the MTB has a single queue per MPHY port, as it only uses the 5-bit MPHY address and does not access the sub-port address bits.

Each port has a programmable upper fill threshold. In the up-bridge direction, queue overflow is avoided through the means of a per queue flow control protocol embedded in the LVDS link as described in *Section 6.3.5 Flow Control*. Should any queue reach this upper threshold, back-pressure is applied via the flow control mechanism over the serial link to the down-bridge (transmitting) device which uses the normal UTOPIA flow control handshaking to prevent any more cells being transferred and thus prevent overflow.

The individual queue per port architecture ensures that the flow control is non-blocking across the 31 ports. However, the 8 sub-ports within each port can be blocking.

Furthermore, as is the nature of link-list buffers, each queue may be over-assigned memory space, working on the assumption that not every queue will back up simultaneously. To accommodate the rare occasions where the buffer as a whole approaches full but individual queues are below their full threshold, the device also compares the overall buffer fill against a threshold. The flow control mechanism provides a global 'halt' command to ensure that no cells will be lost if the overall buffer should approach the overflow condition.

6.3 TRANSMISSION CONVERGENCE SUB-LAYER (TCS)

In the down-bridge direction, the Transmission Convergence Sub-layer (TCS) Assembler performs cell rate de-coupling. The TCS Assembler then prepares the cells for transport over the LVDS link by packaging them within link Transport Containers (TC).

In the up-bridge direction, the TCS Disassemblers unpack the link transport containers and route the cells to the Multi-port Traffic Buffer.

MPHY address, flow control, and OAM information is embedded within the link transport containers.

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6.0 Functional Description (Continued)

6.3.1 Cell Rate Decoupling

In the down-bridge direction, the TCS Assembler inserts idle cells when no valid traffic cells are available from the FIFO for onward transmission. In the up-bridge direction, the TCS Disassembler rejects all received idle cells.

6.3.2 Link Transport Container (TC)

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The ATM cells received on the UTOPIA interface can be standard or user-specified cells. Cell length is programmable from 52 to 64 bytes. These cells are treated as Protocol Data Units (PDU), which are packaged into Transport Containers (TC) for transmission over the serial link. In the reverse direction, the cell PDUs are unpacked from the link TCs before being passed out on the UTOPIA interface.

This is illustrated in *Figure 6*.

The PDU fields are configured as shown in *Table 1*. The total PDU cell length must be in the range of 52 to 64 bytes. In addition, variable length fields must be programmed to an even number of bytes because the DS92UT16 operates with an internal 16 bit data path. The total number of bytes defined for User Prepend plus UDF1/2 and User Append must not exceed 12 bytes to maintain the maximum PDU cell length of 64 bytes.

TABLE 1. PDU Cell Format Options

Field	Fixed/ Variable	Bytes
User Prepend	Variable	0, 2, 4, 6, 8, 10, 12
Cell Header	Fixed	4
UDF1/2	Variable (On/Off)	2, 0 in 16 bit mode 1, 0 in 8 bit mode
Payload	Fixed	48
User Append	Variable	0, 2, 4, 6, 8, 10, 12

Although the UDF1/2 bytes will always be present, the DS92UT16 can be programmed to either transport these bytes or ignore them. If they are to be ignored, then the TCS strips them out in the down-bridge direction and the UTOPIA up-bridge section inserts a HEC byte in UDF 1. Otherwise, they can be transported transparently the same as any other PDU byte.

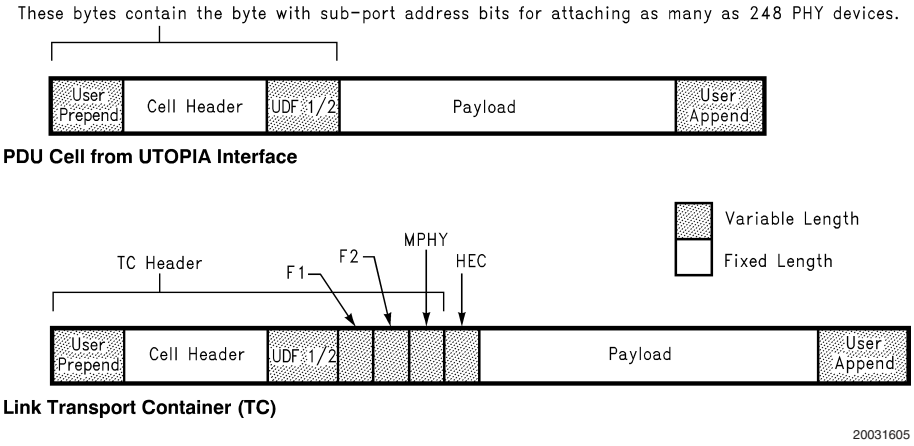

FIGURE 6. PDU and Link Transport Container Format

Each link TC has an MPHY address byte, two Flow Control (F) Channel bytes, and a HEC byte in addition to the PDU cell. The two F1 and F2 bytes per TC constitute the F Channel, which is used for flow control and OAM purposes over the link. The TCS uses the HEC byte for container delineation, frame delineation, and cell header error detection.

6.3.3 MPHY Tagging and Routing

In the down-bridge direction, the DS92UT16 adds an additional byte (MPHY byte) to each PDU. It contains the MPHY port address associated with that PDU, as shown in *Table 2*.

TABLE 2. MPHY Byte

Bit	7	6	5	4	3	2	1	0
Function	MPHY Port Address 0–31					Reserved		

At the other end of the link, this byte is used to route the incoming PDU from the LVDS interface to the appropriate MPHY port queue.

6.3.4 Transport Container Delineation and Error Monitoring

In the down-bridge direction, the device calculates and inserts the HEC byte using the CRC-8 polynomial $x^8 + x^2 + x + 1$ and optional coset $x^6 + x^4 + x^2 + 1$ defined in I.432.1 [2.]. The HEC byte is calculated over the preceding 7–19 bytes, which make up the link TC header. To aid delineation at the far end, the entire contents of the TC, excluding the HEC, are scrambled and the HEC is calculated on the scrambled TC header. A scrambler using the pseudo-random sequence polynomial $x^{31} + x^{28} + 1$ defined in I.432.1 [2.] is used.

In the up-bridge direction, the device determines the cell delineation within the received data by locking onto the HEC byte within the transport container, using the algorithm specified in I.432.1 [2.].

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6.0 Functional Description (Continued)

During normal operation in the up-bridge direction, the device monitors the HEC bytes for errors, with an option to reject cells containing errored HEC's. A performance metric on the number of errored cells detected is maintained.

Although the HEC byte normally over-writes the UDF1 byte before cells are passed out over a physical medium, the DS92UT16 has the option to retain the UDF1 and UDF2 information fields in order to provide a truly transparent UTOPIA bridge. If it is not necessary to pass the UDF1/2 bytes between the ATM and PHY devices at either end of the link, then the user has the option to suppress them to improve link efficiency.

Furthermore, in order to easily share-out the F Channel bandwidth between flow control and various OAM functions, the DS92UT16 uses a frame structure as shown in *Section 6.3.6 F Channel Byte Usage Within the Frame*. A frame contains 56 transport containers with ATM cells. The start of frame is indicated by the HEC byte of TC0, which has had the coset $x^6 + x^4 + x^2 + 1$ added to it. This differentiates the start of frame HEC from the normal cell HEC's.

6.3.5 Flow Control

The flow control mechanism within the DS92UT16 enables applying back-pressure to the source of the ATM cells in both directions. The flow control works independently per queue for all 31 queues. It uses a simple 'halt/send' command per PHY Port. At the destination buffer, the fill level of each Port queue is examined against a programmed threshold. Should the threshold be reached, a halt command is returned to the source, which prevents any more cells being sent to that Port until a 'send' command is subsequently received. Only the Port in question is affected, so this is a non-blocking protocol over the normal 31 Ports. However, the 8 sub-ports within a Port do not have individual flow control. This means a sub-port can block other sub-ports within that Port.

Since a regular flow control opportunity is provided via the F1/F2 bytes of the F Channel, only a small amount of headroom need be reserved to allow for latency in this protocol. Furthermore, should a number of PHY ports approach their limit simultaneously and/or the overall buffer approach a defined global threshold, a global halt may be issued, temporarily blocking all traffic.

The global halt/send command also allows the user to safely maximize the use of the shared buffer by over-assigning the memory among the Ports.

The flow control command is illustrated in *Table 3*. Each port is assigned a control bit in specified F-bytes within the frame structure, as shown in *Section 6.3.6 F Channel Byte Usage Within the Frame*. Within the F byte logic, 1 represents a 'halt' command to that port and logic 0 represents a 'send' command. A global halt is indicated by all ports containing a halt command. The msb of Flow Control 3 byte is reserved.

TABLE 3. Flow Control Coding Within the F Bytes

Flow Control 3		Flow Control 2	Flow Control 1	Flow Control 0
Res	Ports 30–24	Ports 23–16	Ports 15–8	Ports 7–0

6.3.6 F Channel Byte Usage Within the Frame

For the majority of time, the F Channel F1/F2 bytes are used as a flow control opportunity, providing a rapid throttle-back mechanism as described in *Section 6.3.5 Flow Control*. In addition, a small number of F bytes are stolen in a regular fashion to provide a low bandwidth OAM channel. This is controlled by the TC number within the frame, as illustrated in *Table 4*. Hence, an OAM channel is formed by the F1/F2 bytes in TCs 6, 13, 20, 27, 34, 41, 48 and 55, with the F1/F2 bytes in the remaining containers forming a flow control signalling channel.

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6.0 Functional Description (Continued)

TABLE 4. F Channel Byte Usage Within the Frame

TC0	TC1	TC2	TC3	TC4	TC5	TC6
Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Alarm/Sig.
Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Link Labels
TC7	**TC8**	**TC9**	**TC10**	**TC11**	**TC12**	**TC13**
Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	ECC1
Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	ECC2
TC14	**TC15**	**TC16**	**TC17**	**TC18**	**TC19**	**TC20**
Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	ECC3
Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	ECC4
TC21	**TC22**	**TC23**	**TC24**	**TC25**	**TC26**	**TC27**
Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	BIP16
Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	
TC28	**TC29**	**TC30**	**TC31**	**TC32**	**TC33**	**TC34**
Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Reserved
Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	
TC35	**TC36**	**TC37**	**TC38**	**TC39**	**TC40**	**TC41**
Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	ECC5
Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	ECC6
TC42	**TC43**	**TC44**	**TC45**	**TC46**	**TC47**	**TC48**
Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	ECC7
Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	ECC8
TC49	**TC50**	**TC51**	**TC52**	**TC53**	**TC54**	**TC55**
Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	Flow Control 3	Flow Control 1	BIP16
Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	Flow Control 2	Flow Control 0	

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6.3.7 OAM Channel

6.3.7.1 Remote Alarm and Signaling Byte

A byte-wide remote alarm and signaling channel is carried in the F1 byte in TC6 as shown in *Section 6.3.6 F Channel Byte Usage Within the Frame*. This provides a means for the device at the far end of the LVDS link to signal an alarm condition to the near end and vise-versa. This byte also contains the ECC flow control signals. The format of this byte is as shown below. Bit [0] is reserved.

TABLE 5. Remote Alarm and Signalling Byte

Bit	7	6	5	4	3	2	1	0
Function	RLOSA	RLOSB	RBA	RDSLL	EVN	ESSA	ESSB	Res

- RLOSA Remote Loss Of Signal lock at far end device receive port A.
- RLOSB Remote Loss Of Signal lock at far end device receive port B.
- RBA Remote far end device active receive port. Set = remote receive port B active and Clear = remote receive port A active.
- RDSLL Remote far end device active port Descrambler Loss of Lock. Set = Out of lock and Clear = In lock.
- EVN ECC Tx Data Valid/Null indication.
- ESSA ECC RxA Stop/Start indication.
- ESSB ECC RxB Stop/Send indication.

The status of the received RLOSA, RLOSB, RBA and RDSSL bits is reflected in the RARA register for receive port A and in RBRA for receive port B. See *Section 18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS—0x3C RARA* and *Section 18.52 RECEIVE PORT B REMOTE STATUS AND ALARMS—0x7C RBRA* for descriptions of these registers.

The function of the ECC signaling bits EVN, ESSA, and ESSB is described in *Section 16.0 Embedded Communication Channel Operation*.

6.3.7.2 Link Trace Label Byte

Also, in TC6 a byte-wide link trace label is carried in the F2 byte as shown in *Section 6.3.6 F Channel Byte Usage Within the Frame*. This allows the user to verify link connectivity, which is especially useful when a number of cable links are being used. The DS92UT16 may be programmed with both a link label value to transmit and an expected link label. Should the received link label not match the expected value, an alarm interrupt may be raised.

The received Link Label byte is software accessible and an interrupt may be raised on a change of received Link Label byte. So the Link Label byte may also be used as a user defined channel to pass one byte per frame across the link.

6.3.7.3 Embedded Communications Channel (ECC)

An Embedded Communications Channel is provided over the link for software messaging, download, etc. in the F1/F2 bytes of TCs 13, 20, 41 and 48 as shown in *Table 4*. The ECC byte contents are not processed by the DS92UT16. Hence the DS92UT16 is transparent to and does not restrict the system messaging protocol.

The ECC consists of an 8 byte Tx Buffer with corresponding Tx Buffer Ready and Tx Buffer Send flags, and an 8 byte Rx

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6.0 Functional Description (Continued)

Buffer with a corresponding Rx Buffer Full Flag. All bytes of the buffers are software read/write accessible. Tx Buffer Ready is read only.

At the ECC transmit side, the reset state sets the Tx Buffer Ready flag and clears the Tx Buffer Send flag. Then the software assembles a message for transmission in the Tx Buffer. To send a message, the software simply sets Tx Buffer Send, which automatically clears Tx Buffer Ready. The contents of the Tx Buffer are transmitted to the far-end. The Tx Buffer will automatically be retransmitted until the far-end indicates that it has been successfully received. When notified by the far end of successful reception, Tx Buffer Ready is set and an interrupt raised to the software to indicate successful transmission. A new message may now be assembled in the Tx Buffer and transmitted by setting Tx Buffer Send. As all the Tx Buffer bytes are read/write, the message to be transmitted can be assembled in any order and read back by the software before transmission. The same message can be retransmitted simply by setting Tx Buffer Send again.

At the ECC receive side, the reset state clears the Rx Buffer Full flag. When all 8 bytes of a message have been successfully received and stored in the Rx Buffer, the Rx Buffer Full flag is set and an interrupt raised. As all the Rx Buffer bytes are read/write, the message can be read in any order by the software. A new message will not overwrite the current received message until the Rx Buffer Full flag is cleared by the software indicating that the current Rx Buffer has been read and a new message can be received.

The ECC data flow is controlled across the link using the EVN, ESSA, and ESSB bits of the Remote Alarm and Signaling byte (*Section 6.3.7.1 Remote Alarm and Signaling Byte*).

As there are two independent LVDS receive ports, the DS92UT16 has two independent ECC receive sections. These are assigned to the LVDS receive ports Port A and Port B. The ECC of the standby link may therefore be used for software communication.

Section 16.0 Embedded Communication Channel Operation describes the operation and control of the ECC in detail.

6.3.7.4 BIP16

A Bit-Interleaved-Parity mechanism provides a live error performance metric on the LVDS link. A BIP16 value is calculated over a previous block of 28 containers and inserted in the F1/F2 bytes of containers 27 and 55, as shown in *Section 6.3.6 F Channel Byte Usage Within the Frame*. At the far end, the re-calculated BIP16 values are compared against the received values. Any bit errors in this comparison are counted. Should the number of errors exceed a programmed threshold, then an interrupt may be raised.

6.3.7.5 F Channel (Flow Control and OAM) Bandwidth Analysis

This section analyses the bandwidth used by the various components of the F Channel. The figures are dependent upon the link bandwidth and the size of the PDU/ATM cells being carried in the Transport Containers. This illustration is restricted to 800 Mbps and PDU sizes of 52 and 64 bytes. By adding the 4 bytes for the F Channel, the TCs are then 56 and 68 bytes respectively.

Table 6 illustrates the number of bytes used for each function in the F Channel. The top row gives the total number of Transport Containers per Frame as 56. It then shows the number of bytes in each Frame for OAM and Flow Control. There is a total of 112 bytes in each Frame for the F Channel.

Table 7 shows the bit rate used by each portion of the F Channel. The larger 68 byte container uses a lower proportion of the channel bandwidth for F Channel functions.

Table 8 shows the percentage of the channel bandwidth used for each of the functions. The total F Channel bandwidth is only 3.57% of total bandwidth even with the smaller container size.

TABLE 6. F Channel Bandwidth — Bytes

Number of Transport Containers in Frame (8 rows x 7 columns)	56
Bytes per Frame for Remote Alarms and Signalling	1
Bytes per Frame for Link Label	1
Bytes per Frame for ECC	8
Bytes per Frame Reserved	2
Bytes per Frame for BIP16	4
Bytes per Frame for OAM	16
Bytes per Frame for Flow Control	96
Bytes per Frame for F Channel	112

TABLE 7. F Channel Bandwidth — Mbps

Link BW - Mbps	800	800
Container Size - Bytes	56	68
Remote Alarm BW - Mbps	0.26	0.21
Link Label BW - Mbps	0.26	0.21
ECC BW - Mbps	2.04	1.68
Reserved BW - Mbps	0.51	0.42
BIP16 BW - Mbps	1.02	0.84
OAM BW - Mbps	4.08	3.36
Flow Control BW - Mbps	24.49	20.17
F Channel BW - Mbps	28.57	23.53

TABLE 8. F Channel Bandwidth — Percentage

Link BW - Mbps	800	800
Container Size - Bytes	56	68
Remote Alarm BW%	0.03	0.03
Link Label BW%	0.03	0.03
ECC BW%	0.26	0.21
Reserved BW%	0.06	0.05
BIP16 BW%	0.13	0.10
OAM BW%	0.51	0.42
Flow Control BW%	3.06	2.52
F Channel BW%	3.57	2.94

6.4 LVDS PHYSICAL INTERFACE

The DS92UT16 provides one dual transmit and two independent receive high speed LVDS serial interfaces with 800 Mbps bandwidth. The LVDS Interface transmits and receives data over lightly loaded backplanes or up to 10m of cable. The single transmit block drives two pairs of differen-

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6.0 Functional Description (Continued)

tial outputs with independent TRI-STATE® controls for each. The same data is transmitted over both pairs of transmit pins. The two serial receive interfaces are completely separate and independent and are denoted Port A and Port B. Only one receive port is selected for traffic at any one time. This is designated the Active Port. The Standby receive port may be powered down. Alternatively, the Standby receive port's OAM channel can be made available for software communications using the ECC, and for link performance monitoring. This allows the condition of the Standby link to be determined. The LOCK status of both Active and Standby ports is monitored automatically.

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The transmitted data stream contains embedded clock information. The receiver's clock recovery circuit locks onto the embedded clock in either a random data pattern, or by instructing the transmitter to send SYNCH patterns. The DS92LV16 can send SYNCH patterns on power-up or when synchronization is lost. The latter option requires a feedback loop in either hardware or software between the transmitter and the receiver, but has the benefit of a faster lock time. The LOCK status of both receive ports is reflected on external pins and alarm/status bits that are readable via the microprocessor port. The LOCK status, along with the currently active port, is transmitted to the far-end receiver via the Remote Alarm and Signalling byte of the OAM channel as described in *Section 6.3.7.1 Remote Alarm and Signaling Byte*. The recovered clocks of both receive ports are available on external pins.

A Loop Timing option is available whereby the LVDS transmit clock can be sourced directly from the recovered clock of the active receiver, rather than from the external transmit clock input pin.

The transmit port and two receive ports may be independently powered down via microprocessor control. Similarly, the device may be forced to send SYNCH patterns on the transmit port via microprocessor control.

To assist in designer testing and system commissioning of the LVDS interface, the DS92UT16 has a built in BER test facility. The device may be configured to send a PRBS pattern in place of ATM cells. At the receiver, the device locks onto this PRBS pattern and provides an error metric.

6.5 CPU INTERFACE

The DS92UT16 contains a flexible microprocessor port capable of interfacing to any common system processor. Via this port, the system software can customize the behavior of the device from the various options provided, monitor the system performance, and activate diagnostic facilities such as loop-backs and LVDS BER testing.

In addition to an 8-bit address and 8-bit data bus plus the associated bus protocol control signals, the port includes an open-drain interrupt signal. The device may assert this signal on the detection of various alarms within the device, such as excessive HEC errors, ECC buffer full/empty, loss of lock etc. Any of the potential internal sources of this interrupt may be inhibited individually via an interrupt mask.

A software lock mechanism is implemented to prevent spurious modification of some of the DS92UT16 software accessible registers. A predefined UNLOCK write sequence is necessary to allow unrestricted software write access to the DS92UT16. A corresponding LOCK write sequence will prevent any software write access to the these registers. Read access is unrestricted except as noted in the next paragraph. See *Table 9* for the LOCK and UNLOCK sequences. Only device configuration registers such as PDU cell length, UTOPIA interface mode, etc. are protected in this way. All other registers associated with the ECC, performance monitoring and interrupts are always write accessible by the software except as noted in next paragraph. See *Section 18.1 SOFTWARE LOCK — 0x00 to 0x01 SLK0 to SLK1*.

TABLE 9. Software Lock Sequences

Meaning	Sequence	Address	Data
Unlock Sequence	1st write	0x00	0x00
	2nd write	0x01	0xFF
LOCK Sequence	1st write	0x00	0xDE
	2nd write	0x01	0xAD

Powering down a Receive Port inhibits access to the associated registers. This feature saves power when a Receive Port is not in use. It allows re-reading the last value read from a register associated with that Receive Port and disallows writing to registers. Receive Port A (RxA) in Power-down mode inhibits access to registers described in *Section 18.21 RECEIVE PORT A LINK LABEL — 0x20 RALL* to *Section 18.39 RECEIVE PORT A BIT ERROR COUNT — 0x43 to 0x45 RABEC2 to RABEC0*. Receive Port B (RxB) in Power-down mode inhibits access to registers described in *Section 18.40 RECEIVE PORT B LINK LABEL — 0x60 RBLL* to *Section 18.58 RECEIVE PORT B BIT ERROR COUNT — 0x83 to 0x85 RBBEC2 to RBBEC0*. The contents of these registers are not lost or altered in Power-down mode.

6.6 PERFORMANCE MONITORING AND ALARMS

The DS92UT16 provides a number of performance metrics and alarms to assist in equipment/network management. The programmer can independently enable or disable these alarms to raise an interrupt. See *Section 14.0 Performance Monitoring* for a detailed description of the Performance Monitoring and General Alarms.

6.7 TEST INTERFACE

The IEEE 1149.1 JTAG [4.] port on the device provides access to the built-in test features such as boundary SCAN, Internal SCAN and RAM BIST. It may be used to test the device individually or as part of a more comprehensive circuit board or system test. (NOTE: The internal SCAN and RAM BIST functions are not intended for user access. Therefore, the device user should never assert the Test_se pin.)

6.8 LOOPBACKS

To assist in diagnostic testing, the device provides both LVDS interface loopbacks and ATM cell loopbacks. The former is suitable for designer or commission testing when the device is not passing live traffic. The latter allows cell trace testing on live traffic. The ATM cell loopback operates by recognizing the user-defined cell header of the special loopback cells. The available loopback options are shown in *Table 10*.

In addition to providing a live round trip test via the cell loopbacks, the DS92UT16 helps pinpoint failures between transmit and receive paths by counting the number of loopback cells received.

All loopbacks are programmable via the microprocessor interface.

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6.0 Functional Description (Continued)

TABLE 10. Loopback Options

LineLB_LVDS	Physical loopback at the LVDS interface. Loop entering LVDS traffic back out of the device.
LocalLB_LVDS	Physical loopback at the LVDS interface. Loop exiting LVDS traffic back into the device.
Up2Down_ATM	ATM loopback. Route defined cell entering the device at the LVDS interface back out.
Down2Up_ATM	ATM loopback. Route defined cell entering the device at the UTOPIA interface back out.

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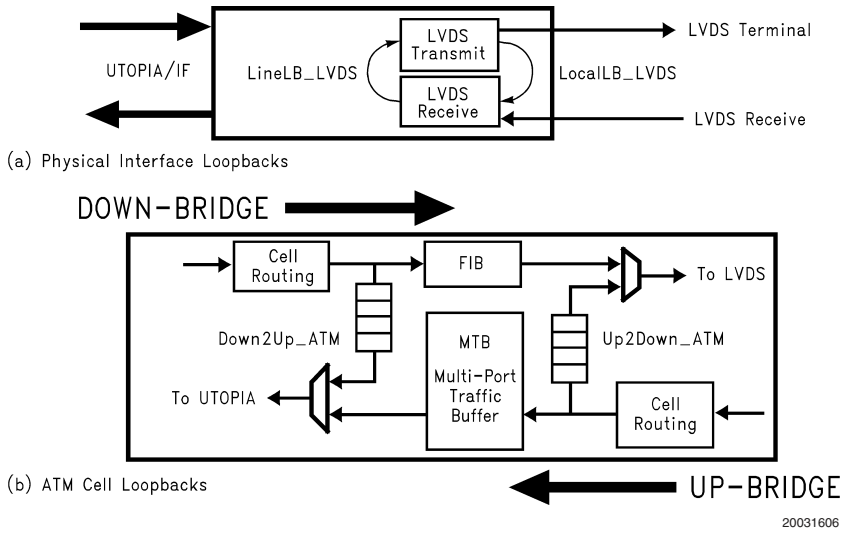

FIGURE 7. LVDS Interface and ATM Cell Loopback Options

7.0 Signal Description

Package ball assignment in *Section 20.0 Package*

TABLE 11. Pin Description

Signal Name	Description	Width	Signal Type	Polarity	Internal Bias
UTOPIA INTERFACE					
U_TxData [15:0]	Transmit toward the PHY Layer data bus.	16	BiDir (Note 2)		
U_TxParity	Transmit data bus parity bit. (odd parity)	1	BiDir (Note 2)		
U_TxCLAV [7:1]	Transmit cell available - Extended.	7	Input (Note 3)	Active High	Pull Down
U_TxCLAV [0]	Transmit cell available - Normal/Extended.	1	BiDir (Note 1)	Active High	Pull Down
U_TxENB [7:1]	Enable Data transfers - Extended.	7	Output (Note 3)	Active Low	
U_TxENB [0]	Enable Data transfers - Normal/Extended.	1	BiDir (Note 2)	Active Low	
U_TxSOC	Transmit Start Of Cell.	1	BiDir (Note 2)	Active High	
U_TxAddr [4:0]	Address of MPHY device being selected.	5	BiDir (Note 2)		
U_RxData [15:0]	Receive from the PHY Layer data bus.	16	BiDir (Note 1)		
U_RxParity	Receive data bus parity bit. (odd parity)	1	BiDir (Note 1)		
U_RxCLAV [7:1]	Receive cell available - Extended.	7	Input (Note 3)	Active High	Pull Down
U_RxCLAV [0]	Receive cell available - Normal/Extended.	1	BiDir (Note 1)	Active High	Pull Down
U_RxENB [7:1]	Enable Data transfers - Extended.	7	Output (Note 3)	Active Low	
U_RxENB [0]	Enable Data transfers - Normal/Extended.	1	BiDir (Note 2)	Active Low	
U_RxSOC	Receive Start Of Cell.	1	BiDir (Note 1)	Active High	
U_RxAddr [4:0]	Address of MPHY device being selected.	5	BiDir (Note 2)		
U_UDBClk	UTOPIA Down Bridge - Input transfer clock.	1	Input (Note 4)		
U_UUBClk	UTOPIA Up Bridge - Output transfer clock.	1	Input (Note 5)		

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7.0 Signal Description (Continued)

TABLE 11. Pin Description (Continued)

Signal Name	Description	Width	Signal Type	Polarity	Internal Bias
LVDS INTERFACE					
LVDS_ADout[+,–]	A Serial data differential outputs.	2	Output		
LVDS_BDout[+,–]	B Serial data differential outputs.	2	Output		
LVDS_ADenb	Serial transmit data A output enable.	1	Input	Active High	Pull Up
LVDS_BDenb	Serial transmit data B output enable.	1	Input	Active High	Pull Up
LVDS_Synch	External control to transmit SYNCH patterns on serial interface.	1	Input	Active High	Pull Down
LVDS_TxClk	Transmit clock.	1	Input		
LVDS_TxPwdn	Transmit section power down	1	Input	Active Low	Pull Up
LVDS_ADin[+,–]	PortA Serial data differential inputs.	2	Input		
LVDS_ALock_n	PortA Clock recovery lock status	1	Output		
LVDS_ARxClk	PortA Recovered clock.	1	Output		
LVDS_ARefClk	PortA Reference clock for receive PLLs.	1	Input		
LVDS_APwdn	PortA Power Down.	1	Input	Active Low	Pull Up
LVDS_BDin[+,–]	PortB Serial data differential inputs.	2	Input		
LVDS_Block_n	PortB Clock recovery lock status.	1	Output		
LVDS_BRxClk	PortB Recovered clock.	1	Output		
LVDS_BRefClk	PortB Reference clock for receive PLLs.	1	Input		
LVDS_BPwdn	PortB Power Down.	1	Input	Active Low	Pull Up
CPU & GENERAL CONTROL					
CPU_cs	Select signal used to validate the address bus for read and write data transfers.	1	Input	Active Low	
CPU_rd (CPU_ds)	Read or Data Strobe, depending on CPU_BusMode.	1	Input	Active Low	
CPU_wr (CPU_rnw)	Write or Read/Write, depending on CPU_BusMode.	1	Input	Active Low (Write)	
CPU_int	Interrupt request line.	1	Output	Active Low	Open Drain
CPU_Data[7:0]	Data bus.	8	BiDir		
CPU_Addr[7:0]	Address bus.	8	Input		
CPU_BusMode	Mode select for bus protocol.	1	Input		Pull Down
GPIO [3:0]	General Purpose Input/Output.	4	BiDir		
Reset_n	Reset min pulse is 2X slowest clock period.	1	Input	Active Low	Pull Up
JTAG TEST INTERFACE					
JTAG_CLK	Test clock.	1	Input		
JTAG_Reset	Test circuit reset.	1	Input	Active Low	Pull Up
JTAG_TMS	Test Mode Select.	1	Input		Pull Up
JTAG_TDI	Test Data In.	1	Input		
JTAG_TDO	Test Data Out.	1	Output		
Test_se	SCAN enable (for manufacturing test only)	1	Input	Active High	Pull Down
TOTAL PIN COUNT					
Total Functional I/O		133			
LVDS V_{DD}/V_{SS}	3.3V LVDS power for analog and digital	46			
CV_{DD}/CV_{SS}	2.5V Core Power for digital functions	6			
IOV_{DD}/IOV_{SS}	3.3V I/O power ring	8			
Total Power		60			
No Connect	No signal connected to this pin	3			
Total Pins	196 LBGA, 15x15 mm, 1.0 mm ball pitch	196			

Note 1: These pins are Inputs in ATM Layer mode and Outputs PHY Layer mode

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7.0 Signal Description (Continued)

TABLE 11. Pin Description (Continued)

Note 2: These pins are Outputs in ATM Layer mode and Inputs PHY Layer mode.

Note 3: These pins are only used in PHY layer mode, Extended 248 PHY mode. In Normal 31 PHY mode or ATM layer mode, they **must be** unconnected.

Note 4: In PHY layer mode this is the Utopia TxClk and in ATM layer mode this is the Utopia RxClk.

Note 5: In PHY layer mode this is the Utopia RxClk and in ATM layer mode this is the Utopia TxClk.

8.0 UTOPIA Interface Operation

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This section describes the operation of the UTOPIA Interface of the DS92UT16. The UTOPIA interface mode of operation is defined in the UTOPIA Configuration (UCFG) register described in *Section 18.59 UTOPIA CONFIGURATION—0xA0 UCFG*. The format of the PDU cells carried over this interface is defined in the PDU Configuration (PDUCFG) register described in *Section 18.5 PDU CONFIGURATION—0x05 PDUCFG*.

The interface can operate in ATM layer mode or PHY layer mode. When operating as a Level 2 ATM layer interface, the protocol can be extended to cope with up to 248 PHY ports rather than the maximum 31 allowed by the standard Level 2 definition. This Extended Level 2 mode is achieved with eight CLAV and eight ENB signals.

On power up the device defaults to ATM layer mode. To prevent potential contention on the Utopia interface signals, all the Utopia pins which are bidirectional are configured as outputs in tri-state mode and the Utopia interface block is disabled. The user must select the device operating mode, ATM layer or PHY layer, by writing the appropriate value to the UMODE bit of the UCFG register before enabling the Utopia interface block and releasing the Utopia interface pins. Enabling the Utopia interface and releasing the Utopia pins is achieved by setting the UBDEN bit of the UCFG register.

8.1 UTOPIA BASIC LEVEL 2 MODE - 31 PORTS (Default Mode)

In UTOPIA Level 2 mode:

- 8-bit or 16-bit data buses are controlled by the BWIDTH bit of the UCFG register. In 8-bit mode only U_TxData[7:0] and U_RxData[7:0] are valid; parity is calculated and checked only over these bits of the data buses and the upper bits of the data buses are not used. In 16-bit mode of the full U_TxData[15:0] and U_RxData[15:0] are valid and parity is calculated over all bits of the data buses.
- One ATM Layer can communicate with up to 31 PHY ports using the MPhy address busses U_TxAddr[4:0] and U_RxAddr[4:0] and the control signals U_TxCLAV[0], U_RxCLAV[0], U_TxENB[0] and U_RxENB[0].
- U_TxCLAV[7:1], U_RxCLAV[7:1], U_TxENB[7:1] and U_RxENB[7:1] are not used.
- All Queues from 30 to 0 of the MTB may be used. There is one queue for each MPhy address so the use of the queues will depend on the connected ports list defined by the UCPL3–UCPL0 registers.
- Uses the connected ports list defined by the UCPL3-UCPL0 registers. In ATM mode, these registers are used to determine the ports that should be polled. In PHY mode, these registers are used to determine which MPhy addresses the device should respond to during polling.
- The connected sub-port list defined in the UCSPL register is not used.
- The sub-port address location defined by USPAL and USPAM registers is not used.
- The CLAV mode bits CLVM[1:0] of the UCFG register should be defined as CLVM[1:0] = 00.

The configuration of the inputs/outputs of the UTOPIA Level 2 interface for ATM Layer mode and PHY Layer mode is shown in *Figure 8*. The main difference is that in ATM mode the CLAV pins are inputs and the MPhy Address and ENB pins are outputs; whereas in PHY mode, the CLAV pins are outputs and the MPhy Address and ENB pins are inputs.

Note that in ATM Layer mode the DS92UT16 does not generate the UTOPIA clocks and must be supplied with these clocks just as in PHY mode.

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8.0 UTOPIA Interface Operation (Continued)

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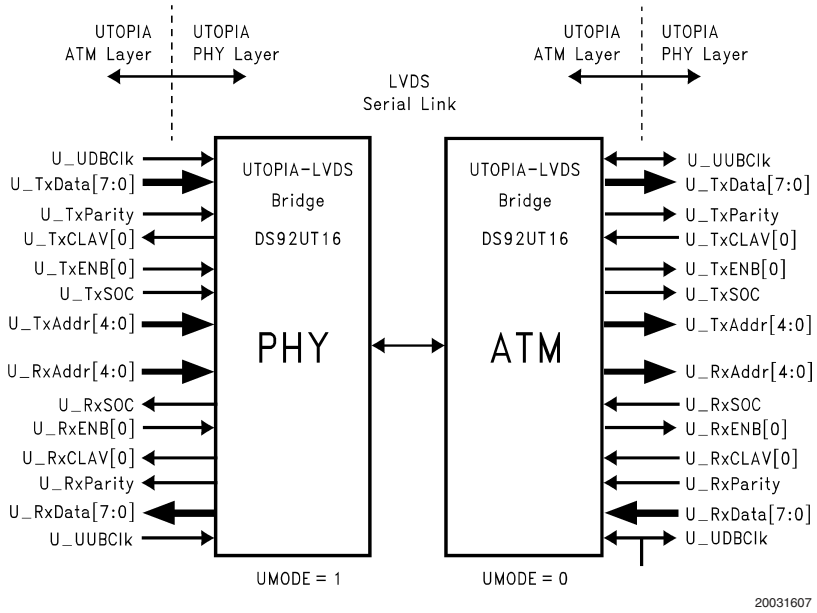

FIGURE 8. Basic UTOPIA Level 2 UMODE Configuration

8.1.1 ATM Polling

When configured as an ATM Layer device, the DS92UT16 polls the connected PHY ports using the MPhy address busses U_TxAddr and U_RxAddr. Only those ports which are connected will be polled. The connected ports list defined in the UCPL3–UCPL0 registers is used to determine which ports are connected. The PHY ports respond only on U_TxCLAV[0] and U_RxCLAV[0]. On reset the UCPL3–UCPL0 registers are all set to 0xFF so the DS92UT16 will poll all ports.

8.1.2 PHY Polling

When configured as a PHY Layer device the DS92UT16 is polled by the connected ATM device. During polling the DS92UT16 will only respond to MPhy addresses, on U_TxAddr and U_RxAddr, which are defined as connected. The connected ports list defined in the UCPL3–UCPL0 registers is used to determine which ports are connected. On reset the UCPL3–UCPL0 registers are all set to 0xFF so the DS92UT16 will respond to all MPhy addresses during polling. The DS92UT16 responds only on U_TxCLAV[0] and U_RxCLAV[0].

NOTE: There must always be at least one connected port defined in the UCPL3–UCPL0 registers. If no ports are to be connected then use Configuration Traffic Inhibit mode described in *Section 10.0 Configuration and Traffic Inhibit Operation*.

8.2 UTOPIA EXTENDED LEVEL 2 MODE - 248 PORTS

In UTOPIA Extended Level 2 mode:

- 8-bit or 16-bit data buses are controlled by the BWIDTH bit of the UCFG register. In 8-bit mode, only U_TxData[7:0] and U_RxData[7:0] are valid; parity is calculated and checked only over these bits of the data buses. In 16-bit mode, the full U_TxData[15:0] and U_RxData[15:0] are valid; parity is calculated and checked over all bits of the data buses.
- In ATM mode, the DS92UT16 can communicate with up to 248 PHY ports using the MPhy address busses U_TxAddr[4:0] and U_RxAddr[4:0], and the control signals U_TxCLAV[7:0], U_RxCLAV[7:0], U_TxENB[7:0] and U_RxENB[7:0]. In PHY mode, the DS92UT16 behaves as a standard Level 2 device and only 31 ports are needed using the MPhy address busses U_TxAddr[4:0] and U_RxAddr[4:0], and the control signals U_TxCLAV[0], U_RxCLAV[0], U_TxENB[0] and U_RxENB[0].
- All Queues from 30 to 0 of the MTB may be used. There is one queue for each MPhy address so the use of the queues will depend on the connected ports list defined by the UCPL3–UCPL0 registers.
- The connected ports list defined by the UCPL3–UCPL0 registers and the connected sub-port list defined in the UCSPL register are used. In ATM mode, these registers are used to determine which ports should be polled. In PHY mode, these registers are used to determine which MPhy addresses the device should respond to during polling.
- The sub-port address location defined by USPAL and USPAM registers is used in ATM mode to determine the location of the 3-bit sub-port address in the PDU cell. In PHY mode these registers are not used.
- The CLAV mode bits CLVM[1:0] of the UCFG register should be defined as CLVM[1:0] = 11.

The configuration of the inputs/outputs of the UTOPIA Level 2 interface for ATM Layer mode and PHY Layer mode is shown in *Figure 9*.

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8.0 UTOPIA Interface Operation (Continued)

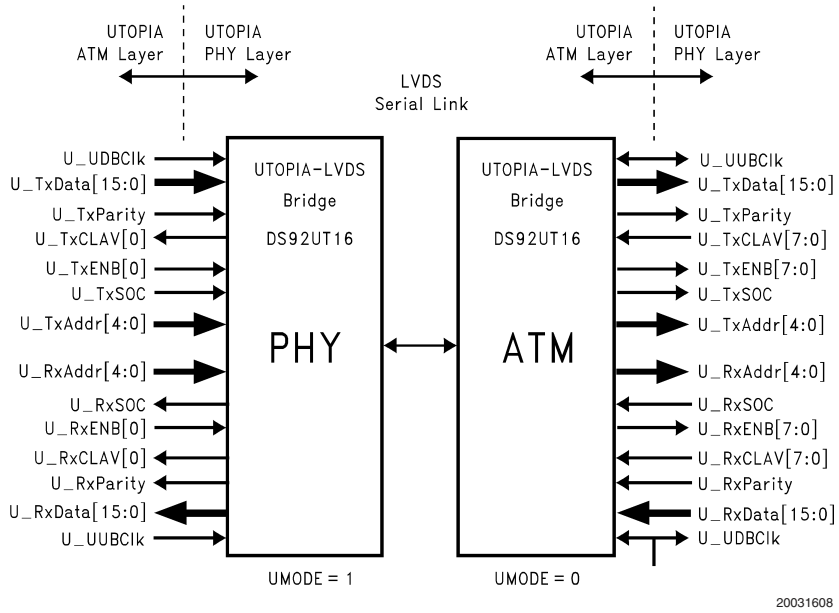

FIGURE 9. Extended UTOPIA Level 2 UMODE Configuration

The main difference is that in ATM mode the CLAV pins are inputs and the MPhy Address and ENB pins are outputs, whereas in PHY mode the CLAV pins are outputs and the MPhy Address and ENB pins are inputs. Also, in ATM mode all eight CLAV and ENB pins are used, but in PHY mode only one of the CLAV and ENB pins are used.

Note that in ATM Layer mode the DS92UT16 does not generate the UTOPIA clocks but must be supplied with these clocks just as in PHY mode.

8.2.1 ATM Polling

When configured as an ATM Layer device, the DS92UT16 polls the connected PHY ports using the MPhy address busses U_TxAddr and U_RxAddr. Only those ports which are connected will be polled. The connected ports list defined in the UCPL3–UCPL0 registers is used to determine which ports are connected. The PHY ports respond on U_TxCLAV[7:0] and U_RxCLAV[7:0]. The MPhy address determines the Port and the CLAV pin number determines the sub-port. Therefore up to 8 sub-ports may be connected to a port. Polling of a single MPhy address will get eight responses on the eight CLAV lines. The DS92UT16 uses the connected sub-port list defined in the UCSPL register to determine which of these eight sub-port responses are valid. On reset, the UCPL3–UCPL0 registers are all set to 0xFF and the UCSPL register is set to 0x01, so the DS92UT16 will poll all ports and assume only sub-port zero is connected.

8.2.2 PHY Polling

When configured as a PHY Layer device, the DS92UT16 is polled by the connected ATM device. During polling, the DS92UT16 will only respond to MPhy addresses on U_TxAddr and U_RxAddr, which are defined as connected. The connected ports list defined in the UCPL3–UCPL0 registers is used to determine which ports are connected. On reset the UCPL3–UCPL0 registers are all set to 0xFF so the DS92UT16 will respond to all MPhy addresses during polling.

NOTE: There must always be at least one connected port defined in the UCPL3–UCPL0 registers. If no ports are to be connected then use Configuration Traffic Inhibit mode described in *Section 10.0 Configuration and Traffic Inhibit Operation*.

8.2.3 Sub-Port Address

The operation of the sub-port address is illustrated in *Figure 10*. To use the Extended Level 2 mode that allows addressing up to 248 Ports, the ATM Layer (that which drives the DS92UT16 in PHY mode) must be capable of inserting a three bit sub-port address in the PDU cell for use by the DS92UT16. This 3-bit sub-port address must reside in either the User Prepend, Cell Header, or UDF bytes. It's location is defined in the UTOPIA Sub-Port Address Location (USPAL) and UTOPIA Sub-Port Address Mask (USPAM) registers. The USPAL register defines which byte of the User Prepend, Cell Header, or UDF, contains the address and the USPAM register defines which three bits of that byte are the sub-port address.

Transmit Path Example: The MPhy address is interpreted as the Port address. So, a cell destined for the PHY designated as Port 0 Sub-Port 7 has the three bit sub-port address 7 (binary "111") inserted into the defined sub-port address location of the PDU cell by the ATM layer head-end. It is then transmitted to the DS92UT16 in PHY mode using MPhy address 0. The DS92UT16 in PHY mode does not examine the sub-port address because all cells are transmitted downbridge anyway.

At the far end, the DS92UT16 in ATM mode extracts the sub-port address. This is used to determine which sub-port CLAV/ENB signals the destination PHY is connected to. A

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8.0 UTOPIA Interface Operation

(Continued)

port address of 0 and a sub-port address of 7 means that the destination PHY is MPhy address 0 attached to U_TxENB[7] and U_TxCLAV[7]. The cell is then transmitted to that PHY.

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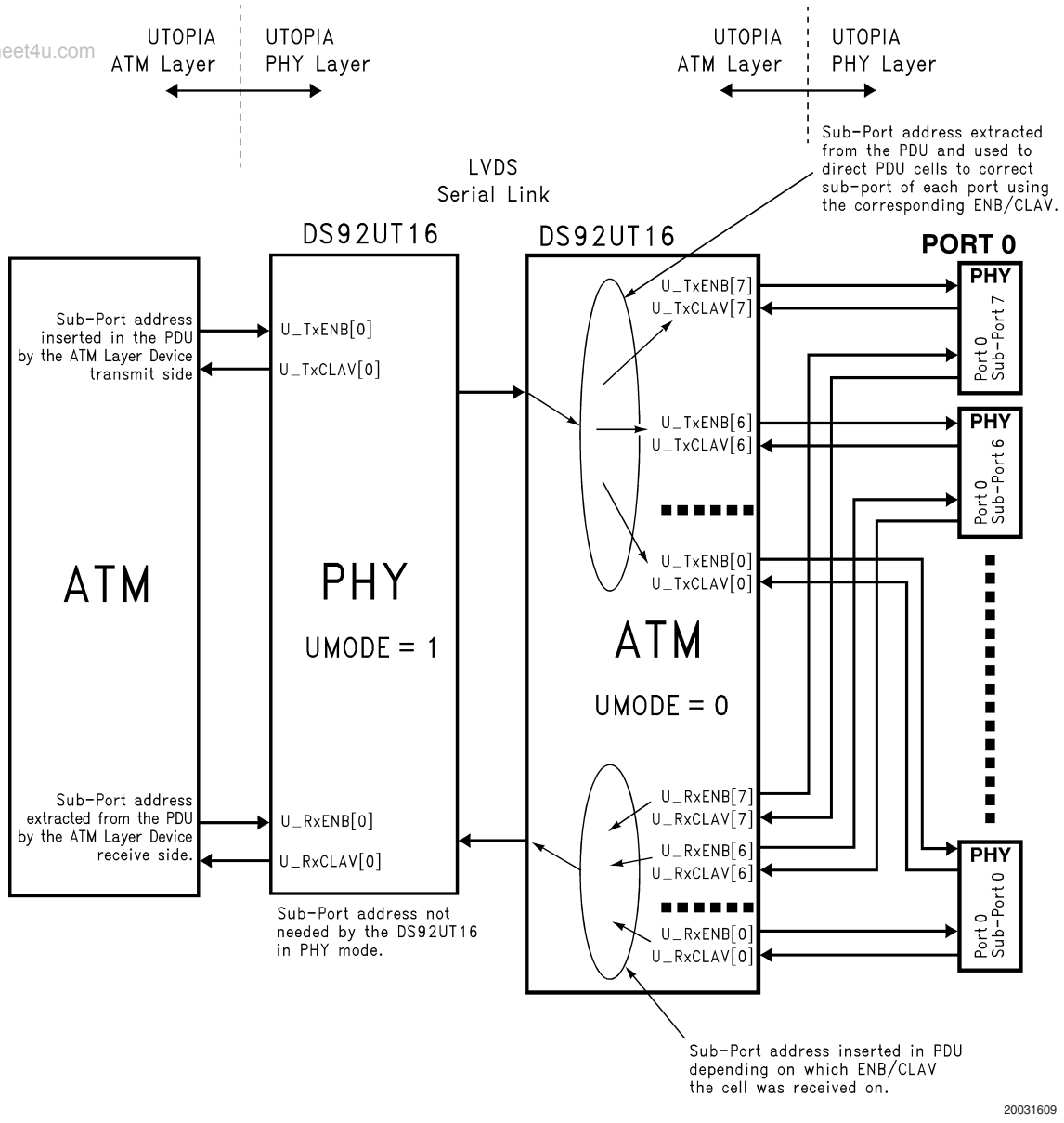

FIGURE 10. Sub-Port Address Operation

Receive Path Example: The DS92UT16 in ATM mode receives a cell from the PHY with MPhy address 0 attached to U_RxENB[6] and U_RxCLAV[6] and designates it as from Port 0 Sub-Port 6. The DS92UT16 inserts the sub-port address 6 (binary "110") into the sub-port address location of the received PDU. Then this PDU is transmitted to the head-end. The head-end ATM layer device must extract this sub-port address from the PDU to determine the full address of the originating PHY.

8.2.4 Connected Port and Sub-Port Lists

Figure 11 illustrates the usage of the connected port list registers (UCPL3–UCPL0) and the connected sub-port list register (UCSPL). In this case, the DS92UT16 in ATM mode defines Port 1 and Sub-port 7 as not connected.

The UCPL3–UCPL0 registers contain 31 bits corresponding to the 31 possible Ports addressed by the MPhy address busses. If a bit location in the UCPL3–UCPL0 registers is set, then that Port is connected. The sub-ports of the con-

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8.0 UTOPIA Interface Operation

(Continued)

nected Port are defined by the UCSPL register. If a bit location in the UCSPL register is set, then that sub-port is connected.

In *Figure 11*, the registers are set as follows: UCPL3 = UCPL2 = UCPL1 = 0xF, UCPL0 = 0xFD, and UCSPL = 0xEF.

With bit 1 of UCPL0 cleared, then Port 1 is not connected. This means that none of the eight sub-ports of Port 1 are connected. So Port 1 Sub-port 7, Port 1 Sub-port 6, Port 1 Sub-port 5, Port 1 Sub-port 4, Port 1 Sub-port 3, Port 1 Sub-port 2, Port 1 Sub-port 1, and Port 1 Sub-port 0 are not connected. Port 1 will therefore, not be polled.

With bit 7 of UCSPL cleared, then sub-port 7 is not connected. This means that sub-port 7 for all possible 31 ports is not connected. So Port 31 Sub-port 7, Port 30 Sub-port 7, Port 29 Sub-port 7,.....and Port 0 Sub-port 7 are not connected.

Therefore, clearing a bit in the UCPL3–UCPL0 registers will disconnect 8 possible PHY port locations and clearing a bit in the UCSPL register will disconnect 31 possible PHY port locations.

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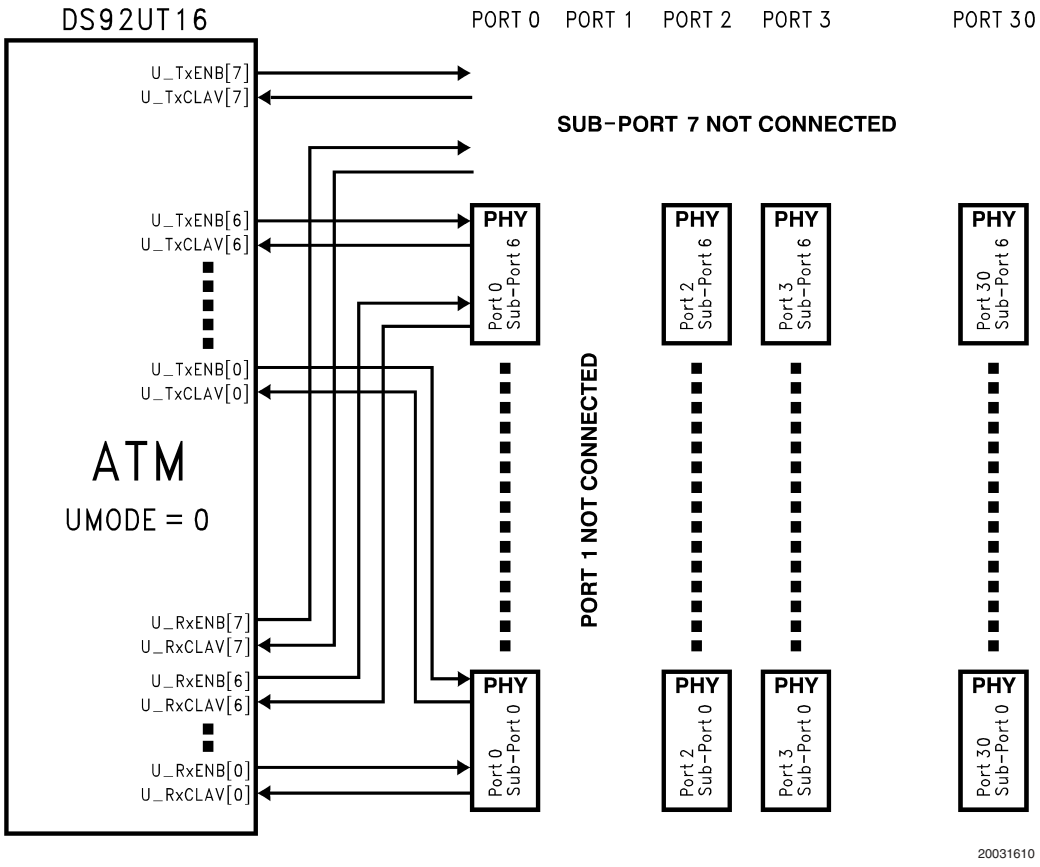

FIGURE 11. Connected Port and Connected Sub-Port Usage

9.0 MTB Queue Configuration

9.1 SINGLE BRIDGE MTB CONFIGURATION

The Multi-port Traffic Buffer is a 160 cell linked-list buffer that is shared across as many as 31 Port queues. There is a single queue per MPHY address.

In the up-bridge direction, a per queue flow control protocol (described in *Section 6.3.5 Flow Control*) prevents queue overflow. Each Port has a programmable upper fill threshold. Should any queue reach this upper threshold, back-pressure is applied over the serial link, via the flow control mechanism, to the far end (transmitting) device. The transmitting device uses the normal UTOPIA flow control handshaking to prevent any more cells being transferred to that MPHY and thus prevents overflow.

With link-list buffers, each queue may be over-assigned memory space, working on the assumption that not every queue will back up simultaneously. To accommodate the rare occasions where the buffer as a whole approaches full but individual queues are below their full threshold, the device also compares the overall buffer fill against a threshold. Should the overall buffer approach overflow, the flow control mechanism provides a global 'halt' command to ensure that no cells will be lost.

The MTB Queue Threshold, MTBQT30–MTBQT0 registers define the maximum size in PDU cells of each of the 31 queues. If all 31 queues are being used it is recommended that the threshold be left at the default of 4 cells. If less than 31 queues are in use then the queue thresholds may be raised if required. The recommended maximum queue thresholds are given in *Table 12*. These are recommended maximum thresholds only.

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9.0 MTB Queue Configuration

(Continued)

It is further recommended that any queue that is not being used is set with a threshold of zero. When a queue has reached its programmed threshold the device flow control mechanism will prevent the far end device from accepting cells for that MPHY address. Therefore, by setting the threshold of an unused queue to zero, it prevents the UTOPIA interface of the far end device from accepting cells for that MPHY address by either, not asserting the CLAV for that MPHY address when in PHY Mode, or not selecting that MPHY address when in ATM mode.

Also, note that setting a threshold of zero will cause the corresponding Queue Full bit in the MTBQFL3–MTBQFL0 registers to be continuously set for that queue.

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TABLE 12. Recommended Maximum MTB Queue Thresholds

Number of Queues in Use	Recommended Threshold	Number of Queues in Use	Recommended Threshold
31	4	15	15
30	4	14	16
29	5	13	18
28	5	12	20
27	5	11	23
26	6	10	26
25	6	9	29
24	7	8	34
23	7	7	39
22	8	6	47
21	9	5	58
20	10	4	74
19	10	3	100
18	11	2	100
17	12	1	154
16	4		

9.2 MULTIPLE BRIDGE MTB CONFIGURATION

When UTOPIA-LVDS bridges are used in parallel as in *Figure 5* the PHY mode DS92UT16s will forward all cells on the UTOPIA TxData bus across the LVDS bridge. Cells that are not addressed for PHYs on a bridge will accumulate in the MTBs of the ATM mode DS92UT16s. If too many cells accumulate the MTB will become full and traffic will be stopped over that bridge. To prevent filling the MTBs PHY port addresses must be distributed evenly across all bridges in the system. Additionally, the MTB queue threshold of any ports not in the Connected Ports List should be set to 0 in order to limit the number of cells that can accumulate.

Table 13 lists the minimum number of ports that must be assigned to each bridge for the total number of ports in the system.

TABLE 13. Minimum Ports per Bridge in a Mult-Bridge System

Total Ports Used	Minimum Number of Ports per Bridge
31	10
30	9
29	8
28	7
27	6
26	5
25	4
24	3
23	2
22	1

10.0 Configuration and Traffic Inhibit Operation

Modifying some device configuration settings should not be carried out while traffic is flowing. A mechanism to inhibit traffic is provided, which should be used when changing any of the settings contained in the PDUCFG, UCFG, USPAL or USPAM registers.

The Traffic Inhibit mechanism causes traffic to stop. The UTOPIA interface will stop transmitting and receiving cells, the LVDS transmit section will transmit Idle cells, and the incoming cells on the active LVDS receive port will be discarded. It is controlled by the Configuration Traffic Inhibit (CTI) and Traffic Inhibit Status (TIS) bits of the General Control and Status (GCS) register, see *Section 18.3 GENERAL CONTROL AND STATUS — 0x03 GCS*.

The processor should set the CTI bit before changing any of the PDUCFG, UCFG, USPAL or USPAM register settings. This will initiate the Traffic Inhibit mechanism. The TIS bit should then be polled. When the TIS bit is set, then traffic is inhibited.

The MTB and FIB queues **MUST** be flushed at this stage. Use the FIBFL and MTBFL bits of the QFL register described in *Section 18.69 QUEUE FLUSH — 0xD8 QFL* to accomplish the queue flushing. Set these bits to flush the queues and then poll these bits to determine when flushed. The queue flushing is complete when these bits are clear.

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10.0 Configuration and Traffic Inhibit Operation (Continued)

The device can now be reconfigured safely. When configuration is completed, then the CTI bit can be cleared by the processor and normal operation resumed.

Note that the CTI bit is set on either power up or software reset (See *Section 18.3 GENERAL CONTROL AND STATUS — 0x03 GCS*) and therefore the Traffic Inhibit mechanism is active. When initialization of the device registers is completed by the processor the CTI bit should be cleared.

Note that the devices at both ends of the LVDS link must be configured with the same values for the PDUCFG, USPAL, and USPAM registers for correct operation.

Note that when configuration of both ends of the link is complete then CTI must not be disabled for at least two PDU transport times (i.e. the length of time it takes to transport two PDUs over the LVDS link). This "CTI disable hold-off period" allows all PDUs of the old configuration to be received and discarded correctly. If this hold-off period is not respected then an idle cell PDU of the old PDU configuration may arrive at a device programmed with the new PDU configuration and incorrectly be interpreted as a valid cell.

Note that any change in the PDU configuration which changes the byte location of the TC HEC byte will cause the far end device to fall out of TC delineation. See *Figure 6*.

11.0 Cell/Frame Delineation and Descrambler Operation

Each of the two Transmission Convergence Sub-Layer (TCS) DisAssemblers receives 16-bit data from the associated LVDS receive section. The TCS DisAssembler must first find the Transport Container (TC) boundaries, then the data can be descrambled and the Frame boundaries found. Once this has been achieved the received data can be disassembled.

After achieving TC delineation and the Descrambler locking, then the cell data within each TC is valid and can be passed to the MTB. If TC delineation is lost, or the Descrambler is not locked, then cell data is invalid and is not passed to the MTB.

Frame delineation must be achieved before the bytes of the F Channel are considered valid. The F Channel consists of the ECC, Flow Control, BIP, Remote Alarm and Signalling and Link Label bytes (*Section 6.3.6 F Channel Byte Usage Within the Frame*). If Frame delineation is lost then

- the received ECC bytes are considered invalid and are assumed to retain the last valid values received
- the Flow Control bytes are considered invalid and are assumed to be all ones, i.e. 'halt' all ports
- the Remote Alarm and Signalling byte is considered invalid and is assumed to retain the last valid value received
- and the Link Label byte is considered invalid and is assumed to retain the last valid value received.

TC and Frame delineation is achieved using the HEC bytes of the TC's. The HEC bytes are not scrambled.

The Descrambler is loaded with the Scrambler sequence on start-up to achieve lock. The operation of these blocks is described below.

11.1 TRANSPORT CONTAINER DELINEATION

At the receive end of the LVDS link, the data will appear as a stream with no indication of Transport Container (TC) or frame boundaries. TC delineation is achieved by finding correct HEC's on the incoming data stream. The TC delineation state diagram is shown in *Figure 12*.

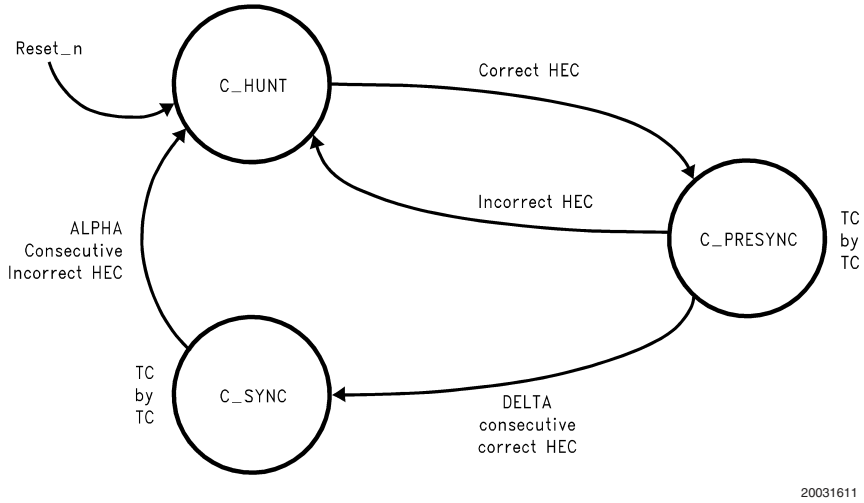

FIGURE 12. State Diagram for TC Delineation

C_HUNT — On reset, the TC delineation state machine starts in the C_HUNT state and TC delineation has not been achieved. In the C_HUNT state, a HEC is calculated word by word on a data stream equal in length to the TC Header and compared against the next received byte. The length of the TC header is derived from the PDUCFG register (*Section 18.5 PDU CONFIGURATION — 0x05 PDUCFG*). This process is repeated until a correct HEC is detected. When a single correct HEC has been detected the state machine moves into the C_PRESYNC state.

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11.0 Cell/Frame Delineation and Descrambler Operation (Continued)

Note that depending on the length of the TC and the length of the TC Header it may be necessary to word slip after a predefined number of HEC calculations in order to obtain a correct HEC.

C_PRESYNC — In C_PRESYNC, if a correct HEC is found DELTA consecutive times then the state machine moves to the C_SYNC state and the system has achieved TC delineation. If an erred HEC is detected during the C_PRESYNC state, the process moves back to the C_HUNT state.

C_SYNC — In the C_SYNC state, TC delineation is assumed to be lost if an erred HEC is obtained on ALPHA consecutive occasions. The state machine will move back to the C_HUNT state.

The values of DELTA and ALPHA are programmable independently for Port A and Port B. They are contained in the RACDT and RBCDT registers (*Section 18.36 RECEIVE PORT A CELL DELINEATION THRESHOLDS — 0x40 RACDT* and *Section 18.55 RECEIVE PORT B CELL DELINEATION THRESHOLDS — 0x80 RBCDT*). On reset, DELTA = 8 and ALPHA = 7.

11.2 FRAME DELINEATION

Once the system has achieved TC delineation, the Frame delineation process can begin. The Frame delineation process is achieved by checking for correct HEC's with the added coset $x^6 + x^4 + x^2 + 1$. This added coset differentiates 'Start of Frame' TC HEC's from normal TC HEC's. Only the HEC of TC0 has this added coset.

This is the standard coset which may be added to all HEC's (CDIS bit in the LKSC register in *Section 18.8 LINK STATUS AND CONTROL — 0x08 LKSC*). If the coset is already added to all HEC's, then it is added again to the HEC of TC0. This ensures that the HEC of TC0 can always be differentiated from that of other TC's.

The Frame delineation state diagram is shown in *Figure 13*.

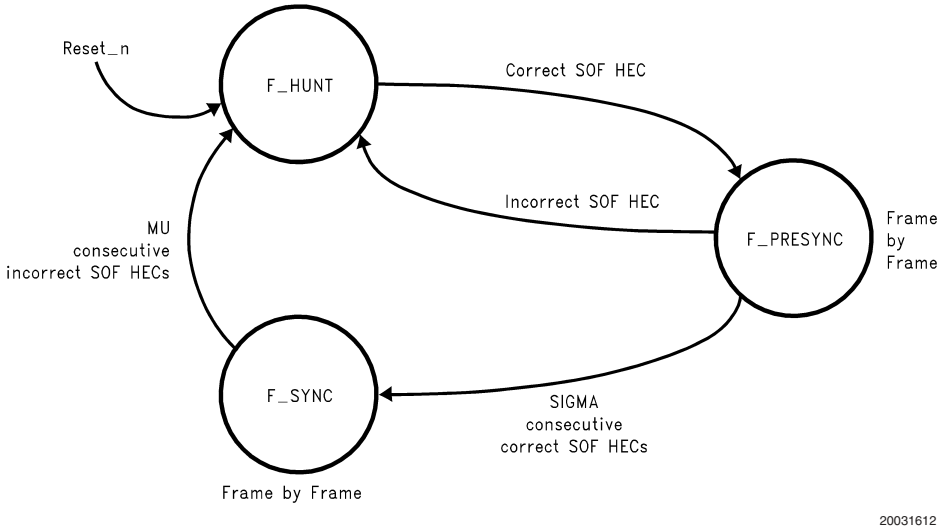

FIGURE 13. State Diagram for Frame Delineation

F_HUNT — On reset, the Frame delineation state machine starts in the F_HUNT state and Frame delineation has not been achieved. Each received HEC is monitored to determine if it has the added coset and is therefore the Start Of Frame (SOF) HEC. When a single correct SOF HEC is detected, the state machine enters the F_PRESYNC state.

F_PRESYNC — In the F_PRESYNC state if a correct SOF HEC is found SIGMA consecutive times the state machine moves to the F_SYNC state and the system is said to have achieved Frame delineation. If an errored SOF HEC is detected during the F_PRESYNC state the state machine moves back to the F_HUNT state.

F_SYNC — In the F_SYNC state, Frame delineation will be assumed to be lost if an erred SOF HEC is obtained on MU consecutive occasions. The state machine will move back to the F_HUNT state.

The values of SIGMA and MU are programmable independently for Port A and Port B. They are contained in the RAFDT and RBFDT registers (*Section 18.37 RECEIVE PORT A FRAME DELINEATION THRESHOLDS — 0x41 RAFDT* and *Section 18.56 RECEIVE PORT B FRAME DELINEATION THRESHOLDS — 0x81 RBFDT*). On reset, SIGMA = 8 and MU = 7.

11.3 DESCRAMBLER OPERATION

Once TC delineation has been obtained, the Descrambler synchronization can begin.

After reset, the Descrambler expects the far-end transmitting device to send it's Scrambler sequence embedded in Idle cells so that the Descrambler can synchronize (lock) to it. This scrambler-sequence transfer is achieved by means of the Remote Descrambler Loss of Lock bit (RDSLL) in the Remote Alarm and Signalling byte (*Section 6.3.7.1 Remote Alarm and Signaling Byte*). This received bit is stored as the RARDSLL bit of the RARA register for Port A (*Section 18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS — 0x3C RARA*) and the RBRDSLL bit of the RBRA register for Port B (*Section 18.52 RECEIVE PORT B REMOTE STATUS AND ALARMS — 0x7C RBRA*).

The lock status of the Descrambler is transmitted to the far-end device as the RDSLL bit. If the Descrambler is out of

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11.0 Cell/Frame Delineation and Descrambler Operation (Continued)

lock, then the transmitted RDSLL = 1. At the far end device, this is stored as RARDSLL or RBRDSLL, depending on which port it is connected to. When this bit is set for the active receive port, it causes the TCS Assembler to transmit the Scrambler sequence embedded in Idle cells. The Descrambler loads this sequence and attempts to lock to it. Once the Descrambler locks to this sequence, it clears the RDSLL bit transmitted to the far-end device, which causes the far-end device to stop sending the Scrambler sequence embedded in Idle cells and to begin sending real traffic cells.

The Descrambler synchronization state diagram is shown in *Figure 14*.

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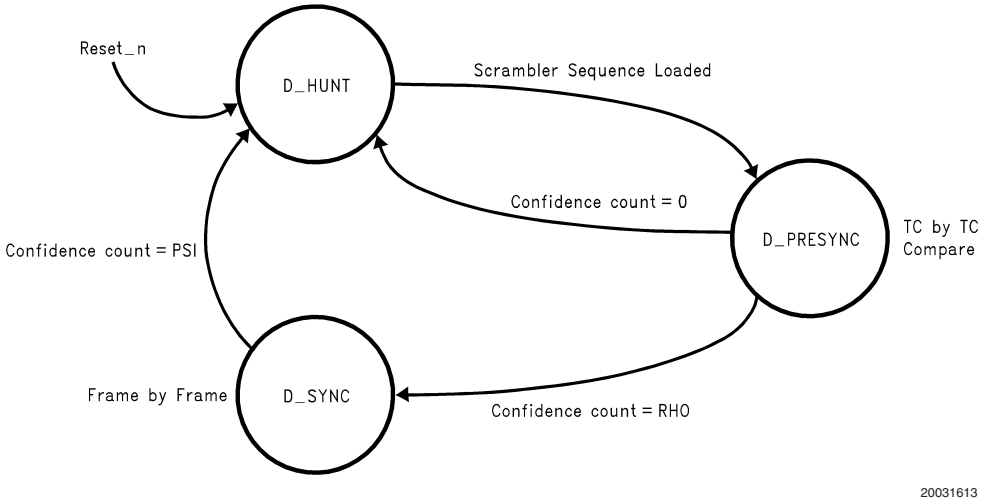

FIGURE 14. State Diagram for Descrambler Synchronization

D_HUNT — On reset, the Descrambler synchronization state machine starts in the D_HUNT state and the Descrambler is not in Lock. When TC delineation has been achieved, the transmitted Scrambler sequence from the far-end device is loaded into the Descrambler. The state machine enters the D_PRESYNC state.

D_PRESYNC — The received scrambler sequences and predicted sequences are compared for each TC. For each correct prediction, a confidence counter *increments*, and for each incorrect prediction, the confidence counter is *decremented*. When the confidence counter reaches RHO, then the state machine moves to the D_SYNCH state and the system is said to have achieved scrambler Lock. If the confidence counter reaches zero then the state machine moves back to the HUNT state.

D_SYNC — The comparison of received scrambler sequences and predicted sequences is repeated for each Frame. For each correct prediction, a confidence counter is *decremented*, and for each incorrect prediction, the confidence counter is *incremented*. The confidence counter has a lower limit of zero. If the confidence counter reaches PSI, then the state machine moves back to the D_HUNT state and the Descrambler is out of Lock.

The state machine will also return directly to D_HUNT if TC delineation is lost.

The values of PSI and RHO are programmable independently for Port A and Port B. They are contained in the RADSLKT and RBDSLKT registers (*Section 18.38 RECEIVE PORT A DESCRAMBLER LOCK THRESHOLDS — 0x42 RADSLKT* and *Section 18.57 RECEIVE PORT B DESCRAMBLER LOCK THRESHOLDS — 0x82 RBDSLKT*). On reset PSI = 8 and RHO = 8.

11.4 ANALYZING LOCK AND SYNCHRONIZATION TIME

After the DS92UT16 LVDS receiver's PLL locks onto the incoming serial data stream and begins to recover data, it must achieve TC lock, then frame lock and descrambler lock before transferring cells. The number of cycles to complete this synchronization depends on the PDU length as well as the byte location in the TC and frame where the receiver begins synchronizing.

Here are the assumptions for this example on calculating the synchronization time.

- PDU length = 64 bytes (maximum possible) = 32 cycles (16 bit data path)
- Max TC length =PDU + 4 bytes = 34 cycles
- Frame = 56 TC = 1904 cycles

Once the LVDS Receive input PLL locks to the incoming serial data stream and recovers data bits, the DS92UT16 searches for a TC HEC byte. Assuming that the DS92UT16 just missed a HEC when the LVDS PHY locked, it will take a minimum of one TC to find the HEC byte. Next, the DS92UT16 will continue finding correct TC HECs until it matches the number in the confidence counter (default setting is DELTA = 8). The TC delineation is now in sync.

Next, the UT16 will start looking for SOF HECs that indicate a start-of-frame. Assuming a SOF has just passed, the max time to find an SOF should be 1 Frame. Now the UT16 will collect frames until the correct number matches the confidence counter (default setting is SIGMA = 8). When the correct number of SOFs matches the confidence counter, the frame delineation is in sync.

Simultaneous with the frame delineation, the DS92UT16 will synchronize and lock the descrambler. The lock procedure begins with the transmitting DS92UT16 sending the scrambler sequence in idle cells. It does this automatically on reset

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11.0 Cell/Frame Delineation and Descrambler Operation (Continued)

or start-up until it receives the cleared RDSLL bit in the Remote Alarm and Signaling byte. After TC delineation occurs at the receive end, the DS92UT16 will count correct scrambler sequence predictions until it matches the confidence counter (default setting is RHO = 8). When the correct number of scrambler sequence predictions matches the confidence counter, the descrambler is synchronized and the receiving DS92UT16 clears the RDSLL bit.

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In this example, the time it takes for a receiving DS92UT16 to synchronize to the transmitting DS92UT16, after the PLL locks, is approximately determined by the following calculation. This time will differ according to PDU length and the value programmed as the confidence thresholds.

(1+8) TC = 9 (34 cycles) = 306 cycles for TC sync, and (1+8) (1 frame) = 9 (1904 cycles) = 17136 cycles. This is a total of 17442 cycles and assumes that the descrambler lock occurs during the 8 frames it takes for the frame delineation to occur.

12.0 LVDS Interface Operation

The LVDS interface combines a transmit serializer and two receive deserializers. The serializer accepts 16- bit data from the TCS Assembler block and transforms it into a serial data stream with embedded clock information. Each deserializer recovers the clock and data from the received serial data stream to deliver the resulting 16-bit wide words to the corresponding TCS DisAssembler block.

The LVDS interface has a Transmit serializer block and two Receive deserializer blocks that can operate independent of each other. The transmit data is duplicated over two differential output pairs with independent tri-state controls. The transmit block has a power-down control. Each receiver has a power down control and the two output stages have independent tri-state control. These features enable efficient operation in various applications.

The serializer and deserializer blocks each have three operating states. They are the Initialization, Data Transfer, and Resynchronization states. In addition, there are two passive states: Powerdown and TRI-STATE.

The following sections describe each operating mode and passive state. For clarity these descriptions refer only to the receive Port A. The operation of receive Port B is the same.

12.1 INITIALIZATION

Before the DS92UT16 sends or receives data, it must initialize the links to and from another DS92UT16. Initialization refers to synchronizing the Serializer's and the Deserializer's PLL's to local clocks. The local clocks must be the same frequency or within a specified range if from different sources. After the Serializers synchronize to the local clocks, the Deserializers synchronize to the Serializers as the second and final initialization step.

Step 1: After applying V_{CC} and GND to the Serializer and Deserializer, the LVDS transmit outputs are held in TRI-STATE and the on-chip power-sequencing circuitry disables the internal circuits. When V_{CC} reaches V_{CC}OK (2.2V) in each device, the PLL in the serializer and deserializer begins locking to the local clock. In the Serializer, the local clock is the LVDS_TxClk, while in the Port A Deserializer it is the reference clock, LVDS_ARefClk. A local on-board oscillator or other source provides the specified clock input to the LVDS_TxClk and LVDS_ARefClk pins.

The Serializer outputs remain in TRI-STATE until the PLL locks to the LVDS_TxClk. After locking to LVDS_TxClk, the Serializer block is now ready to send data or synchronization patterns. If the LVDS_Synch pin is high, or the TXSYNC bit of the LVC register is set (see *Section 18.4 LVDS CONTROL — 0x04 LVC*), then the Serializer block generates and sends the synchronization patterns (sync-pattern).

The internal Port A Deserializer data outputs remain invalid while the PLL locks to the reference clock.

When the Port A Deserializers PLL locks to incoming data or sync-pattern on the LVDS_ADin pins, it will clear the corresponding Local Loss Of Signal bit, LLOSA, in the ETXRXA register (see *Section 18.10 ECC TRANSMIT BUFFER AND RECEIVE LVDS ALARMS — 0x0A ETXRXA*) and the lock pin LVDS_ALock_n will go low.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. The Serializer that is generating the stream to the Deserializer must send random (non-repetitive) data patterns or sync-patterns during this step of the Initialization State. The Deserializer will lock onto sync-patterns within a specified amount of time. The lock to random data depends on the data patterns and, therefore, the lock time is unspecified.

In order to lock to the incoming LVDS data stream, the Deserializer identifies the rising clock edge in a sync-pattern and will synchronize to the embedded clock in less than 5 µs. If the Deserializer is locking to a random data stream from the Serializer, then it performs a series of operations to identify the rising clock edge and locks to it. Because this locking procedure depends on the data pattern, it is not possible to specify how long it will take. At the point where the Port A Deserializer's PLL locks to the embedded clock, the LVDS_ALock_n pin goes low, the LLOSA bit of the ETXRXA register may be cleared and valid data is presented to the TCS DisAssembler block. Note that the LVDS_ALock_n signal is synchronous to valid data being presented to the TCS DisAssembler.

The user's application determines whether sync-patterns or lock to random data is the preferred method for synchronization. If sync-patterns are preferred, the associated Port A deserializer's LVDS_ALock_n pin is a convenient way to provide control of the LVDS_Synch pin, possibly via the RARLOSA (Receive Port A, Remote Loss Of Signal) bit of the RARA register, see *Section 18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS — 0x3C RARA*.

12.2 DATA TRANSFER

After initialization, the Serializer is able to transfer data to the Deserializer. The serial data stream includes a start bit and stop bit appended by the serializer, which frame the sixteen data bits. The start bit is always high and the stop bit is always low. The start and stop bits also function as clock bits embedded in the serial stream.

The Serializer block accepts 16-bit data from the TCS Assembler block. The internal version of the LVDS_TxClk signal latches the incoming data. If the LVDS_Synch input or the TXSYNC bit of the LVC register is high for 5 LVDS_TxClk cycles, the Serializer does not latch data from the TCS Assembler block.

The Serializer transmits the data and clock bits (16+2 bits) at 18 times the LVDS_TxClk frequency. For example, if LVDS_TxClk is 50 MHz, the serial rate is 50 X 18 = 900 Mbps. Since only 16 bits are from input data, the serial "payload" rate is 16 times the LVDS_TxClk frequency. For

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12.0 LVDS Interface Operation

(Continued)

instance, if LVDS_TxClk = 50 MHz, the payload data rate is 50 X 16 = 800 Mbps. LVDS_TxClk is provided by the data source and must be in the range of 30 MHz to 52 MHz.

When the Port A Deserializer channel synchronizes to the input from a Serializer, it drives its LVDS_ALock_n pin low, the LLOSA bit of the ETXRXA register is cleared and valid data is delivered to the TCS DisAssembler. The process flow is that the Port A Deserializer locks to the embedded clock, uses it to generate multiple internal data strobes, and then drives the recovered clock on the LVDS_ARxClk pin. The LVDS_ARxClk is synchronous to the data delivered to the TCS DisAssembler. While the LVDS_ALock_n pin is low, data to the TCS DisAssembler is valid. Otherwise, the data is invalid and is ignored by the TCS DisAssembler and an interrupt may be raised on the LLOSA bit being set high.

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LVDS_ALock_n and LVDS_ARxClk signals will drive a minimum of three CMOS input gates, a 15 pF total load.

The Port A Deserializer input pins LVDS_ADin are high impedance during Receiver Powerdown (LVDS_APwdn pin low or bit RAPWDN of the LVC register set high) and power-off (V_{CC} = 0V).

12.3 RESYNCHRONIZATION

Whenever the Port A Deserializer loses lock, it will automatically try to resynchronize. For example, if the embedded clock edge is not detected two times in succession, the PLL loses lock and the LVDS_ALock_n pin and the LLOSA bit are driven high. The Port A Deserializer then enters the operating mode where it tries to lock to a random data stream. It looks for the embedded clock edge, identifies it and then proceeds through the synchronization process.

The logic state of the LVDS_ALock_n pin indicates whether the data is valid; when it is low, the data is valid. The system must monitor the LVDS_ALock_n pin and LLOSA bit to determine whether received data is valid. The DS92UT16 facilitates this by allowing an interrupt to be raised on LLOSA being set. There is a short delay in response to the PLL losing synchronization to the incoming data stream.

The user can choose to resynchronize to the random data stream or to force fast synchronization by pulsing the Serializer LVDS_Synch pin or setting the TXSYNC bit. This scheme is left up to the user discretion. One recommendation is to provide a feedback loop using the LVDS_ALock_n pin itself to control the sync request of the Serializer, which is the LVDS_Synch pin.

12.4 POWERDOWN/TRI-STATE

The Powerdown state is a very low power consuming sleep mode that the Serializer and Deserializer will occupy while waiting for initialization. You can also use the LVDS_ADenb, LVDS_BDenb, LVDS_TxPwdn, LVDS_APwdn and LVDS_BPwdn pins, or the TXPWDN, TXADEN, TXBDEN, RAPWDN and RBPWDN bits of the LVC register to reduce power when there are no pending data transfers. The Port A Deserializer enters Powerdown when LVDS_APwdn is driven low or the RAPWDN bit is set. In Powerdown, the PLL stops and the outputs go into TRI-STATE, which reduces supply current to the µA range.

To bring the Port A Deserializer block out of the Powerdown state, the system drives LVDS_APwdn high and the RAPWDN bit is cleared. When the Deserializer exits Powerdown, it automatically enters the Initialization state. The system must then allow time for Initialization before data transfer can begin.

The LVDS_TxPwdn driven low or the TXPWDN bit clear, forces the Serializer block into low power consumption where the supply current is in the µA range. The Serializer PLL stops and the output goes into a TRI-STATE condition.

To bring the Serializer block out of the Powerdown state, the system drives LVDS_TxPwdn high and sets the TXPWDN bit. When the Serializer exits Powerdown, its PLL must lock to the LVDS_TxClk before it is ready for the Initialization state. The system must then allow time for Initialization before data transfer can begin.

NOTE: The associated reference clock must always be active for a change of state on the receiver powerdowns. That is LVDS_ARefClk for LVDS_APwdn and LVDS_BRefClk for LVDS_BPwdn must be active to have an effect.

12.5 LOOPBACK TEST OPERATION

The DS92UT16 includes two Loopback modes for testing the device functionality and the transmission line continuity. They are the Line Loopback and the Local Loopback modes.

The Line Loopback connects the serial data input (LVDS_ADin or LVDS_BDin) to the serial data output (LVDS_ADout and LVDS_BDout). The input signal also routes to the parallel data input of the TCS DisAssembler. In the Line Loopback mode, the serial input stream goes through deserializer, passes to both the DisAssembler and the serializer inputs, and then is transmitted out onto the transmission line.

The Local Loopback connects the serial data output from the serializer back to the serial data input of the deserializer. The connection route includes all the functional blocks of the DS92UT16 except for the LVDS serial output buffers and LVDS receiver input.

The ALBC register controls the loopbacks with the LNEN, LNSEL, LCLA and LCLB bits.

12.6 LOOP TIMING OPERATION

The DS92UT16 includes a Loop Timing mode controlled by the LT bit of the GCS register, see *Section 18.3 GENERAL CONTROL AND STATUS — 0x03 GCS*. On reset the LT bit is clear so the LVDS transmit clock is sourced directly from the LVDS_TxClk pin. Setting the LT bit will switch the transmit clock to be sourced from the recovered clock of the active receiver, as defined by the LBA bit of the LKSC register, see *Section 18.8 LINK STATUS AND CONTROL — 0x08 LKSC*. The LVDS transmit and TCA blocks will then be driven by this internal clock and not the LVDS_TxClk pin.

Switching to or from Loop Timing mode will cause the transmitted scrambler sequence to change. This will cause the far end device to loose scrambler lock. However, it may take a number of frames for the far end device to register the lose of scrambler lock because of the setting of the confidence counter, see *Section 11.3 DESCRAMBLER OPERATION*. The far end device will then relock to the new scrambler sequence and operation will resume as normal.

Also, when operating in Loop Timing mode, then a Loss of Lock on the active LVDS receiver, or a switch of active receiver, will also cause the transmitted scrambler sequence to change. This again will cause the far end device to loose scrambler lock. The far end device will then relock to the new scrambler sequence and operation will resume as normal.

Note that from the time that the near end device is switched to or from Loop Timing mode, until the time that the far end device registers the loss of scrambler lock, all received data

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12.0 LVDS Interface Operation

(Continued)

at the far end will be corrupted. This is because the scrambler lock works on a frame-by-frame basis and each frame is 56 transport containers long. For this reason switching to or from Loop Timing mode should not be carried out on live traffic.

Note that both the input LVDS_TxClk clock and active port recovered clock must be present for the switch to complete successfully.

Note also that on reset the device will operate from the LVDS_TxClk input pin clock and therefore this clock must be present to ensure correct operation.

13.0 Switching Receive Ports

The DS92UT16 has two independent receive sections designated Port A and Port B. Either port can receive ATM cell traffic, but only one at a time. The LBA bit of the LKSC register, described in *Section 18.8 LINK STATUS AND CONTROL — 0x08 LKSC*, controls this function.

The ECC also has two independent receive sections. This is controlled by the settings of the ECCA and ECCB bits of the LKSC register. Either one or both ECC receive sections can be active. The selected ECC receive port is independent of the active traffic port selection. For example, you may select Port A as active for cell traffic by clearing the LBA bit, and select the ECC to be receiving on Port B by setting the ECCB bit. The ECC can communicate over either link without affecting the active cell traffic port because the ECC does not use any of the transport container designated for ATM cells.

Selecting the active traffic receive port is accomplished by simply changing the value of the LBA bit. When set high, Port B accepts the traffic cells, and when cleared to low, Port A accepts the traffic cells. After changing the LBA value, the MTB will complete receiving the current cell before switching to the new receive Port. The MTB then waits for the next Start of Cell indication from the associated TCS DisAssembler. This means that the MTB does not need to be flushed or reset because of a change in the active traffic receive Port.

Switching from one port to another completes in a maximum of 6 clock cycles. However, this switch does not start until after receiving the end of the current cell into the MTB.

Changing the value of the LBA bit to switch ports will clear the ABSC bit of the LKSC register. When the switch from one port to the other is completed successfully then the hardware will set the ABSC bit. The processor can poll this bit to determine when the switch has been completed.

14.0 Performance Monitoring

14.1 LIVE TRAFFIC PERFORMANCE MONITORING

Performance monitoring is carried out on live traffic in two ways. One is using the HEC bytes associated with each cell's TC. The other is the BIP bytes of the F channel embedded in the frame structure, as described in *Section 6.3.7.4 BIP16*.

A 24-bit count of errored HEC's received on Port A is contained in the RAHECC2–RAHECC0 registers (*Section 18.27 RECEIVE PORT A HEC COUNT — 0x2E to 0x30 RAHECC2 to RAHECC0*). When the number of received erred HEC's exceeds the threshold defined in the RAHECT2–RAHECT0 registers (*Section 18.28 RECEIVE PORT A HEC THRESHOLD — 0x31 to 0x33 RAHECT2 to RAHECT0*), an interrupt may be raised on the RAXHEC alarm bit in the RAPA alarm register (*Section 18.31 RECEIVE PORT A PERFORMANCE ALARMS — 0x3A RAPA*). The count register RAHECC2–RAHECC0 is reset on read.

A 24-bit count of errored BIP bytes is similarly maintained in the RABIPC2–RABIPC0 registers (*Section 18.29 RECEIVE PORT A BIP COUNT — 0x34 to 0x36 RABIPC2 to RABIPC0*). The associated erred BIP threshold is contained in the RABIPT2–RABIPT0 registers (*Section 18.30 RECEIVE PORT A BIP THRESHOLD — 0x36 to 0x39 RABIPT2 to RABIPT0*) and an interrupt may be raised on the RAXBIP alarm bit in the RAPA alarm register. The count register RABIPC2–RABIPC0 is also reset on read.

The same mechanism is in place for Port B using the RBHECC2–RBHECC0, RBHECT2–RBHECT0, RBBIPC2–RBBIPC0, RBBIPT2–RBBIPT0 and RBPA registers (*Section 18.46 RECEIVE PORT B HEC COUNT — 0x6E to 0x70 RBHECC2 to RBHECC0*, *Section 18.47 RECEIVE PORT B HEC THRESHOLD — 0x71 to 0x73 RBHECT2 to RBHECT0*, *Section 18.48 RECEIVE PORT B BIP COUNT — 0x74 to 0x76 RBBIPC2 to RBBIPC0*, *Section 18.49 RECEIVE PORT B BIP THRESHOLD — 0x77 to 0x79 RBBIPT2 to RBBIPT0* and *Section 18.50 RECEIVE PORT B PERFORMANCE ALARMS — 0x7A RBPA*).

In addition to the HEC and BIP monitoring, live traffic loopback cell monitoring and loopback cell counts are maintained and may raise interrupts on detection of a loopback cell as described in *Section 15.1 ATM CELL LOOPBACK*.

14.2 BIT ERROR COUNT MODE

In addition to live traffic performance monitoring, a PRBS based LVDS link bit error count facility is available. In this mode, no cells are transmitted and instead the raw scrambler pseudo-random sequence (polynomial $x^{31} + x^{28} + 1$) is transmitted. The descrambler will lock to this sequence and then count individual bit errors in the PRBS stream. This bit error count is maintained in a count register. As there is no data cell delineation, the frame delineation will be lost. This is not a live traffic test.

The device will transmit this PRBS data when the TXPRBS bit of the TERRCTL register is set (*Section 18.15 TEST ERROR CONTROL — 0x16 TERRCTL*). When this bit is set, no cell data is transmitted and the TCS Assembler is paused. In addition, no cells will be read from the FIB queue.

The receive section of Port A can lock onto this sequence and maintain the bit error count when the RABEC bit of the RACTL register is set (*Section 18.25 RECEIVE PORT A CONTROL — 0x24 RACTL*). The bit error count is maintained in the RABEC2–RABEC0 registers (*Section 18.39 RECEIVE PORT A BIT ERROR COUNT — 0x43 to 0x45 RABEC2 to RABEC0*). This counter has no associated threshold register and will not generate an interrupt. The counter may be polled (read) at fixed intervals to determine a Bit Error Rate. This counter is reset on read. The count value is only valid when both the TXPRBS bit and the RABEC bit are set.

Port B can operate in the same fashion using the RBBEC bit of the RBCTL register (*Section 18.44 RECEIVE PORT B CONTROL — 0x64 RBCTL*) and the RBBEC2–RBBEC0 registers (*Section 18.58 RECEIVE PORT B BIT ERROR COUNT — 0x83 to 0x85 RBBEC2 to RBBEC0*).

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14.0 Performance Monitoring (Continued)

TABLE 14. Performance Monitoring Alarms

Performance Counter	Associated Alarm	Comments
RAHECC2–RAHECC0 (*Section 18.27 RECEIVE PORT A HEC COUNT — 0x2E to 0x30 RAHECC2 to RAHECC0*)	RAXHEC — Rx Port A Excessive HEC Errors. (*Section 18.31 RECEIVE PORT A PERFORMANCE ALARMS — 0x3A RAPA*)	Rx Port A 24-bit errored HEC counter. Mission mode Up-Bridge receive direction HEC monitoring.
RABIPC2–RABIPC0 (*Section 18.29 RECEIVE PORT A BIP COUNT — 0x34 to 0x36 RABIPC2 to RABIPC0*)	RAXBIP — Rx Port A Excessive BIP Errors. (*Section 18.31 RECEIVE PORT A PERFORMANCE ALARMS — 0x3A RAPA*)	Rx Port A 24-bit errored BIP counter. Mission mode link error monitoring.
RABEC2–RABEC0 (*Section 18.39 RECEIVE PORT A BIT ERROR COUNT — 0x43 to 0x45 RABEC2 to RABEC0*)	None	Rx Port A 24-bit Bit Error Counter. Non-mission mode BER counter of PRBS data on LVDS link.
RBHECC2–RBHECC0 (*Section 18.46 RECEIVE PORT B HEC COUNT — 0x6E to 0x70 RBHECC2 to RBHECC0*)	RBXHEC — Rx Port B Excessive HEC Errors. (*Section 18.50 RECEIVE PORT B PERFORMANCE ALARMS — 0x7A RBPA*)	Rx Port B 24-bit errored HEC counter. Mission mode Up-Bridge receive direction HEC monitoring.
RBBIPC2–RBBIPC0 (*Section 18.48 RECEIVE PORT B BIP COUNT — 0x74 to 0x76 RBBIPC2 to RBBIPC0*)	RBXBIP — Rx Port B Excessive BIP Errors. (*Section 18.50 RECEIVE PORT B PERFORMANCE ALARMS — 0x7A RBPA*)	Rx Port B 24-bit errored BIP counter. Mission mode link error monitoring.
RBBEC2–RBBEC0 (*Section 18.58 RECEIVE PORT B BIT ERROR COUNT — 0x83 to 0x85 RBBEC2 to RBBEC0*)	None	Rx Port B 24-bit Bit Error Counter. Non-mission mode BER counter of PRBS data on LVDS link.
RAU2DLBC (*Section 18.35 RECEIVE PORT A UP2DOWN LOOPBACK CELL COUNT — 0x3E RAU2DLBC*)	U2DLBC — Up-2-Down Loopback Cell Count Change. Cell(s) received on LVDS interface. (*Section 18.72 UTOPIA AND ATM ALARMS — 0xE1 UAA*)	Rx Port A 8-bit Loopback cell counter. Mission mode diagnostic aid.
RBU2DLBC (*Section 18.54 RECEIVE PORT B UP2DOWN LOOPBACK CELL COUNT — 0x7E RBU2DLBC*)	U2DLBC — Up-2-Down Loopback Cell Count Change. Cell(s) received on LVDS interface. (*Section 18.72 UTOPIA AND ATM ALARMS — 0xE1 UAA*)	Rx Port B 8-bit Loopback cell counter. Mission mode diagnostic aid.
D2ULBCC (*Section 18.71 ATM DOWN2UP LOOPBACK CELL COUNT — 0xE0 D2ULBCC*)	D2ULBC — Down-2-Up Loopback Cell Count Change. Cell(s) transmitted back out on UTOPIA interface. (*Section 18.72 UTOPIA AND ATM ALARMS — 0xE1 UAA*)	UTOPIA Interface 8-bit Loopback cell counter. Mission mode diagnostic aid.

TABLE 15. General Alarms

Alarms	Description
LLOSC (*Section 18.10 ECC TRANSMIT BUFFER AND RECEIVE LVDS ALARMS — 0x0A ETXRXA*)	Change of Status on LLOSA or LLOSB.
LLOSA (*Section 18.10 ECC TRANSMIT BUFFER AND RECEIVE LVDS ALARMS — 0x0A ETXRXA*)	Loss of Signal on LVDS receive Port A.
LLOSB (*Section 18.10 ECC TRANSMIT BUFFER AND RECEIVE LVDS ALARMS — 0x0A ETXRXA*)	Loss of Signal on LVDS receive Port B.

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14.0 Performance Monitoring (Continued)

TABLE 15. General Alarms (Continued)

Alarms	Description
ETXBR (*Section 18.10 ECC TRANSMIT BUFFER AND RECEIVE LVDS ALARMS—0x0A ETXRXA*)	ECC transmit buffer ready for new message.
RALLC (*Section 18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA*)	Receive Port A. Link Label Change of value.
RALLM (*Section 18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA*)	Receive Port A. Link Label Mismatch between expected and received value.
RALCS (*Section 18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA*)	Receive Port A. Change of Status on RALDSLL, RALTCLL or RALFLL.
RALDSLL (*Section 18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA*)	Receive Port A. Descrambler Loss of Lock.
RALTCLL (*Section 18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA*)	Receive Port A. Transport Container delineation Loss of Lock.
RALFLL (*Section 18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA*)	Receive Port A. Frame delineation Loss of Lock.
ERABF (*Section 18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA*)	Receive Port A. ECC Receive Buffer Full—contains valid new message.
RARCS (*Section 18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS—0x3C RARA*)	Receive Port A. Remote Change of Status on RARLOSA, RARLOSB, RARBA or RARDSLL.
RARLOSA (*Section 18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS—0x3C RARA*)	Receive Port A. Remote Loss of Signal on LVDS receive Port A.
RARLOSB (*Section 18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS—0x3C RARA*)	Receive Port A. Remote Loss of Signal on LVDS receive Port B.
RARBA (*Section 18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS—0x3C RARA*)	Receive Port A. Remote Active receive port B or A.
RARDSLL (*Section 18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS—0x3C RARA*)	Receive Port A. Remote Descrambler Loss of Lock.
RBLLC (*Section 18.42 RECEIVE PORT B LOCAL ALARMS—0x62 RBLA*)	Receive Port B. Link Label Change of value.
RBLLM (*Section 18.42 RECEIVE PORT B LOCAL ALARMS—0x62 RBLA*)	Receive Port B. Link Label Mismatch between expected and received value.

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14.0 Performance Monitoring (Continued)

TABLE 15. General Alarms (Continued)

Alarms	Description
RBLCS (*Section 18.42 RECEIVE PORT B LOCAL ALARMS—0x62 RBLA*)	Receive Port B. Change of Status on RBLDSLL, RBLTCLL or RBLFLL.
RBLDSLL (*Section 18.42 RECEIVE PORT B LOCAL ALARMS—0x62 RBLA*)	Receive Port B. Descrambler Loss of Lock.
RBLTCLL (*Section 18.42 RECEIVE PORT B LOCAL ALARMS—0x62 RBLA*)	Receive Port B. Transport Container delineation Loss of Lock.
RBLFLL (*Section 18.42 RECEIVE PORT B LOCAL ALARMS—0x62 RBLA*)	Receive Port B. Frame delineation Loss of Lock.
ERBBF (*Section 18.42 RECEIVE PORT B LOCAL ALARMS—0x62 RBLA*)	Receive Port B. ECC Receive Buffer Full—contains valid new message.
RBRCS (*Section 18.52 RECEIVE PORT B REMOTE STATUS AND ALARMS—0x7C RBRA*)	Receive Port B. Remote Change of Status on RBRLOSA, RBRLOSB, RBRBA or RBRDSLL.
RBRLOSA (*Section 18.52 RECEIVE PORT B REMOTE STATUS AND ALARMS—0x7C RBRA*)	Receive Port B. Remote Loss of Signal on LVDS receive Port A
RBRLOSB (*Section 18.52 RECEIVE PORT B REMOTE STATUS AND ALARMS—0x7C RBRA*)	Receive Port B. Remote Loss of Signal on LVDS receive Port B.
RBRBA (*Section 18.52 RECEIVE PORT B REMOTE STATUS AND ALARMS—0x7C RBRA*)	Receive Port B. Remote Active receive port B or A.
RBRDSLL (*Section 18.52 RECEIVE PORT B REMOTE STATUS AND ALARMS—0x7C RBRA*)	Receive Port B. Remote Descrambler Loss of Lock.
PDULA (*Section 18.72 UTOPIA AND ATM ALARMS—0xE1 UAA*)	PDU Length greater than 64 bytes.
CTFRA (*Section 18.72 UTOPIA AND ATM ALARMS—0xE1 UAA*)	Cell Transfer error on UTOPIA interface.
UPRTY (*Section 18.72 UTOPIA AND ATM ALARMS—0xE1 UAA*)	Parity error detected on UTOPIA interface.
FIBOVA (*Section 18.72 UTOPIA AND ATM ALARMS—0xE1 UAA*)	FIB buffer overflow (down-bridge).
MTBSOVA (*Section 18.72 UTOPIA AND ATM ALARMS—0xE1 UAA*)	MTB Soft overflow. One or more of the 31 MTB queues has exceeded its programmed threshold (up-bridge).

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14.0 Performance Monitoring (Continued)

TABLE 15. General Alarms (Continued)

Alarms	Description
MTBHOVA (*Section 18.72 UTOPIA AND ATM ALARMS—0xE1 UAA*)	MTB Hard overflow. The MTB queue has overflowed (up-bridge).

15.0 Loopback Operation

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To assist in diagnostic testing, the DS92UT16 provides both physical interface loopbacks and ATM cell loopbacks as shown in *Figure 7* in *Section 6.8 LOOPBACKS*. The former is suitable for designer or commission testing when the device is not passing live traffic. The latter allows cell trace testing on live traffic. All loopbacks are programmable via the microprocessor interface. The LVDS physical loopbacks are described in *Section 12.5 LOOPBACK TEST OPERATION*.

15.1 ATM CELL LOOPBACK

The ATM Cell Loopback function provides two separate loopback operations. The Down2Up_ATM loopback detects special loopback cells received on the UTOPIA interface and transmits them back out over the UTOPIA interface. The Up2Down_ATM loopback detects special loopback cells received on the LVDS interface and transmits them back out over the LVDS interface. *Figure 7*(b) in *Section 6.8 LOOPBACKS* illustrates both of these operations.

These loopback circuits accommodate one loopback cell at a time. Therefore, a loopback cell should be sent and received before transmitting another loopback cell.

The ATM and LVDS Loopback Control register ALBC controls the ATM cell loopback functionality. See *Section 18.14 GENERAL PURPOSE INPUT OUTPUT—0x15 GPIO*. Bit D2ULB enables the Down2Up_ATM loopback and bit U2DLB enables the Up2Down_ATM loopback. It is possible to enable both loopback operations at the same time.

The special loopback cell format is defined in the ATM Loopback Cell Format registers ALBCF3–ALBCF0. See *Section 18.20 ATM LOOPBACK CELL FORMAT —0x1C to 0x1F ALBCF3 to ALBCF0*. These registers define the contents of the cell's four header bytes, which indicate that a received cell is a loopback cell. Associated with the ALBCF3–ALBCF0 registers are the ATM Loopback Cell Filter registers ALFLT3–ALFLT0. See *Section 18.74 ATM LOOPBACK CELL FILTER—0xF7 to 0xFA ALFLT3 to AFLT0*. These registers define the cell header bits that are compared with the header format declared in the ALBCF3–ALBCF0 registers. It is therefore possible to mask out any bits of the cell header from comparison.

For Down2Up_ATM loopback on the UTOPIA interface only, a loopback cell will be sent back out to the MPhy address on which it was received. So, if a loopback cell was detected coming into the device on MPhy address 0x01, then it will be sent back out of the device on the next occasion that a cell for MPhy address 0x01 is to be sent.

For Up2Down_ATM loopback on the LVDS interface, the MPhy address is embedded in the incoming PDU. Therefore, the loopback cell is simply transmitted back out.

For Down2Up_ATM loopback, only loopback cells as defined by the ALBCF3–ALBCF0 and ALFLT3–ALFLT0 registers are looped-back and all other cells are passed as normal.

For Up2Down_ATM loopback, only loopback cells as defined by the ALBCF3–ALBCF0 and ALFLT3–ALFLT0 registers are looped back and all other cells are passed as normal.

The Down2Up Loopback Cell Count register, the D2ULBCC in *Section 18.71 ATM DOWN2UP LOOPBACK CELL COUNT—0xE0 D2ULBCC*, maintains a count of the Down2UP_ATM loopback cells. Whenever this counter increments, the D2ULBC alarm in the UAA register is set. See *Section 18.72 UTOPIA AND ATM ALARMS—0xE1 UAA*. Note that this counter only increments when the loopback cell exits the device. So the D2ULBC counter increments on **outgoing** loopback cells.

Both Receive Port A and Receive Port B maintain Up2Down_ATM loopback counts. The registers that maintain these counts are the Receive Port A Up2Down Loopback Cell Count register, RAU2DLBC, and the Receive Port B Up2Down Loopback Cell Count register, RBU2DLBC. See *Section 18.35 RECEIVE PORT A UP2DOWN LOOPBACK CELL COUNT—0x3E RAU2DLBC* and *Section 18.54 RECEIVE PORT B UP2DOWN LOOPBACK CELL COUNT—0x7E RBU2DLBC*.

Whenever the counter in the Active receiver (as defined by the LBA bit of the LKSC, see *Section 18.8 LINK STATUS AND CONTROL—0x08 LKSC*) increments, the U2DLBC alarm in the UAA register is set. See *Section 18.72 UTOPIA AND ATM ALARMS—0xE1 UAA*. Although each counter increments whenever it detect an incoming loopback cell, only increments to the active receiver's counter can set the alarm. Note that received loopback cells increment these counters. So the U2DLBC counter increments on **incoming** loopback cells.

Alarms in the UAA register will raise an interrupt if the appropriate interrupt enables are set in the UAIE register. See *Section 18.73 UTOPIA AND ATM INTERRUPT ENABLES—0xE2 UAIE*.

Loopback cells are only counted and looped-back in the appropriate loopback mode. If the loopback mode is not set then any incoming loopback cells are simply treated as normal traffic cells and passed by the device. In Up2Down_ATM loopback mode, only cells from the Active receiver will be looped-back.

A loopback cell transmission may be initiated by the DS92UT16 over the LVDS transmit link. The TXLVLB bit in the ALBC register controls this functionality. Setting the TXLVLB bit causes a single loopback cell to be transmitted over the LVDS transmit link. When the DS92UT16 finishes transmitting the loopback cell, it automatically clears the TXLVLB bit. So, the processor, on setting the TXLVLB bit, should poll it to detect that it clears before trying to set it again to send another loopback cell. The loopback cell transmitted will have a header of the format defined by the ALBCF3–ALBCF0 registers and an MPhy address as defined by the ALBMP register

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16.0 Embedded Communication Channel Operation

This section describes the ECC operation. The ECC transmits one 8 byte message per frame over the link under software control. Flow control ensures that messages are not overwritten at the receive end.

The message to be transmitted is written to the ETXD7–EXTD0 transmit buffer registers and the received messages are stored in the Port A ERAD7–ERAD0 or Port B ERBD7–ERBD0 receive buffer registers. Software control is achieved on the transmit side using the ECC Transmit Buffer Ready (ETXBR) interrupt of the ETXRXA register and the ECC Transmit Send (ETXSD) register.

There are independent receive sections in Port A and Port B and these are controlled using the ECC Receive Port A Buffer Full (ERABF) interrupt of the Receive Port A Local Alarm (RALA) register, and the ECC Receive Port B Buffer Full (ERBBF) interrupt of the Receive Port B Local Alarm (RBLA) register respectively. The choice of receiving ECC messages on Port A or Port B is controlled by the ECCB and ECCA bits of the Link Status and Control (LKSC) register.

The Remote Alarm and Signalling Byte carries the ECC signaling bits. The transmitted Remote Alarm and Signalling Byte carries the ESS signal for both of the local ECC receive sections, ESSA and ESSB. At the receiver a choice must be made as to which ESS bit of the received Remote Alarm and Signalling Byte is valid for the local ECC transmitter. This is controlled by the RAESS and RBESS bits of the RACTL and RBCTL registers respectively.

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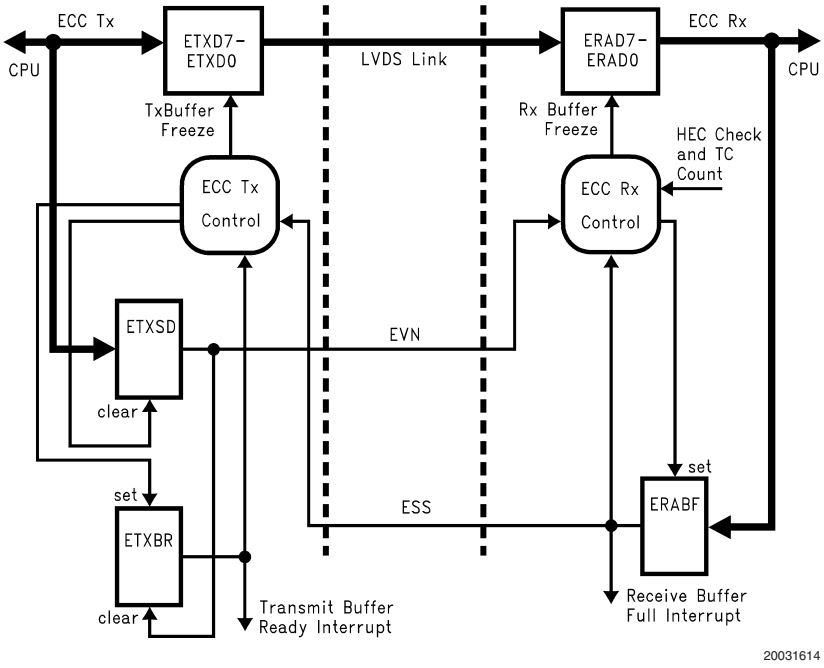

FIGURE 15. The Basic Structure Of The ECC

16.1 BASIC ECC PROTOCOL — ONE TRANSMIT AND ONE RECEIVE

The basic operation of an ECC link is described here using the transmit section of the device at one end of the LVDS link and a single receive section (Port A) of the device at the other end of the link.

The ECC transmitter and receiver communicate via the embedded control signals EVN, ESSA and ESSB in the Remote Alarm and Signalling byte contained in the F1 byte of TC6. By default both receive ports will extract the incoming ESSA bit as the valid ESS to pass to the ECC transmit section. This assumes that the local ECC transmit section is connected to the remote device receiver port A. If the local transmitter is connected to the remote device receiver port B then the incoming ESSB bit must be selected as the valid ESS to pass to the local ECC transmit section. The selection of valid incoming ESS bit is accomplished using the RAESS and RBESS bits of the RACTL and RBCTL registers respectively.

Note that only one of the incoming remote ESS bits is valid on each link as the local transmitter cannot be connected to both receivers on another DS92UT16 device.

The EVN and ESS bits are interpreted as follows:

EVN - Set = Valid ECC data in F1/F2 bytes of TC13, TC20, TC41 and TC48.

Clear = Null (not valid) ECC data in F1/F2 bytes of TC13, TC20, TC41 and TC48.

ESS - Set = Stop sending ECC data as receive buffer is full.

Clear = Send ECC data as receive buffer is ready.

The protocol for transmission of an ECC message is as follows.

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16.0 Embedded Communication Channel Operation (Continued)

Reset

The transmit buffer ready ETXBR bit is set indicating that the transmit buffer ETXD7–ETXD0 can be written to and the Tx Buffer Freeze is clear (inactive).

The transmit buffer send ETXSD bit is clear indicating that no message is being sent and therefore EVN is clear indicating to the receiver that Null data is being transmitted.

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The receive buffer full ERABF bit is clear indicating that no message has been received and therefore ESS is clear indicating to the transmitter that it can send a message when ready.

Assembling A Message

As the ETXBR bit is set the processor now has read/write access to the transmit buffer ETXD7–ETXD0 and can assemble a message by writing to these registers in any order. The message can be read back for checking. Writing to these registers does not affect the ETXBR and ETXSD bits or the EVN signal.

Transmitting A Message

To transmit a message the processor simply sets the send bit ETXSD. This clears the ETXBR bit preventing write access to the transmit buffer so the message being transmitted cannot be corrupted by writes to the ETXD7–ETXD0 registers until transmission is completed. The setting of the ETXSD bit also set the EVN signal indicating to the receiver that Valid data is being transmitted in the F1/F2 bytes of TC13, TC20, TC41 and TC48.

Note that transmitting a message depends on the incoming ESS signal. If ESS is clear indicating that a message can be sent, then the processor can write to the ETXSD bit. However, if ESS is set indicating that a message cannot be sent, then the ETXSD bit is held in reset and cannot be written to by the processor to initiate transmission. This provides flow control from the receiver back to the transmitter.

Receiving A Message

As the receiver ERABF bit is clear the ESS bit is clear indicating that the receiver can accept a message. The receiver monitors the incoming EVN signal to determine when valid data is being transmitted.

On detecting EVN set the receiver uses the TC number to extract the 8 ECC message bytes from the incoming data stream. If an errored HEC is detected on any of the ECC message bytes then the receiver assumes all 8 bytes are corrupted and will re-extract the entire message on the next frame. The transmitter will continue to transmit the message as long as the ESS signal is clear.

When the receiver determines that it has received the entire message it sets the receive buffer full ERABF bit. This prevents the receive buffer ERAD7–ERAD0 being updated by the incoming ECC bytes so that the message cannot be overwritten. It also raises an interrupt to the local processor to indicate that a valid ECC message has been received.

The setting of the ERABF bit also sets the ESS signal back to the transmitter indicating that it should stop transmission. This clears the ETXSD bit which clears the EVN signal thus indicating that transmitted ECC data is Null (not valid).

At this stage the receive buffer is full and cannot receive any further messages. The transmit buffer ready ETXBR is still clear meaning that no new messages can be assembled and ETXSD is held clear so no new messages can be transmitted. This flow control ensures that no new messages will be transmitted until the current received message is read. This situation will remain until the received message is read by the local processor.

Reading A Message

The setting of the ERABF bit in the receiver raises an interrupt to the local processor indicating that a valid ECC message has been received and can be read. The receive buffer registers ERAD7–ERAD0 are read only. The processor may read theses registers in any order and the reading of them has no affect on the ERABF bit or the ESS signal.

When the processor is finished reading the message from the buffer it writes to the ERABF bit to clear it. This allows the receiver to receive a new message. The clearing of the ERABF bit clears the ESS signals indicating to the transmitter that it can send another message.

Transmitting a New Message

The clearing of the incoming ESS signal causes the transmitter to set the transmit buffer ETXBR bit. This allows write access to the transmit buffer ETXD7–ETXD0 for the assembly of a new message. It also releases the ETXSD bit from reset and the processor can now set this bit to send a new message.

At this transmitter stage, the ETXBR bit is set, the ETXSD bit is clear, and EVN is clear. At the receiver, the ERABF bit is clear and the ESS signal is clear. This is the same situation as after reset and therefore, the same sequence as above can be followed to transmit a new message.

Note that the transmit buffer registers can be modified or overwritten to assemble a new message for transmission, or the existing message can be resent simply by setting the ETXSD bit again.

SUMMARY

- Tx - If the ETXBR bit is set, then write the message to the ETXD7–ETXD0 registers.
- Tx - Set the ETXSD bit to send the message. This clears ETXBR.
- Rx - When full message is received, the ERABF bit is set and this raises an interrupt.
- Rx - After reading the message, clear the ERABF bit to allow new message to be received.
- Tx - The clearing of the ERABF bit sets the ETXBR bit, which allows a new message to be assembled and transmitted.

Flow Charts

The Flow Charts in *Figures 16, 17* summarize the control of the ECC receive and transmit.

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16.0 Embedded Communication Channel Operation (Continued)

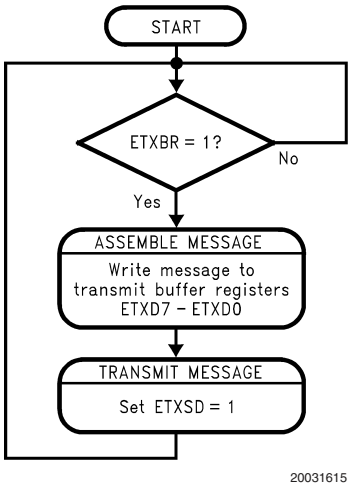

FIGURE 16. ECC Transmit Flow Chart

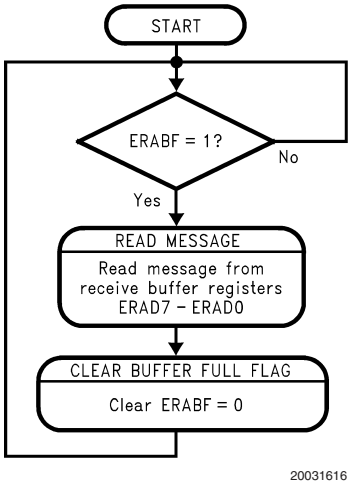

FIGURE 17. ECC Receive Flow Chart (Port A)

16.2 ECC OPERATION WITH ACTIVE AND STANDBY RECEIVERS

The DS92UT16 has two independent receive sections, Port A and Port B. These each contain an ECC receive section and the ECC can be configured to receive over Port A or Port B or over both Port A and Port B together. The ECC receive port can be selected independent of the traffic receive port. Therefore, traffic data is received on the active port designated by the LBA bit of the LKSC register but the ECC can receive on either Port A or Port B as designated by the ECCA and ECCB bits of the same LKSC register. In a protected system with an active and standby LVDS link this can be used to communicate with the standby link while traffic continues to be received from the active link. *Figure 18* shows three DS92UT16 devices with ECC communication over both links.

ECC Receive on Port A: Device 1 communicating with Device 2 only.

Device 1: For the ECC to communicate across Link A only, the ECCA bit of the LKSC register is set and the ECCB bit is clear. The incoming valid ESS signal received over Link A, “RxA valid ESS”, is the only one used by the ECC transmit section in Tx. The RxA port is programmed to extract the incoming ESSA bit as the valid ESS, as the Device 1 transmitter is connected to Device 2 receiver Port A. This is accomplished by clearing the RAESS bit of the RACTL register.

In this case, when an ECC message is transmitted, the “RxA valid ESS” signals when the message has been successfully received by the far-end Device 2. So, ECC communications only occur over Link A between Device 1 and Device 2.

Device 2: The ECCA bit of the LKSC register is set and the ECCB bit is clear. The incoming valid ESS signal received over Link A, “RxA valid ESS”, is the only one used by the ECC transmit section in Tx. The RxA port is programmed to extract the incoming ESSA bit as the valid ESS, as the

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16.0 Embedded Communication Channel Operation (Continued)

Device 2 transmitter is connected to Device 1 receiver Port A. This is accomplished by clearing the RAESS bit of the RACTL register.

ECC Receive on Port B: Device 1 communicating with Device 3 only.

Device 1: For the ECC to communicate across Link B only, the ECCA bit of the LKSC register is clear and the ECCB bit is set. The incoming valid ESS signal received over Link B, "RxB valid ESS", is the only one used by the ECC transmit section in Tx. The RxB port is programmed to extract the incoming ESSB bit as the valid ESS, as the Device 1 transmitter is connected to Device 3 receiver Port B. This is accomplished by setting the RBESS bit of the RBCTL register.

In this case, when an ECC message is transmitted, the "RxB valid ESS" signals when the message has been successfully received by the far-end Device 3. So, ECC communications only occur over Link B between Device 1 and Device 3.

Device 3: The ECCA bit of the LKSC register is clear and the ECCB bit is set. The incoming valid ESS signal received over Link B, "RxB valid ESS", is the only one used by the ECC transmit section in Tx. The RxB port is programmed to extract the incoming ESSB bit as the valid ESS, as the Device 3 transmitter is connected to Device 1 receiver Port B. This is accomplished by setting the RBESS bit of the RBCTL register.

ECC Receive on Port A and Port B: Device 1 communicating with Device 2 and Device 3.

See *Figure 18*.

Device 1: For the ECC to communicate across both Link A and Link B, the ECCB and ECCA bits of the LKSC register are both set. The incoming valid ESS signals received over Link A "RxA valid ESS" and Link B "RxB valid ESS" are both used by the ECC transmit section in Tx.

In this case, when an ECC message is transmitted, both the "RxA valid ESS" and "RxB valid ESS" signals must be used to indicate that the message has been successfully received by **both Device 2 and Device 3** before a new message can be transmitted. So ECC communications occur over both Link A and Link B.

Device 2 and 3: are configured as above for communicating with only Device 1.

Note that, when Device 1 wants to transmit a new message it must wait until both Device 2 and Device 3 indicate that they have received the last message. When Device 2 wants to transmit a new message it must only wait until Device 1 indicates that it has received the last message. Similarly for Device 3 transmitting a new message it must only wait until Device 1 indicates that it has received the last message

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16.0 Embedded Communication Channel Operation (Continued)

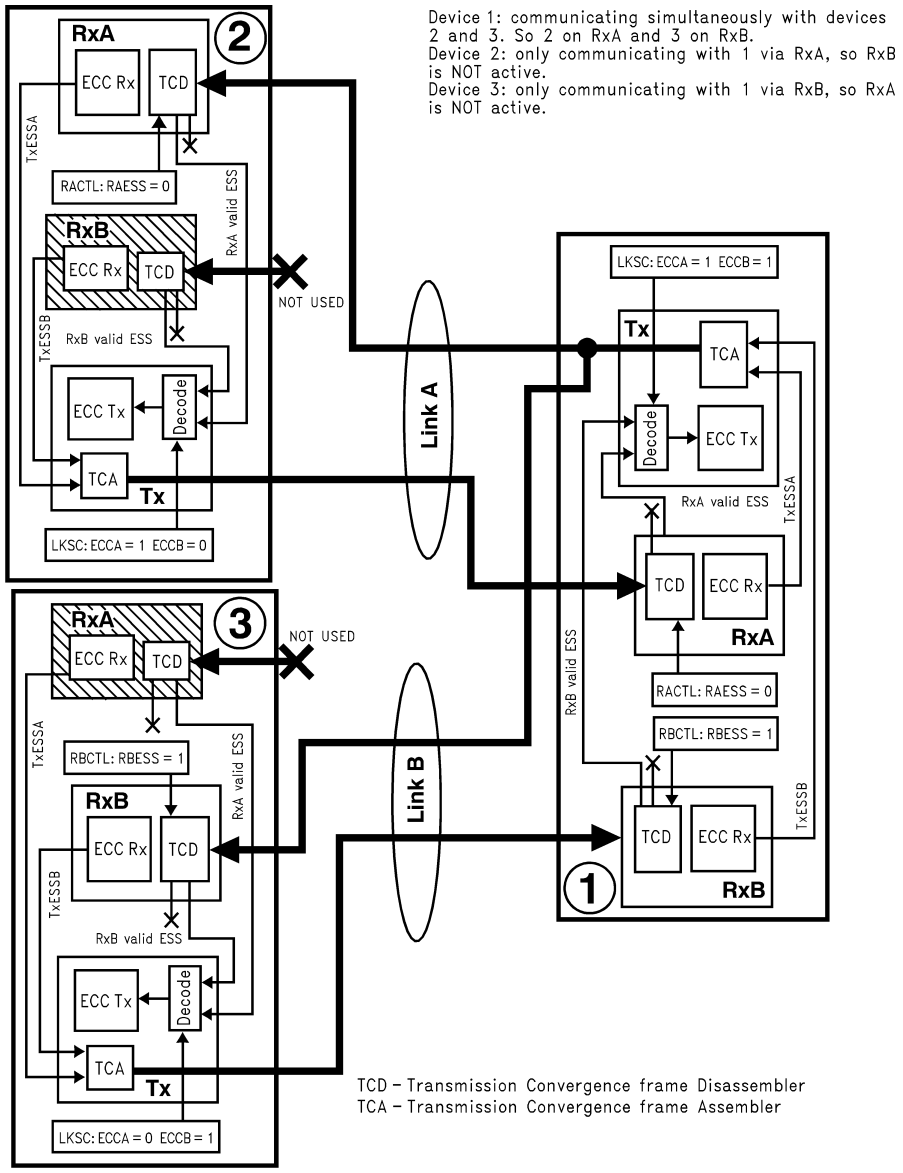

FIGURE 18. ECC Signalling with Active and Standby Links

17.0 Microprocessor Interface Operation

The DS92UT16 contains a flexible microprocessor port capable of interfacing to either Intel or Motorola processors. In addition to an 8-bit address and 8-bit data bus plus the associated bus protocol control signals, the port includes an open-drain interrupt signal. This signal may be asserted on the detection of various alarms within the device and any of the potential internal sources of this interrupt may be individually inhibited via an interrupt mask.

Powering down a Receive Port inhibits access to the associated registers. This feature saves power when a Receive Port is not in use. It allows re-reading the last value read from a register associated with that Receive Port and disallows writing to that port's registers. Receive Port A (RxA) in Power-down mode inhibits access to registers described in*Section 18.21 RECEIVE PORT A LINK LABEL — 0x20 RALL* to *Section 18.39 RECEIVE PORT A BIT ERROR COUNT — 0x43 to 0x45 RABEC2 to RABEC0*. Receive Port B (RxB) in Power-down mode inhibits access to registers described in *Section 18.40 RECEIVE PORT B LINK LABEL — 0x60 RBLL* to *Section 18.58 RECEIVE PORT B BIT ERROR COUNT — 0x83 to 0x85 RBBEC2 to RBBEC0*. The contents of these registers are not lost or altered in Power-down mode.

Typical processor Read and Write cycles for this device are shown in *Figures 19, 20, 21, 22*. The associated timing for each cycle is given in *Tables 16, 17, 18, 19*.

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17.0 Microprocessor Interface Operation (Continued)

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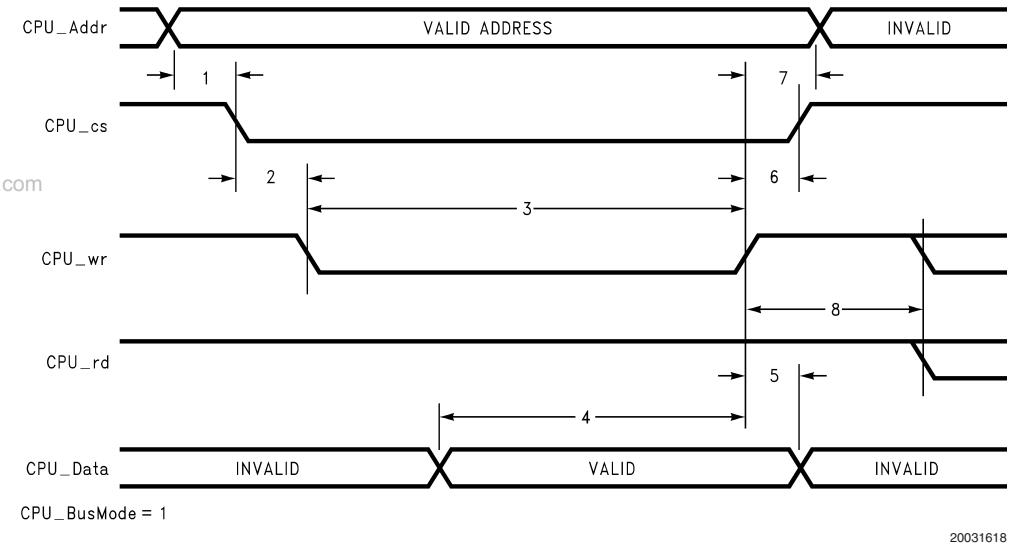

FIGURE 19. Intel Write Cycle

TABLE 16. Intel Write

No.	Parameter	Min	Max	Units
1	Address Setup Time before $\overline{\text{Chip Select}}$ Low	0		ns
2	$\overline{\text{Chip Select}}$ Setup before $\overline{\text{Write}}$ Low	5		ns
3	$\overline{\text{Write}}$ Pulse Width (Notes 6, 7)	6 cycles		
4	Data Setup before $\overline{\text{Write}}$ High (Notes 6, 7)	5 cycles		
5	Data Hold after $\overline{\text{Write}}$ High	5		ns
6	$\overline{\text{Chip Select}}$ Hold after $\overline{\text{Write}}$ High	5		ns
7	Address Hold after $\overline{\text{Write}}$ High	0		ns
8	$\overline{\text{Write}}$ Recovery Time (Notes 6, 8)	1 cycle		

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17.0 Microprocessor Interface Operation (Continued)

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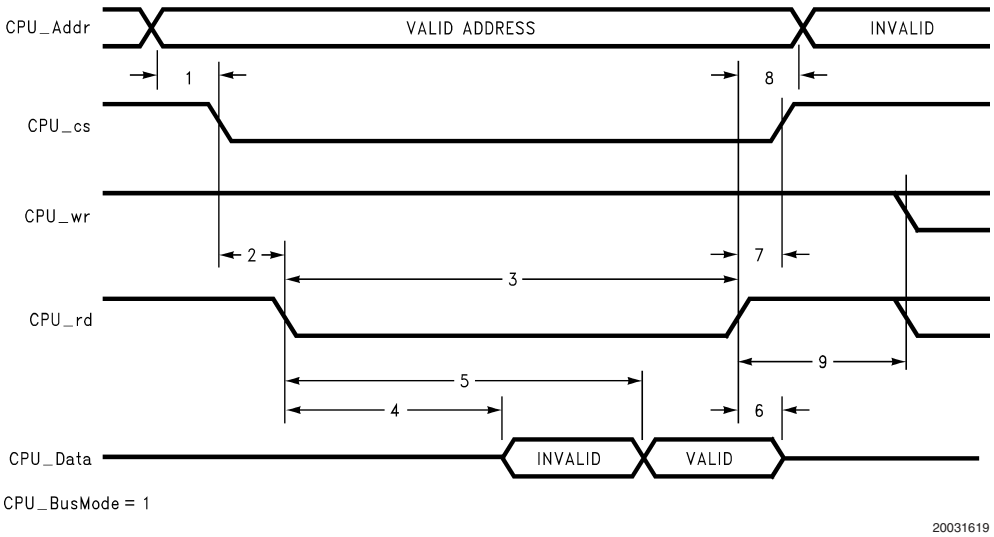

FIGURE 20. Intel Read Cycle

TABLE 17. Intel Read

No.	Parameter	Min	Max	Units
1	Address Setup Time before $\overline{\text{Chip Select}}$ Low	0		ns
2	$\overline{\text{Chip Select}}$ Setup before $\overline{\text{Write}}$ Low	0		ns
3	$\overline{\text{Read}}$ Pulse Width (Notes 6, 7)	8 cycles		
4	$\overline{\text{Read}}$ Low to Data Low Impedance		10	ns
5	$\overline{\text{Read}}$ Low to Valid Data (Notes 6, 7)		7 cycles + 15 ns	
6	$\overline{\text{Read}}$ High to Data High Impedance		15	ns
7	$\overline{\text{Chip Select}}$ Hold after $\overline{\text{Read}}$ High	0		ns
8	Address Hold after $\overline{\text{Read}}$ High	0		ns
9	$\overline{\text{Read}}$ Recovery Time (Notes 6, 8)	1 cycle		

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17.0 Microprocessor Interface Operation (Continued)

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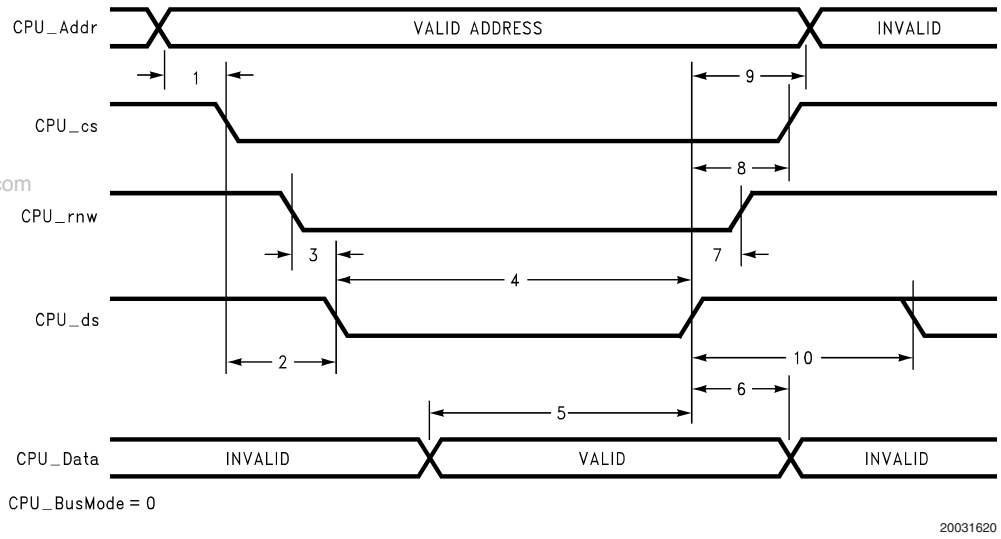

FIGURE 21. Motorola Write Cycle

TABLE 18. Motorola Write

No.	Parameter	Min	Max	Units
1	Address Setup Time before $\overline{\text{Chip Select}}$ Low	0		ns
2	$\overline{\text{Chip Select}}$ Setup before $\overline{\text{Data Strobe}}$ Low	0		ns
3	Read/$\overline{\text{Write}}$ Setup before $\overline{\text{Data Strobe}}$ Low	5		ns
4	$\overline{\text{Data Strobe}}$ Pulse Width (Notes 6, 7)	6 cycles		
5	Data Setup before $\overline{\text{Data Strobe}}$ High (Notes 6, 7)	5 cycles		
6	Data Hold after $\overline{\text{Data Strobe}}$ High	5		ns
7	Read/$\overline{\text{Write}}$ Hold after $\overline{\text{Data Strobe}}$ High	5		ns
8	$\overline{\text{Chip Select}}$ Hold after $\overline{\text{Data Strobe}}$ High	5		ns
9	Address Hold after $\overline{\text{Data Strobe}}$ High	0		ns
10	$\overline{\text{Data Strobe}}$ Recovery Time (Notes 6, 8)	1 cycle		

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17.0 Microprocessor Interface Operation (Continued)

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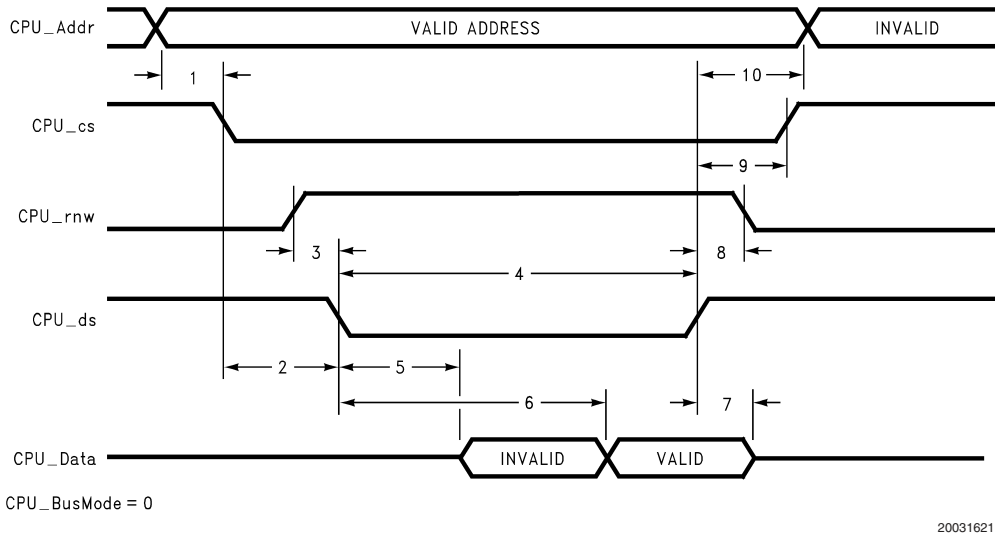

FIGURE 22. Motorola Read Cycle

TABLE 19. Motorola Read

No.	Parameter	Min	Max	Units
1	Address Setup Time before $\overline{\text{Chip Select}}$ Low	0		ns
2	$\overline{\text{Chip Select}}$ Setup before $\overline{\text{Data Strobe}}$ Low	0		ns
3	Read/$\overline{\text{Write}}$ Setup before $\overline{\text{Data Strobe}}$ Low	5		ns
4	$\overline{\text{Data Strobe}}$ Pulse Width (Notes 6, 7)	8 cycles		
5	$\overline{\text{Data Strobe}}$ Low to Data Low Impedance		10	ns
6	$\overline{\text{Data Strobe}}$ Low to Valid Data (Notes 6, 7)		7 cycles + 15 ns	
7	$\overline{\text{Data Strobe}}$ High to Data High Impedance		15	ns
8	Read/$\overline{\text{Write}}$ Hold after $\overline{\text{Data Strobe}}$ High	5		ns
9	$\overline{\text{Chip Select}}$ Hold after $\overline{\text{Data Strobe}}$ High	5		ns
10	Address Hold after $\overline{\text{Data Strobe}}$ High	0		ns
11	$\overline{\text{Data Strobe}}$ Recovery Time (Notes 6, 8)	1 cycle		

Note 6: "Cycle" must be greater than or equal to the cycle time of the slowest DS92UT16 clock.

Note 7: When an LVDS receiver loses or gains "lock", the recovered clock may stay high for up to 2.5 cycles. If a processor access is in progress to one of the registers in either of the recovered clock domains, then a READ will return the value of the last READ access, and a WRITE will not change the value of the target register. To accommodate this possible gap in the clock, 3 cycles has been added to these timings and they should therefore be regarded as worst case. If access time needs to be increased and a system is robust enough to accept these possible incorrect accesses then 3 cycles can be removed from these timings.

Note 8: A recovery time of 1 cycle is required between successive processor accesses.

SOFTWARE LOCK

Note that the device has a software lock mechanism implemented for security. This is described in *Section 6.5 CPU INTERFACE* and *Section 18.1 SOFTWARE LOCK—0x00 to 0x01 SLK0 to SLK1*.

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18.0 Register Description

This section describes all the software accessible registers in the DS92UT16. A summary of all registers is shown in *Table 20*.

TABLE 20. Register Map Summary

Register Name	Address	Software Lock	Reset Value	Section and Description
SLK0	0x00	N	0x00	18.1 Software Lock 1
SLK1	0x01	N	0x00	18.1 Software Lock 2
VID	0x02	N	(Note 9)	18.2 Version Identification
GCS	0x03	Y	0x05	18.3 General Control and Status
LVC	0x04	Y	0x3B	18.4 LVDS Control
PDUCFG	0x05	Y	0x00	18.5 PDU Configuration
IS	0x06	N	0x00	18.6 Interrupt Source
ISE	0x07	N	0x00	18.7 Interrupt Source Enables
LKSC	0x08	Y	0x34	18.8 Link Status and Control
TXLL	0x09	N	0x00	18.9 Transmit Link Label
ETXRXA	0x0A	N	0x01	18.10 ECC Transmit Buffer and Receive LVDS Alarms
ETXRXIE	0x0B	N	0x00	18.11 ECC Transmit Buffer and Receive LVDS Interrupt Enables
ETXSD	0x0C	N	0x00	18.12 ECC Transmit Buffer Send
ETXD7	0x0D	N	0x00	18.13 ECC Transmit Buffer 7
ETXD6	0x0E	N	0x00	18.13 ECC Transmit Buffer 6
ETXD5	0x0F	N	0x00	18.13 ECC Transmit Buffer 5
ETXD4	0x10	N	0x00	18.13 ECC Transmit Buffer 4
ETXD3	0x11	N	0x00	18.13 ECC Transmit Buffer 3
ETXD2	0x12	N	0x00	18.13 ECC Transmit Buffer 2
ETXD1	0x13	N	0x00	18.13 ECC Transmit Buffer 1
ETXD0	0x14	N	0x00	18.13 ECC Transmit Buffer 0
GPIO	0x15	N	0xF0	18.14 General Purpose Input/Output
TERRCTL	0x16	Y	0x00	18.15 Test Error Control
ERRBIP1	0x17	Y	0x00	18.16 BIP Error Mask 1
ERRBIP0	0x18	Y	0x00	18.16 BIP Error Mask 0
ERRHEC	0x19	Y	0x00	18.17 HEC Error Mask 0
ALBC	0x1A	N	0x00	18.18 ATM and LVDS Loopback Control
ALBMP	0x1B	N	0x00	18.19 ATM Loopback Cell MPhy
ALBCF3	0x1C	N	0x00	18.20 ATM Loopback Cell Format 3
ALBCF2	0x1D	N	0x00	18.20 ATM Loopback Cell Format 2
ALBCF1	0x1E	N	0x00	18.20 ATM Loopback Cell Format 1
ALBCF0	0x1F	N	0x00	18.20 ATM Loopback Cell Format 0
RALL	0x20	N	0x00	18.21 Receive Port A Link Label
RAELL	0x21	N	0x00	18.22 Receive Port A Expected Link Label
RALA	0x22	N	0x00	18.23 Receive Port A Local Alarms
RALIE	0x23	N	0x00	18.24 Receive Port A Local Interrupt Enables
RACTL	0x24	Y	0x01	18.25 Receive Port A Control
Reserved	0x25			
ERAD7	0x26	N	0x00	18.26 ECC Receive Buffer A 7
ERAD6	0x27	N	0x00	18.26 ECC Receive Buffer A 6
ERAD5	0x28	N	0x00	18.26 ECC Receive Buffer A 5
ERAD4	0x29	N	0x00	18.26 ECC Receive Buffer A 4
ERAD3	0x2A	N	0x00	18.26 ECC Receive Buffer A 3
ERAD2	0x2B	N	0x00	18.26 ECC Receive Buffer A 2
ERAD1	0x2C	N	0x00	18.26 ECC Receive Buffer A 1
ERAD0	0x2D	N	0x00	18.26 ECC Receive Buffer A 0

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18.0 Register Description (Continued)

TABLE 20. Register Map Summary (Continued)

Register Name	Address	Software Lock	Reset Value	Section and Description
RAHECC2	0x2E	N	0x00	18.27 Receive Port A HEC Count 2
RAHECC1	0x2F	N	0x00	18.27 Receive Port A HEC Count 1
RAHECC0	0x30	N	0x00	18.27 Receive Port A HEC Count 0
RAHECT2	0x31	N	0xFF	18.28 Receive Port A HEC Threshold 2
RAHECT1	0x32	N	0xFF	18.28 Receive Port A HEC Threshold 1
RAHECT0	0x33	N	0xFF	18.28 Receive Port A HEC Threshold 0
RABIPC2	0x34	N	0x00	18.29 Receive Port A BIP Count 2
RABIPC1	0x35	N	0x00	18.29 Receive Port A BIP Count 1
RABIPC0	0x36	N	0x00	18.29 Receive Port A BIP Count 0
RABIPT2	0x37	N	0xFF	18.30 Receive Port A BIP Threshold 2
RABIPT1	0x38	N	0xFF	18.30 Receive Port A BIP Threshold 1
RABIPT0	0x39	N	0xFF	18.30 Receive Port A BIP Threshold 0
RAPA	0x3A	N	0x00	18.31 Receive Port A Performance Alarms
RAPIE	0x3B	N	0x00	18.32 Receive Port A Performance Interrupt Enables
RARA	0x3C	N	0x0D	18.33 Receive Port A Remote Alarms
RARIE	0x3D	N	0x00	18.34 Receive Port A Remote Interrupt Enables
RAU2DLBC	0x3E	N	0x00	18.35 Receive Port A ATM Up2Down Loopback Cell Count
Unused	0x3F			
RACDT	0x40	Y	0x78	18.36 Receive Port A Cell Delineation Thresholds
RAFDT	0x41	Y	0x78	18.37 Receive Port A Frame Delineation Thresholds
RADSLKT	0x42	Y	0x88	18.38 Receive Port a Descrambler Lock Thresholds
RABEC2	0x43	N	0x00	18.38 Receive Port A Bit Error Count 2
RABEC1	0x44	N	0x00	18.38 Receive Port A Bit Error Count 1
RABEC0	0x45	N	0x00	18.38 Receive Port A Bit Error Count 0
Unused	0x46			
Reserved	0x47			
Reserved	0x48			
Unused	0x49 to 0x56			
Resered	0x57			
Reserved	0x58			
Reserved	0x59			
Reserved	0x5A			
Unused	0x5B			
Reserved	0x5C			
Reserved	0x5D			
Reserved	0x5E			
Reserved	0x5F			
RBLL	0x60	N	0x00	18.40 Receive Port B Link Label
RBELL	0x61	N	0x00	18.41 Receive Port B Expected Link Label
RBLA	0x62	N	0x00	18.42 Receive Port B Local Alarms
RBLIE	0x63	N	0x00	18.43 Receive Port B Local Interrupt Enables
RBCTL	0x64	Y	0x01	18.44 Receive Port B Control
Reserved	0x65			
ERBD7	0x66	N	0x00	18.45 ECC Receive Buffer B 7
ERBD6	0x67	N	0x00	18.45 ECC Receive Buffer B 6
ERBD5	0x68	N	0x00	18.45 ECC Receive Buffer B 5

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18.0 Register Description (Continued)

TABLE 20. Register Map Summary (Continued)

Register Name	Address	Software Lock	Reset Value	Section and Description
ERBD4	0x69	N	0x00	18.45 ECC Receive Buffer B 4
ERBD3	0x6A	N	0x00	18.45 ECC Receive Buffer B 3
ERBD2	0x6B	N	0x00	18.45 ECC Receive Buffer B 2
ERBD1	0x6C	N	0x00	18.45 ECC Receive Buffer B 1
ERBD0	0x6D	N	0x00	18.45 ECC Receive Buffer B 0
RBHECC2	0x6E	N	0x00	18.46 Receive Port B HEC Count 2
RBHECC1	0x6F	N	0x00	18.46 Receive Port B HEC Count 1
RBHECC0	0x70	N	0x00	18.46 Receive Port B HEC Count 0
RBHECT2	0x71	N	0xFF	18.47 Receive Port B HEC Threshold 2
RBHECT1	0x72	N	0xFF	18.47 Receive Port B HEC Threshold 1
RBHECT0	0x73	N	0xFF	18.47 Receive Port B HEC Threshold 0
RBBIPC2	0x74	N	0x00	18.48 Receive Port B BIP Count 2
RBBIPC1	0x75	N	0x00	18.48 Receive Port B BIP Count 1
RBBIPC0	0x76	N	0x00	18.48 Receive Port B BIP Count 0
RBBIPT2	0x77	N	0xFF	18.49 Receive Port B BIP Threshold 2
RBBIPT1	0x78	N	0xFF	18.49 Receive Port B BIP Threshold 1
RBBIPT0	0x79	N	0xFF	18.49 Receive Port B BIP Threshold 0
RBPA	0x7A	N	0x00	18.50 Receive Port B Performance Alarms
RBPIE	0x7B	N	0x00	18.51 Receive Port B Performance Interrupt Enables
RBRA	0x7C	N	0x0D	18.52 Receive Port B Remote Alarms
RBRIE	0x7D	N	0x00	18.53 Receive Port B Remote Interrupt Enables
RBU2DLBC	0x7E	N	0x00	18.54 Receive Port B ATM Up2Down Loopback Cell Count
Unused	0x7F			
RBCDT	0x80	Y	0x78	18.55 Receive Port B Cell Delineation Thresholds
RBFDT	0x81	Y	0x78	18.56 Receive Port B Frame Delineation Thresholds
RBDSLKT	0x82	Y	0x88	18.57 Receive Port B Descrambler Lock Thresholds
RBBEC2	0x83	N	0x00	18.58 Receive Port Bit Error Count 2
RBBEC1	0x84	N	0x00	18.58 Receive Port Bit Error Count 1
RBBEC0	0x85	N	0x00	18.58 Receive Port Bit Error Count 0
Unused	0x86			
Reserved	0x87			
Reserved	0x88			
Unused	0x89 to 0x96			
Reserved	0x97			
Reserved	0x98			
Reserved	0x99			
Reserved	0x9A			
Unused	0x9B			
Reserved	0x9C			
Reserved	0x9D			
Reserved	0x9E			
Reserved	0x9F			
UCFG	0xA0	Y	0x00	18.59 UTOPIA Configuration
UCPL3	0xA1	Y	0x7F	18.60 UTPOIA Connected Port List 3
UCPL2	0xA2	Y	0xFF	18.60 UTPOIA Connected Port List 2
UCPL1	0xA3	Y	0xFF	18.60 UTPOIA Connected Port List 1

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18.0 Register Description (Continued)

TABLE 20. Register Map Summary (Continued)

Register Name	Address	Software Lock	Reset Value	Section and Description
UCPL0	0xA4	Y	0xFF	18.60 UTPOIA Connected Port List 0
Reserved	0xA5			
UCSPL	0xA6	Y	0x01	18.61 UTOPIA Connected Sub-Port List
USPAL	0xA7	Y	0x00	18.62 UTOPIA Sub-Port Address Location
USPAM	0xA8	Y	0x07	18.63 UTOPIA Sub-Port Address Mask
MTBQT30	0xA9	Y	0x04	18.64 MTB Queue Threshold 30
MTBQT29	0xAA	Y	0x04	18.64 MTB Queue Threshold 29
MTBQT28	0xAB	Y	0x04	18.64 MTB Queue Threshold 28
MTBQT27	0xAC	Y	0x04	18.64 MTB Queue Threshold 27
MTBQT26	0xAD	Y	0x04	18.64 MTB Queue Threshold 26
MTBQT25	0xAE	Y	0x04	18.64 MTB Queue Threshold 25
MTBQT24	0xAF	Y	0x04	18.64 MTB Queue Threshold 24
MTBQT23	0xB0	Y	0x04	18.64 MTB Queue Threshold 23
MTBQT22	0xB1	Y	0x04	18.64 MTB Queue Threshold 22
MTBQT21	0xB2	Y	0x04	18.64 MTB Queue Threshold 21
MTBQT20	0xB3	Y	0x04	18.64 MTB Queue Threshold 20
MTBQT19	0xB4	Y	0x04	18.64 MTB Queue Threshold 19
MTBQT18	0xB5	Y	0x04	18.64 MTB Queue Threshold 18
MTBQT17	0xB6	Y	0x04	18.64 MTB Queue Threshold 17
MTBQT16	0xB7	Y	0x04	18.64 MTB Queue Threshold 16
MTBQT15	0xB8	Y	0x04	18.64 MTB Queue Threshold 15
MTBQT14	0xB9	Y	0x04	18.64 MTB Queue Threshold 14
MTBQT13	0xBA	Y	0x04	18.64 MTB Queue Threshold 13
MTBQT12	0xBB	Y	0x04	18.64 MTB Queue Threshold 12
MTBQT11	0xBC	Y	0x04	18.64 MTB Queue Threshold 11
MTBQT10	0xBD	Y	0x04	18.64 MTB Queue Threshold 10
MTBQT9	0xBE	Y	0x04	18.64 MTB Queue Threshold 9
MTBQT8	0xBF	Y	0x04	18.64 MTB Queue Threshold 8
MTBQT7	0xC0	Y	0x04	18.64 MTB Queue Threshold 7
MTBQT6	0xC1	Y	0x04	18.64 MTB Queue Threshold 6
MTBQT5	0xC2	Y	0x04	18.64 MTB Queue Threshold 5
MTBQT4	0xC3	Y	0x04	18.64 MTB Queue Threshold 4
MTBQT3	0xC4	Y	0x04	18.64 MTB Queue Threshold 3
MTBQT2	0xC5	Y	0x04	18.64 MTB Queue Threshold 2
MTBQT1	0xC6	Y	0x04	18.64 MTB Queue Threshold 1
MTBQT0	0xC7	Y	0x04	18.64 MTB Queue Threshold 0
MTBQFL3	0xC8	N	0x00	18.65 MTB Queue Full 3
MTBQFL2	0xC9	N	0x00	18.65 MTB Queue Full 2
MTBQFL1	0xCA	N	0x00	18.65 MTB Queue Full 1
MTBQFL0	0xCB	N	0x00	18.65 MTB Queue Full 0
MTBQE3	0xCC	N	0x7F	18.66 MTB Queue Empty 3
MTBQE2	0xCD	N	0xFF	18.66 MTB Queue Empty 2
MTBQE1	0xCE	N	0xFF	18.66 MTB Queue Empty 1
MTBQE0	0xCF	N	0xFF	18.66 MTB Queue Empty 0
MTBQF3	0xD0	Y	0x00	18.67 MTB Queue Flush 3
MTBQF2	0xD1	Y	0x00	18.67 MTB Queue Flush 2
MTBQF1	0xD2	Y	0x00	18.67 MTB Queue Flush 1

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18.0 Register Description (Continued)

TABLE 20. Register Map Summary (Continued)

Register Name	Address	Software Lock	Reset Value	Section and Description
MTBQF0	0xD3	Y	0x00	18.67 MTB Queue Flush 0
MTBCF3	0xD4	Y	0x00	18.68 MTB Cell Flush 3
MTBCF2	0xD5	Y	0x00	18.68 MTB Cell Flush 2
MTBCF1	0xD6	Y	0x00	18.68 MTB Cell Flush 1
MTBCF0	0xD7	Y	0x00	18.68 MTB Cell Flush 0
QFL	0xD8	Y	0x00	18.69 Queue Flush
MTBQOV3	0xD9	N	0x00	18.70 MTB Queue Overflow 3
MTBQOV2	0xDA	N	0x00	18.70 MTB Queue Overflow 2
MTBQOV1	0xDB	N	0x00	18.70 MTB Queue Overflow 1
MTBQOV0	0xDC	N	0x00	18.70 MTB Queue Overflow 0
Unused	0xDD to 0xDF			
D2ULBCC	0xE0	N	0x00	18.71 ATM Down2Up Loopback Cell Count
UAA	0xE1	N	0x00	18.72 UTOPIA and ATM Alarms
UAIE	0xE2	N	0x00	18.73 UTOPIA and ATM Interrupt Enables
Unused	0xE3 to 0xF6			
ALFLT3	0xF7	N	0xFF	18.74 ATM Loopback Cell Filter 3
ALFLT2	0xF8	N	0xFF	18.74 ATM Loopback Cell Filter 2
ALFLT1	0xF9	N	0xFF	18.74 ATM Loopback Cell Filter 1
ALFLT0	0xFA	N	0xFF	18.74 ATM Loopback Cell Filter 0
Unused	0xFB			
Reserved	0xFC			
Reserved	0xFD			
Reserved	0xFE			
Reserved	0xFF			

Note 9: The reset value of the VID register will be different for various versions of the device.

Note 10: All configuration and control registers can be read by the processor to determine the status of the DS92UT16.

Note 11: All reserved (register bits for internal use only) and unused (no register) bits will be read as zero and should be written as zero to ensure future compatibility.

Note 12: Writing to read only register bits has no affect.

18.1 SOFTWARE LOCK — 0x00 to 0x01 SLK0 to SLK1

TABLE 21. SLK0–SLK1

	7	6	5	4	3	2	1	0
SLK0 0x00	0	0	0	0	0	0	0	0
SLK1 0x01	0	0	0	0	0	0	0	0

Type: Read as 0x00

Software Lock: No

Reset Value: 0x00

The Software Lock registers are used to implement a software lock mechanism on configuration and control registers to prevent spurious software changes to the device which may affect its operation. On reset the Software Lock is ON. Writes to registers protected by this lock will have no affect. To switch the lock OFF the following sequence of writes to the SLK registers must occur.

UNLOCK SEQUENCE

1. Write data 0x00 to SLK0.

2. Write data 0xFF to SLK1.

The software lock is now OFF and those registers protected by it can be successfully written to.

To switch the lock back On the following sequence of writes to the SLK registers must occur.

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18.0 Register Description (Continued)

LOCK SEQUENCE

1. Write data 0xDE to SLK0.

2. Write data 0xAD to SLK1.

The software lock is now ON and those registers protected by it cannot be written to.

The order of the writes in each sequence must be followed. However, the sequence does not have to be contiguous. For instance, the processor can **Write data 0xDE to SLK0**, then carry out further read/write cycles to this or another device before completing the LOCK sequence with **Write data 0xAD to SLK1**.

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The full lock or unlock sequence must be completed to take effect.

The status of the Software Lock can be read at any time from the SLOCK bit of the GCS register.

18.2 VERSION IDENTIFICATION — 0x02 VID

TABLE 22. VID

7	6	5	4	3	2	1	0
VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]

Type: Read only

Software Lock: No

Reset Value: (Note 9)

- **VID[7:0]** Version identification number. NOTE that this is only a proprietary Version number and that the standard Device ID register is contained in the JTAG TAP controller as described in *Section 19.0 Test Features*.

18.3 GENERAL CONTROL AND STATUS — 0x03 GCS

TABLE 23. GCS

7	6	5	4	3	2	1	0
Reserved	Reserved	GIE	LT	RESET	CTI	TIS	SLOCK

Type: Bits[5:2] Read/Write
Bit[1:0] Read Only

Software Lock: Yes

Reset Value: 0x05

- **GIE** The Global Interrupt Enable enables the device interrupt output pin CPU_INT. Set = Interrupts enabled and Clear = Interrupts disabled.
- **LT** The Loop Timing bit enables the connection of the Active Rx port recovered clock to the LVDS Transmit clock (the active Rx port is as defined by the LBA bit of the LKSC register). LT Set = LVDS Tx clock sourced from Active Rx port recovered clock. LT Clear = LVDS Tx clock sourced from LVDS_TxClk pin.
- **RESET** Set = Software reset of all registers except this bit. The Software Lock status as refiected by SLOCK is also not affected by a software reset.
- **CTI** Configuration Traffic Inhibit. The setting of this bit initiates the Traffic Inhibit functionality, which stops traffic flow. The UTOPIA interface will stop transmitting and receiving cells, the LVDS transmit section will transmit Idle cells and the incoming cells on the active LVDS receive port will be discarded. The MTB and FIB queues must also be flushed. This bit should be set by the processor whenever the device is being fundamentally reconfigured from the default settings, specifically whenever any of the PDUCFG, UCFG, USPAL or USPAM registers are being changed. The processor should set this bit before changing any of the above mentioned register settings. This will initiate Traffic Inhibit. The TIS bit should then be polled until set to confirm that traffic is inhibited. **Note that the MTB and FIB queues MUST be flushed at this stage. This is accomplished with the FIBFL and MTBFL bits of the QFL register described in *Section 18.69 QUEUE FLUSH — 0xD8 QFL*.** The device can now be safely reconfigured. When the TIS bit is set, then traffic is inhibited and the device can safely be reconfigured. When configuration is completed, then the CTI bit can be cleared by the processor and normal operation resumed. **Note that CTI is set on reset so the device is in Traffic Inhibit mode.** See *Section 10.0 Configuration and Traffic Inhibit Operation*.
- **TIS** Traffic Inhibit Status. This bit reflects the status of the Traffic Inhibit functionality. When set then traffic is inhibited as described for the CTI bit above. When clear then the device operates normally. The setting of the CTI bit will initiate Traffic Inhibit which sets the TIS bit. Clearing of the CTI bit clears the TIS bit.
- **SLOCK** This refiects the status of the Software Lock functionality. Set = Software lock ON and Clear = Software Lock OFF. The processor can use this bit to determine the Software Lock functionality status when writing to lockable registers.

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18.0 Register Description (Continued)

18.4 LVDS CONTROL — 0x04 LVC

TABLE 24. LVC

7	6	5	4	3	2	1	0
Reserved	Reserved	TXPWDN	TXBDEN	TXADEN	TXSYNC	RAPWDN	RBPWDN

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Type: Read/Write
Software Lock: Yes
Reset Value: 0x3B

The LVDS control register configures the LVDS serializer/deserializers.

- **TXPWDN** Transmit section LVDS power down. Set = Power Up and Clear = Power Down. This register value is combined with the LVDS_TxPwdn pin to generate the internal power down setting for transmit section. If either this register bit or the LVDS_TxPwdn pin is clear then the transmit LVDS section is powered down.
- **TBDEN** LVDS B Transmit data output enable. Set = Enable and Clear = Disable. This register value is combined with the LVDS_BDenb pin to generate the output enable for the LVDS transmit section B. If either this register bit or the LVDS_BDenb pin is clear then the transmitter B output is disabled.
- **TXADEN** LVDS A Transmit data output enable. Set = Enable and Clear = Disable. This register value is combined with the LVDS_ADenb pin to generate the output enable for the LVDS transmit section A. If either this register bit or the LVDS_ADenb pin is clear then the transmitter A output is disabled.
- **TXSYNC** Transmit LVDS synchronization pattern. Set = Enable and Clear = Disable. This register value is combined with the LVDS_Synch pin to generate the SYNCH input to the LVDS transmit section. If either this register bit or the LVDS_Synch pin is set then SYNCH patterns are output from the LVDS transmit section.
- **RAPWDN** Receive Port A LVDS power down. Set = Power Up and Clear = Power Down. This register value is combined with the LVDS_APwdn pin to generate the internal power down setting for receive Port A. If either this register bit or the LVDS_APwdn pin is clear then the receive Port A LVDS section is powered down.
- **RBPWDN** Receive Port B LVDS power down. Set = Power Up and Clear = Power Down. This register value is combined with the LVDS_BPwdn pin to generate the internal power down setting for receive Port B. If either this register bit or the LVDS_BPwdn pin is clear then the receive Port B LVDS section is powered down.

18.5 PDU CONFIGURATION — 0x05 PDUCFG

TABLE 25. PDUCFG

7	6	5	4	3	2	1	0
Reserved	UP[2]	UP[1]	UP[0]	UDF	UA[2]	UA[1]	UA[0]

Type: Read/Write
Software Lock: Yes
Reset Value: 0x00

The PDU Configuration register defines the contents and size of the PDU cells. The register does this by defining the size of the User Prepend, whether or not the UDF is to be transported, and the size of the User Append. The total size of the PDU must be in the range 52 to 64 bytes. Therefore the total size of the User Prepend, plus UDF and User Append must not exceed 12 bytes. Further, as the DS92UT16 operates with an internal 16 bit data path the size of the User Prepend and User Append is defined in words (16 bits/2 bytes). If the UDF is to be transported, then in UTOPIA 16-bit mode UDF1 and UDF2 bytes are transported and in UTOPIA 8-bit mode the UDF byte is transported.

- **UP[2:0]** The UP bits define the length of the User Prepend. Range 0 to 6 words.
- **UDF** The UDF bit when set indicates that the UDF word should be transported. When cleared the UDF word is not transported.
- **UA[2:0]** The UA bits define the length of the User Append. Range 0 to 6 words.

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18.0 Register Description (Continued)

18.6 INTERRUPT SOURCE — 0x06 IS

TABLE 26. IS

7	6	5	4	3	2	1	0
UAA	ETXRXA	RBLA	RBPA	RBRA	RALA	RAPA	RARA

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Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The Interrupt Source register reflects the source of pending interrupts.

- **UAA** Set = Interrupt pending in the UAA register.
- **ETXRXA** Set = Interrupt pending in the ETXRXA register.
- **RBLA** Set = Interrupt pending in the RBLA register.
- **RBPA** Set = Interrupt pending in the RBPA register.
- **RBRA** Set = Interrupt pending in the RBRA register.
- **RALA** Set = Interrupt pending in the RALA register.
- **RAPA** Set = Interrupt pending in the RAPA register.
- **RARA** Set = Interrupt pending in the RARA register.

18.7 INTERRUPT SOURCE ENABLES — 0x07 ISE

TABLE 27. ISE

7	6	5	4	3	2	1	0
UAAIE	ETXRXAIE	RBLAIE	RBPAIE	RBRAIE	RALAIE	RAPAIE	RARAIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the corresponding alarms in the IS register. Set = interrupt sources enabled and Clear = interrupt sources disabled.

18.8 LINK STATUS AND CONTROL — 0x08 LKSC

TABLE 28. LKSC

7	6	5	4	3	2	1	0
RDSLKOV	SCDIS	CEN	ECCA	ECCB	ABSC	LBA	FTXSCR

Type: Bits[7:3] Read/Write
Bit[2] Read Only
Bits[1:0] Read/Write

Software Lock: Yes

Reset Value: 0x34

The Link Status and Control register is the general control for the transmit and receive links.

- **RDSLOV** Remote Descrambler Lock Override. When clear, this allows the transmitter/assembler to automatically send Idle cells containing the Scrambler sequence whenever the remote descrambler falls out of lock. This determined by either the RARDSLK bit or the RBRDSLK bit clear, depending on the Active receive port defined by the LBA bit. This action should force the remote descrambler back into lock. Traffic cells are not transmitted during this action until remote descrambler lock is achieved. If the RDSLKOV bit is set then the actual status of the remote descrambler (RARDSLK or RBRDSLK) is ignored and it is assumed that the remote descrambler is locked and therefore normal traffic cells are transmitted.
- **SCDIS** Transmit scrambler disable. When set the scrambler is disabled and unscrambled data is transmitted. When clear the scrambler is active and transmitted data is scrambled.
- **CEN** Coset enable. When set then the optional coset $x^6 + x^4 + x^2 + 1$ is added to the generated CRC-8 used for the HEC. When clear the coset is not added to the HEC.

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18.0 Register Description (Continued)

- **ECCA** ECC active on Port A bit. When set, this indicates to the ECC transmit section that the ETXBR bit (*Section 18.10 ECC TRANSMIT BUFFER AND RECEIVE LVDS ALARMS—0x0A ETXRXA*) will be set only when the far end ECC receiver connected to Port A indicates via the ECC signalling (received ESSA or ESSB signal, as selected by bit RAESS of register RACTL) over Port A that the message has been received successfully. When clear the ECC signalling over Port A will be ignored as the ECC Port A receiver is disabled and the ERABF bit will be held clear. See *Section 16.0 Embedded Communication Channel Operation*.
- **ECCB** ECC active on Port B bit. When set, this indicates to the ECC transmit section that the ETXBR bit (*Section 18.10 ECC TRANSMIT BUFFER AND RECEIVE LVDS ALARMS—0x0A ETXRXA*) will be set only when the far end ECC receiver connected to Port B indicates via the ECC signalling (received ESSA or ESSB signal, as selected by bit RBESS of register RBCTL) over Port B that the message has been received successfully. When clear the ECC signalling over Port B will be ignored as the ECC Port B receiver is disabled and the ERBBF bit will be held clear. See *Section 16.0 Embedded Communication Channel Operation*.
- **ECCB and ECCA** Note that when both these bits are clear, then the ECC transmitter and both receivers are inactive. The ETXBR, ETXSD, ERABF and ERBBF bits will be held clear, the ECC signalling is ignored and no messages are transmitted or received. See *Section 16.0 Embedded Communication Channel Operation*.
- **ECCB and ECCA** Note that when both these bits are set, this indicates to the ECC transmit section that the ETXBR bit will only be set when both far end ECC receivers indicate that the transmitted message has been received successfully (received ESS signals). See *Section 16.0 Embedded Communication Channel Operation*.
- **ABSC** A/B Switch completed. When switching active traffic receive port this bit can be polled by the processor to determine when the switch has been completed successfully. A change of the LBA bit will clear this bit. The ABSC bit should then be polled by the processor. The ABSC bit is set by the hardware when the active port switching is completed. This bit relates to the LBA active traffic switching bit and is **not** related to the ECC port switching bit ECCA and ECCB. See *Section 13.0 Switching Receive Ports*.
- **LBA** Local receive port A or B control. When this bit is set, then Receive Port B is Active and Port A is Standby. When clear, then Port A is Active and Port B is Standby. This bit defines the active traffic port and does not affect which ECC channel is active as defined by the ECCA and ECCB bits above. See *Section 13.0 Switching Receive Ports*.
- **FTXSCR** Force Transmit Scrambler Sequence. When set this forces the transmission of the scrambler sequence which is used to lock the descrambler.

18.9 TRANSMIT LINK LABEL—0x09 TXLL

TABLE 29. TXLL

7	6	5	4	3	2	1	0
TXLL[7]	TXLL[6]	TXLL[5]	TXLL[4]	TXLL[3]	TXLL[2]	TXLL[1]	TXLL[0]

Type: Read/Write

Software Lock: No

Reset Value: 0x00

The Transmit Link Label register defines the contents of the Link Trace Label byte transmitted in TC6.

- **TXLL[7:0]** Transmitted Link Trace Label byte contents.

18.10 ECC TRANSMIT BUFFER AND RECEIVE LVDS ALARMS—0x0A ETXRXA

TABLE 30. ETXRXA

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	LLOSC	LLOSA	LLOSB	ETXBR

Type: Bits[3:1] Read only/Clear on Read
Bit[0] Read only

Software Lock: No

Reset Value: 0x01

This register contains the status of the ECC transmit buffer and the LOCK signals from the two LVDS receive ports. When set the LLOSA, LLOSB and LLOSC bits will raise an interrupt if the corresponding interrupt enable bit is set.

- **LLOSA** Local Loss Of Signal on receive Port A. When set this will also clear all the bits in the Receive Port A Remote Alarms register.
- **LLOSB** Local Loss Of Signal on receive Port B. When set this will also clear all the bits in the Receive Port B Remote Alarms register.
- **LLOSC** Local Loss Of Signal Change. When set this indicates that there has been a change of value for either LLOSA or LLOSB.

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18.0 Register Description (Continued)

The ETXBR register bit indicates that the ECC transmit section has successfully transmitted the full ECC message consisting of the 8 data bytes contained in registers ETXD7–ETXD0 and a new message can be assembled and transmitted. This is a read only bit that the processor must examine before assembling a new ECC message in the ETXD7–ETXD0 data registers.

If this bit is not set then any writes to ETXD7–ETXD0 will have no affect.

On reset the ETXBR will be set indicating a message can be assembled for transmission. The processor assembles a message in the ETXD7–ETXD0 data registers. To send the message the processor simply sets the ETXSD register bit. This clears the ETXBR bit which prevents write access to the ETXD7–ETXD0 registers so that the message cannot be overwritten. When the far end ECC receiver indicates via the ECC signalling that the message has been received successfully, then the near end ECC transmitter ETXSD bit is cleared and the ETXBR bit is set. The ETXBR bit, when set, may raise a processor interrupt if the corresponding interrupt enable is set. The processor can therefore detect that a message has been successfully transmitted either by the interrupt or by polling the ETXBR bit.

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Note that the ETXBR bit **cannot** be cleared on a read of this register but can only be cleared by setting the ETXSD bit of the ETXSD register.

- **ETXBR** The ETXBR bit, when set, indicates that the current ECC message has been successfully transmitted and a new message can be assembled. If this bit is not set, then the current message has not been received at the far end and a new message cannot be assembled. The ETXBR bit is cleared by the setting of the ETXSD bit. The ETXBR bit is set either by the far end successfully receiving a message or by the processor clearing the ETXSD bit.

18.11 ECC Tx BUFFER AND Rx LVDS INTERRUPT ENABLES — 0x0B ETXRXIE

TABLE 31. ETXRXIE

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	LLOSCIE	LLOSAIE	LLOSBIE	ETXBRIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the alarms in the ETXRXA register. Set = interrupt enabled and Clear = interrupt disabled.

18.12 ECC TRANSMIT BUFFER SEND — 0x0C ETXSD

TABLE 32. ETXSD

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ETXSD

Type: Read/Write

Software Lock: No

Reset Value: 0x00

The ETXSD register bit controls the transmission of an ECC message.

- **ETXSD** The setting of the ETXSD bit initiates the transmission of the ECC message in the ETXD0–ETXD7 data registers, but only if the ETXBR is also set. Once transmission of a message has been initiated in this way, it will proceed until the far end ECC receiver indicates, via the ECC signalling, that the message has been received successfully. The ETXSD bit will be cleared and the ETXBR register bit is set automatically when the far end ECC receiver indicates that the message has been received successfully. To re-send the same message simply set the ETXSD bit again.
- See *Section 16.0 Embedded Communication Channel Operation* for a complete description of the Embedded Communication Channel operation.
- The processor can halt transmission of a message by clearing the ETXSD bit which sets the ETXBR bit to enable a new message to be constructed in the ETXD7–ETXD0 registers.

18.13 ECC TRANSMIT BUFFER — 0x0D to 0x14 ETXD7 to ETXD0

TABLE 33. ETXD7–ETXD0

	7	6	5	4	3	2	1	0
ETXD7 0x0D	ETXD7[7]	ETXD7[6]	ETXD7[5]	ETXD7[4]	ETXD7[3]	ETXD7[2]	ETXD7[1]	ETXD7[0]
ETXD6 0x0E	ETXD6[7]	ETXD6[6]	ETXD6[5]	ETXD6[4]	ETXD6[3]	ETXD6[2]	ETXD6[1]	ETXD6[0]
ETXD5 0x0F	ETXD5[7]	ETXD5[6]	ETXD5[5]	ETXD5[4]	ETXD5[3]	ETXD5[2]	ETXD5[1]	ETXD5[0]
ETXD4 0x10	ETXD4[7]	ETXD4[6]	ETXD4[5]	ETXD4[4]	ETXD4[3]	ETXD4[2]	ETXD4[1]	ETXD4[0]
ETXD3 0x11	ETXD3[7]	ETXD3[6]	ETXD3[5]	ETXD3[4]	ETXD3[3]	ETXD3[2]	ETXD3[1]	ETXD3[0]

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18.0 Register Description (Continued)

TABLE 33. ETXD7–ETXD0 (Continued)

	7	6	5	4	3	2	1	0
ETXD2 0x12	ETXD2[7]	ETXD2[6]	ETXD2[5]	ETXD2[4]	ETXD2[3]	ETXD2[2]	ETXD2[1]	ETXD2[0]
ETXD1 0x13	ETXD1[7]	ETXD1[6]	ETXD1[5]	ETXD1[4]	ETXD1[3]	ETXD1[2]	ETXD1[1]	ETXD1[0]
ETXD0 0x14	ETXD0[7]	ETXD0[6]	ETXD0[5]	ETXD0[4]	ETXD0[3]	ETXD0[2]	ETXD0[1]	ETXD0[0]

Type: Read/Write

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Software Lock: No

Reset Value: 0x00

The ETXD7, ETXD6, ETXD5, ETXD4, ETXD3, ETXD2, ETXD1 and ETXD0 registers contain the ECC message to be transmitted.

- **ETXD7–ETXD0** When the ETXBR bit is set, then these registers have full read/write access to allow flexible assembly of the ECC message before initiating transmission by setting the ETXSD bit. When the ETXBR is clear during message transmission, these registers are read only so that the message being transmitted cannot be overwritten and corrupted.

18.14 GENERAL PURPOSE INPUT OUTPUT — 0x15 GPIO

TABLE 34. GPIO

7	6	5	4	3	2	1	0
DDR[3]	DDR[2]	DDR[1]	DDR[0]	IO[3]	IO[2]	IO[1]	IO[0]

Type: Bits [7:4] Read/Write

Bits[3:0] are Read Only when GPIO[3:0] are defined as Inputs, and Read/Write when GPIO[3:0] are defined as Outputs.

Software Lock: No

Reset Value: 0xF0

The General Purpose Input/Output register controls the four general purpose input/output pins GPIO[3:0].

- **DDR[3:0]** The Data Direction bits DDR[3:0] define the function of the GPIO[3:0] pins. When a DDR bit is set the corresponding GPIO pin is an input and when the DDR bit is clear the corresponding GPIO pin is an output.
- **IO[3:0]** The IO bits reflect the value of the GPIO pins. When defined as an output by the DDR bit, then the IO bit value is driven out on the corresponding GPIO pin. When defined as an input by the DDR bit, then the IO bit value captures the incoming value on the corresponding GPIO pin.

18.15 TEST ERROR CONTROL — 0x16 TERRCTL

TABLE 35. TERRCTL

7	6	5	4	3	2	1	0
EBRST[3]	EBRST[2]	EBRST[1]	EBRST[0]	ERFHEC	ERCHEC	ERBIP	TXPRBS

Type: Read/Write

Software Lock: Yes

Reset Value: 0x00

The Test Error Control register is used to control the transmission of a PRBS pattern for Bit Error Rate testing, or to introduce HEC and BIP errors so that the Cell Delineation, Frame Delineation, Descrambler Lock and performance monitoring functions can be tested. This is a test register and should not be used on live traffic. The exact nature of the errored HEC and BIP bytes is determined by the ERRBIP1, ERRBIP0 and ERRHEC registers.

- **EBRST[3:0]** The Error Burst bits EBRST[3:0] define the number of consecutive erred HEC's and/or BIP's to be generated and transmitted.
- **ERFHEC** The Error Frame HEC bit, when set, will cause EBRST consecutive Frame HEC's to be erred. When this has been completed the hardware will clear this bit.
- **ERCHEC** The Error Cell HEC bit, when set, will cause EBRST consecutive Cell HEC's to be erred. When this has been completed the hardware will clear this bit.
- **ERBIP** The Error BIP bit, when set, will cause EBRST consecutive BIP's to be erred. When this has been completed the hardware will clear this bit.
- **TXPRBS** Transmit PRBS pattern. When set, the transmit section sends the raw scrambler pseudo-random sequence (polynomial $x^{31} + x^{28} + 1$). No data is transmitted. The TCS Assembler will be paused and no cells will be read from the FIB queue. The far end receiver can lock to this PRBS pattern to count bit errors if the RABEC/RBBEC bit is set in the RACTL/RBCTL register. This is not a live traffic test.

18.16 ERROR BIP MASK — 0x17 to 0x18 ERRBIP1 to ERRBIP0

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18.0 Register Description (Continued)

TABLE 36. ERRBIP1–ERRBIP0

	7	6	5	4	3	2	1	0
ERRBIP1 0x17	EBIP1[7]	EBIP1[6]	EBIP1[5]	EBIP1[4]	EBIP1[3]	EBIP1[2]	EBIP1[1]	EBIP1[0]
ERRBIP0 0x18	EBIP0[7]	EBIP0[6]	EBIP0[5]	EBIP0[4]	EBIP0[3]	EBIP0[2]	EBIP0[1]	EBIP0[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x00

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The Error BIP Mask registers controls how errors are introduced into the BIP bytes when bit ERBIP of the TERRCTL register is set. If a bit is set in the ERRBIP1 or ERRBIP0 register then the corresponding bit in the transmitted BIP is inverted. ERRBIP1 corresponds to the first transmitted BIP byte and ERRBIP0 corresponds to the second transmitted BIP byte.

18.17 ERROR HEC MASK—0x19 ERRHEC

TABLE 37. ERRHEC

7	6	5	4	3	2	1	0
EHEC[7]	EHEC[6]	EHEC[5]	EHEC[4]	EHEC[3]	EHEC[2]	EHEC[1]	EHEC[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x00

The Error HEC Mask register controls the introduction of errors into the HEC byte when the ERFHEC and/or ERCHEC bits of the TERRCTL register are set. If a bit is set in the ERRHEC register, then the corresponding bit in the transmitted HEC is inverted.

18.18 ATM AND LVDS LOOPBACK CONTROL—0x1A ALBC

TABLE 38. ALBC

7	6	5	4	3	2	1	0
Reserved	LNEN	LNSEL	LCLA	LCLB	TXLVLB	D2ULB	D2DLB

Type: Read/Write

Software Lock: No

Reset Value: 0x00

The ATM and LVDS Loopback Control register controls the loopback functions of the device.

Note that the LVDS Line and Local Loopbacks should not be on at the same time.

- **LNEN** LVDS Line Loopback enable. Set = ON and Clear = OFF. When set this enables the loopback of the LVDS receive section, determined by LNSEL, to the transmitter.
- **LNSEL** LVDS Line Loopback receive section select. Set = Receive B and Clear = Receive A.
- **LCLA** LVDS Local Loopback transmit to receive Port A. Set = ON and Clear = OFF.
- **LCLB** LVDS Local Loopback transmit to receive Port B. Set = ON and Clear = OFF.
- **TXLVLB** When set, this initiates the transmission of a single loopback cell Down Bridge on the LVDS transmitter. This cell will be transmitted with the MPhy address defined in the ALBMP register and will have a header format as defined in the ALBCF3–ALBCF0 registers. When the bit is clear, the cell has been transmitted. The processor sets the bit to initiate the transmission and then polls this bit to determine when transmission has been completed, at which time the process can be repeated to transmit another loopback cell. See *Section 15.1 ATM CELL LOOPBACK*.
- **D2ULB** When set, this enables the ATM Down2Up loopback circuit. Any incoming cells from the UTOPIA interface which match the format of ALBCF3–ALBCF0, masked by the ALFLT3–ALFLT0 registers, are not stored in the FIB traffic queue but transmitted back out over the UTOPIA interface. See *Section 15.1 ATM CELL LOOPBACK*.
- **U2DLB** When set, this enables the ATM Up2Down loopback circuit. Any incoming cells from the active LVDS receive port which match the format of ALBCF3–ALBCF0 registers, masked by the ALFLT3–ALFLT0 registers, are not stored in the MTB traffic queue but transmitted back out over the LVDS transmitter. Note that although there are two independent receivers, this loopback is designed to operate on live traffic and so only affects cells from the active receiver as defined by the LBA bit of the LKSC register. See *Section 15.1 ATM CELL LOOPBACK*.

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18.0 Register Description (Continued)

18.19 ATM LOOPBACK MPhy—0x1B ALBMP

TABLE 39. ALBMP

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LBMP[4]	LBMP[3]	LBMP[2]	LBMP[1]	LBMP[0]

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Type: Read/Write
Software Lock: No
Reset Value: 0x00

The ATM Loopback MPhy register defines the MPhy address attached to the ATM loopback cell. Setting the TXLVLB bit in the ALBC register initiates these loopback cells.

- **LBMP[4:0]** ATM loopback cell five bit MPhy address.

18.20 ATM LOOPBACK CELL FORMAT —0x1C to 0x1F ALBCF3 to ALBCF0

TABLE 40. ALBCF3–ALBCF0

	7	6	5	4	3	2	1	0
ALBCF3 0x1C	ALBCF3[7]	ALBCF3[6]	ALBCF3[5]	ALBCF3[4]	ALBCF3[3]	ALBCF3[2]	ALBCF3[1]	ALBCF3[0]
ALBCF2 0x1D	ALBCF2[7]	ALBCF2[6]	ALBCF2[5]	ALBCF2[4]	ALBCF2[3]	ALBCF2[2]	ALBCF2[1]	ALBCF2[0]
ALBCF1 0x1E	ALBCF1[7]	ALBCF1[6]	ALBCF1[5]	ALBCF1[4]	ALBCF1[3]	ALBCF1[2]	ALBCF1[1]	ALBCF1[0]
ALBCF0 0x1F	ALBCF0[7]	ALBCF0[6]	ALBCF0[5]	ALBCF0[4]	ALBCF0[3]	ALBCF0[2]	ALBCF0[1]	ALBCF0[0]

Type: Read/Write
Software Lock: No
Reset Value: 0x00

The ALBCF3, ALBCF2, ALBCF1 and ALBCF0 registers define the format of the ATM loopback cell header.

- **ALBCF3[7:0]** Loopback Cell header byte H1 format.
- **ALBCF2[7:0]** Loopback Cell header byte H2 format.
- **ALBCF1[7:0]** Loopback Cell header byte H3 format.
- **ALBCF0[7:0]** Loopback Cell header byte H4 format.

18.21 RECEIVE PORT A LINK LABEL—0x20 RALL

TABLE 41. RALL

7	6	5	4	3	2	1	0
RALL[7]	RALL[6]	RALL[5]	RALL[4]	RALL[3]	RALL[2]	RALL[1]	RALL[0]

Type: Read only
Software Lock: No
Reset Value: 0x00

The Receive Port A Link Label register contains the Link Trace Label byte received in TC6 on receive Port A. Whenever the received link label changes value, the RALLC alarm bit in the RALA register is set, which will raise an interrupt if the corresponding interrupt enable bit is set.

- **RALL[7:0]** Port A Received Link Trace Label byte contents.

18.22 RECEIVE PORT A EXPECTED LINK LABEL—0x21 RAELL

TABLE 42. RAELL

7	6	5	4	3	2	1	0
RAELL[7]	RAELL[6]	RAELL[5]	RAELL[4]	RAELL[3]	RAELL[2]	RAELL[1]	RAELL[0]

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18.0 Register Description (Continued)

Type: Read only

Software Lock: No

Reset Value: 0x00

The Receive Port A Expected Link Label register defines the expected contents of the Link Trace Label byte received in TC6 on receive Port A. If the actual received value, as stored in the RALL register is not the same as the expected value defined here the RALLM alarm bit in the RALA register is set, which may raise a processor interrupt if the corresponding interrupt enable is set.

- **RAELL[7:0]** Port A Expected Received Link Trace Label byte contents.

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18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA

TABLE 43. RALA

7	6	5	4	3	2	1	0
Reserved	RALLC	RALLM	RALCS	RALDSLL	RALTCLL	RALFF	ERABF

Type: Bits[6:1] Read only/Clear on Read
Bit[0] Read/Write

Software Lock: No

Reset Value: 0x00

The Receive Port A Local Alarms register contains information on the status of the Port A disassembler. When set RALLC, RALLM, RALDSLL, RALTCLL and RALFLL will raise an interrupt if the corresponding interrupt enable bits are set. Also a change in value on RALDSLL, RALTCLL or RALFLL will set the RALCS bit which will raise an interrupt if the corresponding interrupt enable bit is set.

- **RALLC** Receive Port A, Local Link Label Change of Status. Set = Change in RALL register value.
- **RALLM** Receive Port A, Local Link Label Mismatch. Set = Received link label RALL different than expected link label RAELL.
- **RALCS** Receive Port A, Local Change of Status. Set = change in value of RALDSLL, RALTCLL or RALFLL bits
- **RALDSLL** Receive Port A, Local Descrambler Loss of Lock. Set = Out of Lock and Clear = Lock.
- **RALLTCLL** Receive Port A, Local Transport Container Delineation Loss of Lock. Set = Out of Lock and Clear = Lock.
- **RALFLL** Receive Port A, Local Frame Delineation Loss of Lock. Set = Out of Lock and Clear = Lock.

The ERABF register bit indicates that the ECC receive section for Port A has successfully received a full ECC message consisting of the 8 data bytes contained in registers ERAD7–ERAD0, and the message can now be read by the processor.

On reset, the ERABF will be clear indicating no valid message has been received. When a valid message is received and stored in the ERAD7–ERAD0 data registers, the ERABF bit will be set and will raise an interrupt if the corresponding interrupt enable bit is set. Therefore, the processor can detect a received message on the interrupt or by polling the ERABF bit. When the processor has finished reading the message from the ERAD7–ERAD0 data registers and is ready to receive a new message it simply clears the ERABF bit. When a full message has been successfully received this is communicated to the far-end device via the ECC signalling.

- **ERABF** The ERABF bit, when set, indicates that ERAD7–ERAD0 data registers contain a full valid received message. The data in the ERAD7–ERAD0 data registers cannot be overwritten with a new received message while ERABF is set. When ERABF is cleared this allows the ERAD7–ERAD0 data registers to be overwritten with a new received message.

18.24 RECEIVE PORT A LOCAL INTERRUPT ENABLES—0x23 RALIE

TABLE 44. RALIE

7	6	5	4	3	2	1	0
Reserved	RALLCIE	RALLMIE	RALCSIE	RALDSLLIE	RALTCLLIE	RALFLLIE	ERABFIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the alarms in the RALA register. Set = interrupt enabled and Clear = interrupt disabled.

18.25 RECEIVE PORT A CONTROL—0x24 RACTL

TABLE 45. RACTL

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RAESS	RABEC	RADFLK	RACDIS

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18.0 Register Description (Continued)

Type: Read/Write

Software Lock: Yes

Reset Value: 0x01

The Receive Port A Control register defines the operation of the Port A TCS DisAssembler section.

- **RAESS** Receive Port A, Valid Received ESS bit select. Two ESS bits are received in the Remote Alarm and Signaling Byte as described in *Section 6.3.7.1 Remote Alarm and Signaling Byte*. Only one of these received bits may be designated as valid. The valid bit is extracted and passed to the ECC transmit section as the ECC signaling bit (ESS) received on Port A. When RAESS is set then the Remote Alarm and Signaling Byte bit[1], ESSB, is selected as valid and bit[2], ESSA is ignored. When RAESS is clear then the Remote Alarm and Signaling Byte bit[2], ESSA, is selected as valid and bit[1], ESSB is ignored. The names ESSA and ESSB of these bits refers to the remote receiver port from which they originated and are **not** associated with the local receivers Port A and Port B. See *Section 16.0 Embedded Communication Channel Operation*.
- **RABEC** Receive Port A, Bit Error Count mode. When set the receiver expects to receive the raw scrambler PRBS pattern. See TXPRBS bit of the TERRCTL register. The descrambler will lock to this sequence and then count individual bit errors in the PRBS stream. This bit error count will be refiected in the RABEC2–RABEC0 registers. As there is no data cell delineation, the frame delineation will be lost. This is not a live traffic test.
- **RADFLK** Receive Port A, Descrambler Force Lock. When set the descrambler will be forced out of lock and will immediately begin to re-lock. The hardware will clear this bit and the descrambler lock status can be monitored on the RALDSLL bit of the RALA register, see *Section 18.23 RECEIVE PORT A LOCAL ALARMS —0x22 RALA*.
- **RACDIS** Receive Port A, Cell Discard. When set then cells with an errored HEC are discarded.

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18.26 ECC RECEIVE BUFFER A — 0x26 to 0x2D ERAD7 to ERAD0

TABLE 46. ERAD7–ERAD0

	7	6	5	4	3	2	1	0
ERAD7 0x26	ERAD7[7]	ERAD7[6]	ERAD7[5]	ERAD7[4]	ERAD7[3]	ERAD7[2]	ERAD7[1]	ERAD7[0]
ERAD6 0x27	ERAD6[7]	ERAD6[6]	ERAD6[5]	ERAD6[4]	ERAD6[3]	ERAD6[2]	ERAD6[1]	ERAD6[0]
ERAD5 0x28	ERAD5[7]	ERAD5[6]	ERAD5[5]	ERAD5[4]	ERAD5[3]	ERAD5[2]	ERAD5[1]	ERAD5[0]
ERAD4 0x29	ERAD4[7]	ERAD4[6]	ERAD4[5]	ERAD4[4]	ERAD4[3]	ERAD4[2]	ERAD4[1]	ERAD4[0]
ERAD3 0x2A	ERAD3[7]	ERAD3[6]	ERAD3[5]	ERAD3[4]	ERAD3[3]	ERAD3[2]	ERAD3[1]	ERAD3[0]
ERAD2 0x2B	ERAD2[7]	ERAD2[6]	ERAD2[5]	ERAD2[4]	ERAD2[3]	ERAD2[2]	ERAD2[1]	ERAD2[0]
ERAD1 0x2C	ERAD1[7]	ERAD1[6]	ERAD1[5]	ERAD1[4]	ERAD1[3]	ERAD1[2]	ERAD1[1]	ERAD1[0]
ERAD0 0x2D	ERAD0[7]	ERAD0[6]	ERAD0[5]	ERAD0[4]	ERAD0[3]	ERAD0[2]	ERAD0[1]	ERAD0[0]

Type: Read only

Software Lock: No

Reset Value: 0x00

The ERAD7, ERAD6, ERAD5, ERAD4, ERAD3, ERAD2, ERAD1 and ERAD0 registers contain the Port A received ECC message.

- **ERAD7–ERAD0** When the ERABF bit is set then these registers contain a valid received ECC message for Port A and cannot be overwritten by any incoming messages. When the ERABF bit is clear these registers may not contain a valid message and should not be interpreted as such.

18.27 RECEIVE PORT A HEC COUNT — 0x2E to 0x30 RAHECC2 to RAHECC0

TABLE 47. RAHECC2–RAHECC0

	7	6	5	4	3	2	1	0
RAHECC2 0x2E	RAHECC2[7]	RAHECC2[6]	RAHECC2[5]	RAHECC2[4]	RAHECC2[3]	RAHECC2[2]	RAHECC2[1]	RAHECC2[0]
RAHECC1 0x2F	RAHECC1[7]	RAHECC1[6]	RAHECC1[5]	RAHECC1[4]	RAHECC1[3]	RAHECC1[2]	RAHECC1[1]	RAHECC1[0]
RAHECC0 0x30	RAHECC0[7]	RAHECC0[6]	RAHECC0[5]	RAHECC0[4]	RAHECC0[3]	RAHECC0[2]	RAHECC0[1]	RAHECC0[0]

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The RAHECC2, RAHECC1 and RAHECC0 registers contain the Port A received errored HEC count.

- **RAHECC2–RAHECC0** This register must be read in the order of most significant byte RAHECC2 first and least significant byte RAHECC0 last or the value read will not be valid. This counter will not roll-over from 0xFFFFFF to 0x000000 but will stick at 0xFFFFFF.

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18.0 Register Description (Continued)

18.28 RECEIVE PORT A HEC THRESHOLD — 0x31 to 0x33 RAHECT2 to RAHECT0

TABLE 48. RAHECT2–RAHECT0

	7	6	5	4	3	2	1	0
RAHECT2 0x31	RAHECT2[7]	RAHECT2[6]	RAHECT2[5]	RAHECT2[4]	RAHECT2[3]	RAHECT2[2]	RAHECT2[1]	RAHECT2[0]
RAHECT1 0x32	RAHECT1[7]	RAHECT1[6]	RAHECT1[5]	RAHECT1[4]	RAHECT1[3]	RAHECT1[2]	RAHECT1[1]	RAHECT1[0]
RAHECT0 0x33	RAHECT0[7]	RAHECT0[6]	RAHECT0[5]	RAHECT0[4]	RAHECT0[3]	RAHECT0[2]	RAHECT0[1]	RAHECT0[0]

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Type: Read/Write

Software Lock: No

Reset Value: 0xFF

The RAHECT2, RAHECT1 and RAHECT0 registers contain the Port A received erred HEC threshold. When the error count RAHECC equals the threshold RAHECT then the RAXHEC alarm will be set.

These registers should not be set to all zeroes.

- **RAHECT2–RAHECT0** Most significant byte RAHECT2 and least significant byte RAHECT0.

18.29 RECEIVE PORT A BIP COUNT — 0x34 to 0x36 RABIPC2 to RABIPC0

TABLE 49. RABIPC2–RABIPC0

	7	6	5	4	3	2	1	0
RABIPC2 0x34	RABIPC2[7]	RABIPC2[6]	RABIPC2[5]	RABIPC2[4]	RABIPC2[3]	RABIPC2[2]	RABIPC2[1]	RABIPC2[0]
RABIPC1 0x35	RABIPC1[7]	RABIPC1[6]	RABIPC1[5]	RABIPC1[4]	RABIPC1[3]	RABIPC1[2]	RABIPC1[1]	RABIPC1[0]
RABIPC0 0x36	RABIPC0[7]	RABIPC0[6]	RABIPC0[5]	RABIPC0[4]	RABIPC0[3]	RABIPC0[2]	RABIPC0[1]	RABIPC0[0]

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The RABIPC2, RABIPC1 and RABIPC0 registers contain the Port A received errored BIP count.

- **RABIPC2–RABIPC0** This register must be read in the order of most significant byte RABIPC2 first and least significant byte RABIPC0 last or the value read will not be valid. This counter will not roll-over from 0xFFFFFF to 0x000000 but will stick at 0xFFFFFF.

18.30 RECEIVE PORT A BIP THRESHOLD — 0x36 to 0x39 RABIPT2 to RABIPT0

TABLE 50. RABIPT2–RABIPT0

	7	6	5	4	3	2	1	0
RABIPT2 0x37	RABIPT2[7]	RABIPT2[6]	RABIPT2[5]	RABIPT2[4]	RABIPT2[3]	RABIPT2[2]	RABIPT2[1]	RABIPT2[0]
RABIPT1 0x38	RABIPT1[7]	RABIPT1[6]	RABIPT1[5]	RABIPT1[4]	RABIPT1[3]	RABIPT1[2]	RABIPT1[1]	RABIPT1[0]
RABIPT0 0x39	RABIPT0[7]	RABIPT0[6]	RABIPT0[5]	RABIPT0[4]	RABIPT0[3]	RABIPT0[2]	RABIPT0[1]	RABIPT0[0]

Type: Read/Write

Software Lock: No

Reset Value: 0xFF

The RABIPT2, RABIPT1 and RABIPT0 registers contain the Port A received errored BIP threshold. When the error count RABIPC equals the threshold RABIPT then the RAXBIP alarm will be set.

These registers should not be set to all zeroes.

- **RABIPT2–RABIPT0** Most significant byte RABIPT2 and least significant byte RABIPT0.

18.31 RECEIVE PORT A PERFORMANCE ALARMS — 0x3A RAPA

TABLE 51. RAPA

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RAXHEC	RAXBIP

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

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18.0 Register Description (Continued)

The Receive Port A Performance Alarms register contains information about the error performance of Port A. When set RAXHEC and RAXBIP will raise an interrupt if the corresponding interrupt enable bits are set.

- **RAXHEC** Receive Port A, Excessive HEC Errors. Set = Number of HEC errors counted in RAHECC is equal to or greater than the threshold set in RAHECT. This bit is set when RAHECC = RAHECT and can only be cleared by a read of this register.
- **RAXBIP** Receive Port A, Excessive BIP Errors. Set = Number of BIP errors counted in RABIPC is equal to or greater than the threshold set in RABIPT. This bit is set when RABIPC = RABIPT and can only be cleared by a read of this register.

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18.32 RECEIVE PORT A PERFORMANCE INTERRUPT ENABLES — 0x3B RAPIE

TABLE 52. RAPIE

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RAXHECIE	RAXBIPIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the alarms in the RAPA register. Set = interrupt enabled and Clear = interrupt disabled.

18.33 RECEIVE PORT A REMOTE STATUS AND ALARMS — 0x3C RARA

TABLE 53. RARA

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RARCS	RARLOSA	RARLOSB	RARBA	RARDSLL

Type: Bits[4:2] and [0] Read only/Clear on Read
Bit[1] Read only

Software Lock: No

Reset Value: 0x0D

The Receive Port A Remote Status and Alarms register contains information on the status of the far-end device, which is connected to Port A. On a local Loss of Signal on Port A, LLOSA alarm, these bits return to their reset values. When set, the RARLOSA, RARLOSB, RARBA, and RARDSLL bits will raise an interrupt if the corresponding interrupt enable is set. Also, a change in value on RARLOSA, RARLOSB, RARDSLL or RARBA will set the RARCS bit. When set, the RARCS bit will raise an interrupt if the corresponding interrupt enable is set.

- **RARCS** Receive Port A, Remote Change of Status at far end device LVDS receive Ports.
- **RARLOSA** Receive Port A, Remote Loss Of Signal at far end device LVDS receive Port A.
- **RARLOSB** Receive Port A, Remote Loss Of Signal at far end device LVDS receive Port B.
- **RARBA** Receive Port A, Remote far end device active receive Port. Set = Port B active and Clear = Port A active. Note that this bit, if set, will not clear on a read of this register.
- **RARDSLL** Receive Port A, Remote far end device active receive port Descrambler Loss of Lock. Set = Out of Lock and Clear = Lock.

18.34 RECEIVE PORT A REMOTE INTERRUPT ENABLES — 0x3D RARIE

TABLE 54. RARIE

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RARCSIE	RARLOSAIE	RARLOSBIE	RARBAIE	RARDSLLIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the alarms in the RARA register. Set = interrupt enabled and Clear = interrupt disabled.

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18.0 Register Description (Continued)

18.35 RECEIVE PORT A UP2DOWN LOOPBACK CELL COUNT — 0x3E RAU2DLBC

TABLE 55. RAU2DLBC

7	6	5	4	3	2	1	0
RAU2DLBC[7]	RAU2DLBC[6]	RAU2DLBC[5]	RAU2DLBC[4]	RAU2DLBC[3]	RAU2DLBC[2]	RAU2DLBC[1]	RAU2DLBC[0]

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Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The Receive Port A Up2Down Loopback Cell Count register counts the number of incoming loopback cells detected from the Port A LVDS interface when Up2Down loopback is enabled with the U2DLB bit of the ALBC register, see *Section 18.18 ATM AND LVDS LOOPBACK CONTROL — 0x1A ALBC*. Note that this counter is incremented when an incoming loopback cell is received and that this differs from the functionality of the Down2Up Loopback Cell Count register, see *Section 18.71 ATM DOWN2UP LOOPBACK CELL COUNT — 0xE0 D2ULBCC*.

- **RAU2DLBC[7:0]** Port A Up2Down Loopback Cell Count value. This register will not roll-over from 0x00 to 0xFF but will stick at 0xFF.

18.36 RECEIVE PORT A CELL DELINEATION THRESHOLDS — 0x40 RACDT

TABLE 56. RACDT

7	6	5	4	3	2	1	0
ALPHA[3]	ALPHA[2]	ALPHA[1]	ALPHA[0]	DELTA[3]	DELTA[2]	DELTA[1]	DELTA[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x78

The Receive Port A Cell and Transport Container Delineation Thresholds register controls the operation of the Port A cell delineation state machine. The cell delineation lock status is reflected in the RALTCLL bit of the RALA register.

- **ALPHA[3:0]** When in lock this is the number of consecutive incorrect cell HEC's required to lose cell delineation lock.
- **DELTA[3:0]** When out of lock this is the number of consecutive correct cell HEC's required to gain cell delineation lock.

18.37 RECEIVE PORT A FRAME DELINEATION THRESHOLDS — 0x41 RAFDT

TABLE 57. RAFDT

7	6	5	4	3	2	1	0
MU[3]	MU[2]	MU[1]	MU[0]	SIGMA[3]	SIGMA[2]	SIGMA[1]	SIGMA[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x78

The Receive Port A Frame Delineation Thresholds register controls the operation of the Port A frame delineation state machine. The frame delineation lock status is refiected in the RALFLL bit of the RALA register.

- **MU[3:0]** When in lock this is the number of consecutive incorrect cell HEC's required to lose frame delineation lock.
- **SIGMA[3:0]** When out of lock this is the number of consecutive correct frame HEC's required to gain frame delineation lock.

18.38 RECEIVE PORT A DESCRAMBLER LOCK THRESHOLDS — 0x42 RADSLKT

TABLE 58. RADSLKT

7	6	5	4	3	2	1	0
PSI[3]	PSI[2]	PSI[1]	PSI[0]	RHO[3]	RHO[2]	RHO[1]	RHO[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x88

The Receive Port A Descrambler Lock Thresholds register controls the operation of the Port A descrambler lock state machine confidence counter. The descrambler lock status is reflected in the RALDSLL bit of the RALA register.

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18.0 Register Description (Continued)

- **PSI[3:0]** When in lock this is the threshold that the descrambler confidence counter must reach to lose descrambler lock. When in lock the descrambler confidence counter increments on incorrect HEC predictions and decrements on good HEC predictions.
- **RHO[3:0]** When out of lock this is the threshold that the descrambler confidence counter must reach to gain descrambler lock. When out of lock the descrambler confidence counter decrements on incorrect HEC predictions and increments on good HEC predictions.

18.39 RECEIVE PORT A BIT ERROR COUNT — 0x43 to 0x45 RABEC2 to RABEC0

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TABLE 59. RABEC2–RABEC0

	7	6	5	4	3	2	1	0
RABEC2 0x43	RABEC2[7]	RABEC2[6]	RABEC2[5]	RABEC2[4]	RABEC2[3]	RABEC2[2]	RABEC2[1]	RABEC2[0]
RABEC1 0x44	RABEC1[7]	RABEC1[6]	RABEC1[5]	RABEC1[4]	RABEC1[3]	RABEC1[2]	RABEC1[1]	RABEC1[0]
RABEC0 0x45	RABEC0[7]	RABEC0[6]	RABEC0[5]	RABEC0[4]	RABEC0[3]	RABEC0[2]	RABEC0[1]	RABEC0[0]

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The RABEC2, RABEC1 and RABEC0 registers contain the Port A received bit error count whenever the RABEC bit of the RACTL register is set. If the RABEC bit of the RACTL register is clear these registers are cleared.

- **RABEC2–RABEC0** This register must be read in the order of most significant byte RABEC2 first and least significant byte RABEC0 last, or the value read will not be valid. This counter will not roll-over from 0xFFFFFF to 0x000000 but will stick at 0xFFFFFF.

18.40 RECEIVE PORT B LINK LABEL — 0x60 RBLL

TABLE 60. RBLL

7	6	5	4	3	2	1	0
RBLL[7]	RBLL[6]	RBLL[5]	RBLL[4]	RBLL[3]	RBLL[2]	RBLL[1]	RBLL[0]

Type: Read only

Software Lock: No

Reset Value: 0x00

The Receive Port B Link Label register contains the Link Trace Label byte received in TC6 on receive Port B. Whenever the received link label changes value, the RBLLC alarm bit in the RBLA register is set, which will raise an interrupt if the corresponding interrupt enable bit is set.

- **RBLL[7:0]** Port B Received Link Trace Label byte contents.

18.41 RECEIVE PORT B EXPECTED LINK LABEL — 0x61 RBELL

TABLE 61. RBELL

7	6	5	4	3	2	1	0
RBELL[7]	RBELL[6]	RBELL[5]	RBELL[4]	RBELL[3]	RBELL[2]	RBELL[1]	RBELL[0]

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18.0 Register Description (Continued)

Type: Read/Write

Software Lock: No

Reset Value: 0x00

The Receive Port B Expected Link Label register defines the expected contents of the Link Trace Label byte received in TC6 on receive Port B. If the actual received value, as stored in the RBLL register is not the same as the expected value defined here the RBLLM alarm bit in the RBLA register is set, which may raise a processor interrupt if the corresponding interrupt enable is set.

- **RBELL[7:0]** Port B Expected Received Link Trace Label byte contents.

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18.42 RECEIVE PORT B LOCAL ALARMS — 0x62 RBLA

TABLE 62. RBLA

7	6	5	4	3	2	1	0
Reserved	RBLLC	RBLLM	RBLCS	RBLDSLL	RBLTCLL	RBLFLL	ERBBF

Type: Bits[6:1] Read only/Clear on Read
Bit[0] Read/Write

Software Lock: No

Reset Value: 0x00

The Receive Port B Local Alarms register contains information on the status of the Port B disassembler. When set, RBLLC, RBLLM, RBLDSLL, RBLTCLL, and RBLFLL will raise an interrupt if the corresponding interrupt enable bits are set. Also, a change in value on RBLDSLL, RBLTCLL and RBLFLL will set the RBLCS bit, which will raise an interrupt if the corresponding interrupt enable bit is set.

- **RBLLC** Receive Port B, Local Link Label Change of Status. Set = Change in RBLL register value.
- **RBLLM** Receive Port B, Local Link Label Mismatch. Set = Received link label RBLL different than expected link label RBELL.
- **RBLCS** Receive Port B, Local Change of Status. Set = change in value of RBLDSLL, RBLTCLL or RBLFLL bits.
- **RBLDSLL** Receive Port B, Local Descrambler Loss of Lock. Set = Out of Lock and Clear = Lock.
- **RBLTCLL** Receive Port B, Local Transport Container Delineation Loss of Lock. Set = Out of Lock and Clear = Lock.
- **RBLFLL** Receive Port B, Local Frame Delineation Loss of Lock. Set = Out of Lock and Clear = Lock.

The ERBBF register bit indicates that the ECC receive section for Port B has successfully received a full ECC message consisting of the 8 data bytes contained in registers ERBD7–ERBD0 and a the message can now be read by the processor.

On reset, the ERBBF will be clear indicating no valid message has been received. When a valid message is received and stored in the ERBD7–ERBD0 data registers, the ERBBF bit will be set and will raise an interrupt if the corresponding interrupt enable bit is set. Therefore, the processor can detect a received message on the interrupt or by polling the ERBBF bit. When the processor has finished reading the message from the ERBD7–ERBD0 data registers and is ready to receive a new message, it simply clears the ERBBF bit. When a full message has been successfully received, this is communicated to the far-end device via the ECC signalling.

- **ERBBF** The ERBBF bit, when set, indicates that ERBD7–ERBD0 data registers contain a full valid received message. The data in the ERBD7–ERBD0 data registers cannot be overwritten with a new received message while ERBBF is set. When ERBBF is cleared, this allows the ERBD7–ERBD0 data registers to be overwritten with a new received message.

18.43 RECEIVE PORT B LOCAL INTERRUPT ENABLES — 0x63 RBLIE

TABLE 63. RBLIE

7	6	5	4	3	2	1	0
Reserved	RBLLCIE	RBLLMIE	RBLCSIE	RBLSLLIE	RBLTCLLIE	RBLFLLIE	ERBBFIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the alarms in the RBLA register. Set = interrupt enabled and Clear = interrupt disabled.

18.44 RECEIVE PORT B CONTROL — 0x64 RBCTL

TABLE 64. RBCTL

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RBESS	RBBEC	RBDFLK	RBCDIS

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18.0 Register Description (Continued)

Type: Read/Write

Software Lock: Yes

Reset Value: 0x01

The Receive Port B Control register defines the operation of the Port B TCS DisAssembler section.

- **RBESS** Receive Port B, Valid Received ESS bit select. Two ESS bits are received in the Remote Alarm and Signaling Byte as described in *Section 6.3.7.1 Remote Alarm and Signaling Byte*. Only one of these received bits may be designated as valid. The valid bit is extracted and passed to the ECC transmit section as the ECC signaling bit (ESS) received on Port B. When RBESS is set, then the Remote Alarm and Signaling Byte bit[1], ESSB, is selected as valid and bit[2], ESSA is ignored. When RBESS is clear then the Remote Alarm and Signaling Byte bit[2], ESSA, is selected as valid and bit[1], ESSB is ignored. The names ESSA and ESSB of these bits refers to the remote receiver port from which they originated and are **not** associated with the local receivers Port A and Port B. See *Section 16.0 Embedded Communication Channel Operation*.
- **RBBEC** Receive Port B, Bit Error Count mode. When set the receiver expects to receive the raw scrambler PRBS pattern. See TXPRBS bit of the TERRCTL register. The descrambler will lock to this sequence and then count individual bit errors in the PRBS stream. This bit error count will be refiected in the RBBEC2–RBBEC0 registers. As there is no data cell delineation, the frame delineation will be lost. This is not a live traffic test.
- **RBDFLK** Receive Port B, Descrambler Force Lock. When set the descrambler will be forced out of lock and will immediately begin to re-lock. The hardware will clear this bit and the descrambler lock status can be monitored on the RBLDSLL bit of the RBLA register, see *Section 18.42 RECEIVE PORT B LOCAL ALARMS — 0x62 RBLA*.
- **RBCDIS** Receive Port B, Cell Discard. When set then cells with an errored HEC are discarded.

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18.45 ECC RECEIVE BUFFER B — 0x66 to 0x6D ERBD7 to ERBD0

TABLE 65. ERBD7–ERBD0

	7	6	5	4	3	2	1	0
ERBD7 0x66	ERBD7[7]	ERBD7[6]	ERBD7[5]	ERBD7[4]	ERBD7[3]	ERBD7[2]	ERBD7[1]	ERBD7[0]
ERBD6 0x67	ERBD6[7]	ERBD6[6]	ERBD6[5]	ERBD6[4]	ERBD6[3]	ERBD6[2]	ERBD6[1]	ERBD6[0]
ERBD5 0x68	ERBD5[7]	ERBD5[6]	ERBD5[5]	ERBD5[4]	ERBD5[3]	ERBD5[2]	ERBD5[1]	ERBD5[0]
ERBD4 0x69	ERBD4[7]	ERBD4[6]	ERBD4[5]	ERBD4[4]	ERBD4[3]	ERBD4[2]	ERBD4[1]	ERBD4[0]
ERBD3 0x6A	ERBD3[7]	ERBD3[6]	ERBD3[5]	ERBD3[4]	ERBD3[3]	ERBD3[2]	ERBD3[1]	ERBD3[0]
ERBD2 0x6B	ERBD2[7]	ERBD2[6]	ERBD2[5]	ERBD2[4]	ERBD2[3]	ERBD2[2]	ERBD2[1]	ERBD2[0]
ERBD1 0x6C	ERBD1[7]	ERBD1[6]	ERBD1[5]	ERBD1[4]	ERBD1[3]	ERBD1[2]	ERBD1[1]	ERBD1[0]
ERBD0 0x6D	ERBD0[7]	ERBD0[6]	ERBD0[5]	ERBD0[4]	ERBD0[3]	ERBD0[2]	ERBD0[1]	ERBD0[0]

Type: Read only

Software Lock: No

Reset Value: 0x00

The ERBD7, ERBD6, ERBD5, ERBD4, ERBD3, ERBD2, ERBD1, and ERBD0 registers contain the Port B received ECC message.

- **ERBD7–ERBD0** When the ERBBF bit is set, then these registers contain a valid received ECC message for Port B and cannot be overwritten by any incoming messages. When the ERBBF bit is clear, these registers may not contain a valid message and should not be interpreted as such.

18.46 RECEIVE PORT B HEC COUNT — 0x6E to 0x70 RBHECC2 to RBHECC0

TABLE 66. RBHECC2–RBHECC0

	7	6	5	4	3	2	1	0
RBHECC2 0x6E	RBHECC2[7]	RBHECC2[6]	RBHECC2[5]	RBHECC2[4]	RBHECC2[3]	RBHECC2[2]	RBHECC2[1]	RBHECC2[0]
RBHECC1 0x6F	RBHECC1[7]	RBHECC1[6]	RBHECC1[5]	RBHECC1[4]	RBHECC1[3]	RBHECC1[2]	RBHECC1[1]	RBHECC1[0]
RBHECC0 0x70	RBHECC0[7]	RBHECC0[6]	RBHECC0[5]	RBHECC0[4]	RBHECC0[3]	RBHECC0[2]	RBHECC0[1]	RBHECC0[0]

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The RBHECC2, RBHECC1 and RBHECC0 registers contain the Port B received errored HEC count.

- **RBHECC2–RBHECC0** This register must be read in the order of most significant byte RBHECC2 first and least significant byte RBHECC0 or the value read will not be valid. This counter will not roll-over from 0xFFFFFF to 0x000000 but will stick at 0xFFFFFF.

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18.0 Register Description (Continued)

18.47 RECEIVE PORT B HEC THRESHOLD — 0x71 to 0x73 RBHECT2 to RBHECT0

TABLE 67. RBHECT2–RBHECT0

	7	6	5	4	3	2	1	0
RBHECT2 0x71	RBHECT2[7]	RBHECT2[6]	RBHECT2[5]	RBHECT2[4]	RBHECT2[3]	RBHECT2[2]	RBHECT2[1]	RBHECT2[0]
RBHECT1 0x72	RBHECT1[7]	RBHECT1[6]	RBHECT1[5]	RBHECT1[4]	RBHECT1[3]	RBHECT1[2]	RBHECT1[1]	RBHECT1[0]
RBHECT0 0x73	RBHECT0[7]	RBHECT0[6]	RBHECT0[5]	RBHECT0[4]	RBHECT0[3]	RBHECT0[2]	RBHECT0[1]	RBHECT0[0]

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Type: Read/Write

Software Lock: No

Reset Value: 0xFF

The RBHECT2, RBHECT1 and RBHECT0 registers contain the Port B received erred HEC threshold. When the error count RBHECC equals the threshold RBHECT, then the RBXHEC alarm will be set.

These registers should not be set to all zeroes.

- **RBHECT2–RBHECT0** Most significant byte RBHECT2 and least significant byte RBHECT0.

18.48 RECEIVE PORT B BIP COUNT — 0x74 to 0x76 RBBIPC2 to RBBIPC0

TABLE 68. RBBIPC2–RBBIPC0

	7	6	5	4	3	2	1	0
RBBIPC2 0x74	RBBIPC2[7]	RBBIPC2[6]	RBBIPC2[5]	RBBIPC2[4]	RBBIPC2[3]	RBBIPC2[2]	RBBIPC2[1]	RBBIPC2[0]
RBBIPC1 0x75	RBBIPC1[7]	RBBIPC1[6]	RBBIPC1[5]	RBBIPC1[4]	RBBIPC1[3]	RBBIPC1[2]	RBBIPC1[1]	RBBIPC1[0]
RBBIPC0 0x76	RBBIPC0[7]	RBBIPC0[6]	RBBIPC0[5]	RBBIPC0[4]	RBBIPC0[3]	RBBIPC0[2]	RBBIPC0[1]	RBBIPC0[0]

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The RBBIPC2, RBBIPC1 and RBBIPC0 registers contain the Port B received errored BIP count.

- **RBBIPC2–RBBIPC0** This register must be read in the order of most significant byte RBBIPC2first and least significant byte RBBIPC0 or the value read will not be valid. This counter will not roll-over from 0xFFFFFF to 0x000000 but will stick at 0xFFFFFF.

18.49 RECEIVE PORT B BIP THRESHOLD — 0x77 to 0x79 RBBIPT2 to RBBIPT0

TABLE 69. RBBIPT2–RBBIPT0

	7	6	5	4	3	2	1	0
RBBIPT2 0x77	RBBIPT2[7]	RBBIPT2[6]	RBBIPT2[5]	RBBIPT2[4]	RBBIPT2[3]	RBBIPT2[2]	RBBIPT2[1]	RBBIPT2[0]
RBBIPT1 0x78	RBBIPT1[7]	RBBIPT1[6]	RBBIPT1[5]	RBBIPT1[4]	RBBIPT1[3]	RBBIPT1[2]	RBBIPT1[1]	RBBIPT1[0]
RBBIPT0 0x79	RBBIPT0[7]	RBBIPT0[6]	RBBIPT0[5]	RBBIPT0[4]	RBBIPT0[3]	RBBIPT0[2]	RBBIPT0[1]	RBBIPT0[0]

Type: Read/Write

Software Lock: No

Reset Value: 0xFF

The RBBIPT2, RBBIPT1 and RBBIPT0 registers contain the Port B received erred BIP threshold. When the error count RBBIPC equals the threshold RBBIPT, then the RBXBIP alarm will be set.

These registers should not be set to all zeroes.

- **RBBIPT2–RBBIPT0** Most significant byte RBBIPT2 and least significant byte RBBIPT0.

18.50 RECEIVE PORT B PERFORMANCE ALARMS — 0x7A RBPA

TABLE 70. RBPA

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RBXHEC	RBXBIP

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

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18.0 Register Description (Continued)

The Receive Port B Performance Alarms register contains information about the error performance of Port B. When set RBXHEC and RBXBIP will raise an interrupt if the corresponding interrupt enable bits are set.

- **RBXHEC** Receive Port B, Excessive HEC Errors. Set = Number of HEC errors counted in RBHECC is equal to or greater than the threshold set in RBHECT. This bit is set when RBHECC = RBHECT and can only be cleared by a read of this register.
- **RBXBIP** Receive Port B, Excessive BIP Errors. Set = Number of BIP errors counted in RBBIPC is equal to or greater than the threshold set in RBBIPT. This bit is set when RBBIPC = RBBIPT and can only be cleared by a read of this register.

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18.51 RECEIVE PORT B PERFORMANCE INTERRUPT ENABLES — 0x7B RBPIE

TABLE 71. RBPIE

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RBXHECIE	RBXBIPIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the alarms in the RBPA register. Set = interrupt enabled and Clear = interrupt disabled.

18.52 RECEIVE PORT B REMOTE STATUS AND ALARMS — 0x7C RBRA

TABLE 72. RBRA

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RBRCS	RBRLOSA	RBRLOSB	RBRBA	RBRDSLL

Type: Bits[4:2] and [0] Read only/Clear on Read
Bit[1] Read only

Software Lock: No

Reset Value: 0x0D

The Receive Port B Remote Status and Alarms register contains information on the status of the far-end device, which is connected to Port B. On a local Loss of Signal on Port B, LLOSB alarm, these bits return to their reset values. When set, the RBRLOSA, RBRLOSB, RBRBA, and RBRDSLL bits will raise an interrupt if the corresponding interrupt enable is set. Also, a change in value on RBRLOSA, RBRLOSB, RBRDSLL or RBRBA will set the RBRCS bit. When set, the RBRCS bit will raise an interrupt if the corresponding interrupt enable is set.

- **RBRCS** Receive Port B, Remote Change of Status at far end device LVDS receive Ports.
- **RBRLOSA** Receive Port B, Remote Loss Of Signal at far end device LVDS receive Port A.
- **RBRLOSB** Receive Port B, Remote Loss Of Signal at far end device LVDS receive Port B.
- **RBRBA** Receive Port B, Remote far end device active receive Port. Set = Port B active and Clear = Port A active. Note that this bit, if set, will not clear on a read of this register.
- **RBRDSLL** Receive Port B, Remote far end device active receive port Descrambler Loss of Lock. Set = Out of Lock and Clear = Lock.

18.53 RECEIVE PORT B REMOTE INTERRUPT ENABLES — 0x7D RBRIE

TABLE 73. RBRIE

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RBRCSIE	RBRLOSAIE	RBRLOSBIE	RBRBAIE	RBRDSLLIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the alarms in the RBRB register. Set = interrupt enabled and Clear = interrupt disabled.

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18.0 Register Description (Continued)

18.54 RECEIVE PORT B UP2DOWN LOOPBACK CELL COUNT — 0x7E RBU2DLBC

TABLE 74. RBU2DLBC

7	6	5	4	3	2	1	0
RBU2DLBC[7]	RBU2DLBC[6]	RBU2DLBC[5]	RBU2DLBC[4]	RBU2DLBC[3]	RBU2DLBC[2]	RBU2DLBC[1]	RBU2DLBC[0]

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Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The Receive Port B Up2Down Loopback Cell Count register counts the number of incoming loopback cells detected from the Port B LVDS interface when Up2Down loopback is enabled with the U2DLB bit of the ALBC register, see *Section 18.18 ATM AND LVDS LOOPBACK CONTROL — 0x1A ALBC*. Note that this counter is incremented when an incoming loopback cell is received and that this differs from the functionality of the Down2Up Loopback Cell Count register, see *Section 18.71 ATM DOWN2UP LOOPBACK CELL COUNT — 0xE0 D2ULBCC*.

- **RBU2DLBC[7:0]** Port B Up2Down Loopback Cell Count value. This register will not roll-over from 0x00 to 0xFF but will stick at 0xFF.

18.55 RECEIVE PORT B CELL DELINEATION THRESHOLDS — 0x80 RBCDT

TABLE 75. RBCDT

7	6	5	4	3	2	1	0
ALPHA[3]	ALPHA[2]	ALPHA[1]	ALPHA[0]	DELTA[3]	DELTA[2]	DELTA[1]	DELTA[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x78

The Receive Port B Cell and Transport Container Delineation Thresholds register controls the operation of the Port B cell delineation state machine. The cell delineation lock status is reflected in the RBLTCLL bit of the RBLA register.

- **ALPHA[3:0]** When in lock this is the number of consecutive incorrect cell HEC's required to lose cell delineation lock.
- **DELTA[3:0]** When out of lock this is the number of consecutive correct cell HEC's required to gain cell delineation lock.

18.56 RECEIVE PORT B FRAME DELINEATION THRESHOLDS — 0x81 RBFDT

TABLE 76. RBFDT

7	6	5	4	3	2	1	0
MU[3]	MU[2]	MU[1]	MU[0]	SIGMA[3]	SIGMA[2]	SIGMA[1]	SIGMA[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x78

The Receive Port B Frame Delineation Thresholds register controls the operation of the Port B frame delineation state machine. The frame delineation lock status is reflected in the RBLFLL bit of the RBLA register.

- **MU[3:0]** When in lock this is the number of consecutive incorrect cell HEC's required to lose frame delineation lock.
- **SIGMA[3:0]** When out of lock this is the number of consecutive correct frame HEC's required to gain frame delineation lock.

18.57 RECEIVE PORT B DESCRAMBLER LOCK THRESHOLDS — 0x82 RBDSLKT

TABLE 77. RBDSLKT

7	6	5	4	3	2	1	0
PSI[3]	PSI[2]	PSI[1]	PSI[0]	RHO[3]	RHO[2]	RHO[1]	RHO[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x88

The Receive Port B Descrambler Lock Thresholds register controls the operation of the Port B descrambler lock state machine confidence counter. The descrambler lock status is reflected in the RBLDSLL bit of the RBLA register.

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18.0 Register Description (Continued)

- **PSI[3:0]** When in lock this is the threshold that the descrambler confidence counter must reach to lose descrambler lock. When in lock the descrambler confidence counter increments on incorrect HEC predictions and decrements on good HEC predictions.
- **RHO[3:0]** When out of lock this is the threshold that the descrambler confidence counter must reach to gain descrambler lock. When out of lock the descrambler confidence counter decrements on incorrect HEC predictions and increments on good HEC predictions.

18.58 RECEIVE PORT B BIT ERROR COUNT — 0x83 to 0x85 RBBEC2 to RBBEC0

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TABLE 78. RBBEC2–RBBEC0

	7	6	5	4	3	2	1	0
RBBEC2 0x83	RBBEC2[7]	RBBEC2[6]	RBBEC2[5]	RBBEC2[4]	RBBEC2[3]	RBBEC2[2]	RBBEC2[1]	RBBEC2[0]
RBBEC1 0x84	RBBEC1[7]	RBBEC1[6]	RBBEC1[5]	RBBEC1[4]	RBBEC1[3]	RBBEC1[2]	RBBEC1[1]	RBBEC1[0]
RBBEC0 0x85	RBBEC0[7]	RBBEC0[6]	RBBEC0[5]	RBBEC0[4]	RBBEC0[3]	RBBEC0[2]	RBBEC0[1]	RBBEC0[0]

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The RBBEC2, RBBEC1 and RBBEC0 registers contain the Port B received bit error count whenever the RBBEC bit of the RBCTL register is set. If the RBBEC bit of the RBCTL register is clear, these registers are cleared.

- **RBBEC2–RBBEC0** This register must be read in the order of most significant byte RBBEC2 first and least significant byte RBBEC0 last, or the value read will not be valid. This counter will not roll-over from 0xFFFFFF to 0x000000 but will stick at 0xFFFFFF.

18.59 UTOPIA CONFIGURATION — 0xA0 UCFG

TABLE 79. UCFG

7	6	5	4	3	2	1	0
Reserved	Reserved	CLVM[1]	CLVM[0]	BWIDTH	Reserved	UBDEN	UMODE

Type: Read/Write

Software Lock: Yes

Reset Value: 0x00

The UTOPIA Configuration register defines the UTOPIA interface operating modes. The default is ATM Layer Level 2 mode (31 ports) using CLAV0 with16 bit data.

- **CLVM[1:0]** Clav Mode bits. 00 = Up to 31 ports using CLAV0, 01 or 10 = Reserved, 11 = Up to 248 ports using CLAV0 to CLAV7.
- **BWIDTH** UTOPIA data bus width. Set = 8-bit data bus and Clear = 16-bit mode.
- **UBDEN** UTOPIA Bidirectional pins enable. Set = the UTOPIA bidirectional pins take on the functionality as defined by the UMODE setting. Clear = All UTOPIA interface bidirectional pins are tri-stated. This is to avoid pin contention at the UTOPIA pins on reset.
- **UMODE** UTOPIA ATM or PHY mode. Set = PHY Layer interface and Clear = ATM Layer Interface.

18.60 UTOPIA CONNECTED PORT LIST — 0xA1 to 0xA4 UCPL3 to UCPL0

TABLE 80. UCPL1–UCPL0

	7	6	5	4	3	2	1	0
UCPL3 0xA1	Reserved	UCPL3[6]	UCPL3[5]	UCPL3[4]	UCPL3[3]	UCPL3[2]	UCPL3[1]	UCPL3[0]
UCPL2 0xA2	UCPL2[7]	UCPL2[6]	UCPL2[5]	UCPL2[4]	UCPL2[3]	UCPL2[2]	UCPL2[1]	UCPL2[0]
UCPL1 0xA3	UCPL1[7]	UCPL1[6]	UCPL1[5]	UCPL1[4]	UCPL1[3]	UCPL1[2]	UCPL1[1]	UCPL1[0]
UCPL0 0xA4	UCPL0[7]	UCPL0[6]	UCPL0[5]	UCPL0[4]	UCPL0[3]	UCPL0[2]	UCPL0[1]	UCPL0[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0xFF, except UCPL3 = 0x7F

The UCPL3, UCPL2, UCPL1 and UCPL0 registers define the connected UTOPIA ports for polling. The sub-ports present for the connected ports is defined in the UCSPL register. Note that at least one port has to be connected for correct polling to occur, so these registers should never be set to all zeroes. See *Section 8.0 UTOPIA Interface Operation*. If no ports are required then use of the Configuration Traffic inhibit functionality is recommended. See *Section 10.0 Configuration and Traffic Inhibit Operation*.

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18.0 Register Description (Continued)

- **UCPL3–UCPL0** UCPL3[6] corresponds to port 31 and UCPL0[0] corresponds to port 0. When a bit is set then the port is connected and will be polled, when clear the port is not connected and will not be polled.

18.61 UTOPIA CONNECTED SUB-PORT LIST—0xA6 UCSPL

TABLE 81. UCSPL

7	6	5	4	3	2	1	0
UCSPL[7]	UCSPL[6]	UCSPL[5]	UCSPL[4]	UCSPL[3]	UCSPL[2]	UCSPL[1]	UCSPL[0]

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Type: Read/Write

Software Lock: Yes

Reset Value: 0x01

The UCSPL register defines the connected UTOPIA sub-ports within all ports for polling.

- **UCSPL** UCSPL[7] corresponds to sub-port 7 (CLAV7) and UCSPL[0] corresponds to sub-port 0 (CLAV0). When a bit is set, then the sub-port is connected and will be polled; when clear, the sub-port is not connected and will not be polled.

18.62 UTOPIA SUB-PORT ADDRESS LOCATION—0xA7 USPAL

TABLE 82. USPAL

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	USPL[4]	USPL[3]	USPL[2]	USPL[1]	USPL[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x00

The UTOPIA Sub-Port Address Location register defines which byte of the PDU header the sub-port address is contained in when using Extended UTOPIA mode. The PDU header consists of the User Prepend, the ATM cell header and UDF bytes, and so can be a maximum of 18 bytes. The first of these bytes is denoted as byte 0. The corresponding USPAM register is used to define which bits in the byte contain the sub-port address.

- **USPAL[4:0]** Byte number of the PDU header byte which contains the UTOPIA sub-port address.

18.63 UTOPIA SUB-PORT ADDRESS MASK—0xA8 USPAM

TABLE 83. USPAM

7	6	5	4	3	2	1	0
USPAM[7]	USPAM[6]	USPAM[5]	USPAM[4]	USPAM[3]	USPAM[2]	USPAM[1]	USPAM[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x07

The UTOPIA Sub-Port Address Mask register defines which bits of the PDU header byte defined by the USPAL register contain the sub-port address.

- **USPAM[7:0]** Set = This bit location contains valid sub-port address bit.Clear = Ignore this bit location.

Note that only 3 bit locations must be set in this register to give the 3 bit sub-port address location. All other bits must be clear. By default, bits USPAM[2:0] are set, indicating that the sub-port address is located in bits [2:0] of the PDU header byte indicated by the USPAL register, with the MSB in bit [2] and the LSB in bit [0]. If USPAM bits [6], [4] and [1] were set, then the sub-port address would be located in bits [6], [4] and [1] of the PDU header byte indicated by the USPAL register, with the MSB in bit [6] and the LSB in bit [1].

18.64 MTB QUEUE THRESHOLD—0xA9 to 0xC7 MTBQT30 to MTBQT0

TABLE 84. MTBQT30–MTBQT0

	7	6	5	4	3	2	1	0
MTBQT30 0xA9	MTBQT30[7]	MTBQT30[6]	MTBQT30[5]	MTBQT30[4]	MTBQT30[3]	MTBQT30[2]	MTBQT30[1]	MTBQT30[0]
MTBQT29 0xAA	MTBQT29[7]	MTBQT29[6]	MTBQT29[5]	MTBQT29[4]	MTBQT29[3]	MTBQT29[2]	MTBQT29[1]	MTBQT29[0]
MTBQT2 0xC5	MTBQT2[7]	MTBQT2[6]	MTBQT2[5]	MTBQT2[4]	MTBQT2[3]	MTBQT2[2]	MTBQT2[1]	MTBQT2[0]

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18.0 Register Description (Continued)

TABLE 84. MTBQT30–MTBQT0 (Continued)

	7	6	5	4	3	2	1	0
MTBQT1 0xC6	MTBQT1[7]	MTBQT1[6]	MTBQT1[5]	MTBQT1[4]	MTBQT1[3]	MTBQT1[2]	MTBQT1[1]	MTBQT1[0]
MTBQT0 0xC7	MTBQT0[7]	MTBQT0[6]	MTBQT0[5]	MTBQT0[4]	MTBQT0[3]	MTBQT0[2]	MTBQT0[1]	MTBQT0[0]

Type: Read/Write

Software Lock: Yes

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Reset Value: 0x04

The MTB Queue Threshold registers define the maximum size, in PDU cells, of each of the 31 queues. If all 31 queues are being used, it is recommended that the threshold be left at the default of 4 cells. If less than 31 queues are in use, then the queue threshold may be raised according to *Section 9.1 SINGLE BRIDGE MTB CONFIGURATION*.

- **MTBQT30[7:0]** Maximum number of PDU cells for queue 30.
- **MTBQT29[7:0]** Maximum number of PDU cells for queue 29.
- **.....**
- **MTBQT1[7:0]** Maximum number of PDU cells for queue 1.
- **MTBQT0[7:0]** Maximum number of PDU cells for queue 0.

18.65 MTB QUEUE FULL — 0xC8 to 0xCB MTBQFL3 to MTBQFL0

TABLE 85. MTBQFL3–MTBQFL0

	7	6	5	4	3	2	1	0
MTBQFL3 0xC8	MTBQFL3[7]	MTBQFL3[6]	MTBQFL3[5]	MTBQFL3[4]	MTBQFL3[3]	MTBQFL3[2]	MTBQFL3[1]	MTBQFL3[0]
MTBQT29 0xC9	MTBQFL2[7]	MTBQFL2[6]	MTBQFL2[5]	MTBQFL2[4]	MTBQFL2[3]	MTBQFL2[2]	MTBQFL2[1]	MTBQFL2[0]
MTBQFL1 0xCA	MTBQFL1[7]	MTBQFL1[6]	MTBQFL1[5]	MTBQFL1[4]	MTBQFL1[3]	MTBQFL1[2]	MTBQFL1[1]	MTBQFL1[0]
MTBQFL0 0xCB	MTBQFL0[7]	MTBQFL0[6]	MTBQFL0[5]	MTBQFL0[4]	MTBQFL0[3]	MTBQFL0[2]	MTBQFL0[1]	MTBQFL0[0]

Type: Read only

Software Lock: No

Reset Value: 0x00

The MTBQFL3, MTBQFL2, MTBQFL1 and MTBQFL0 registers show which queues are full.

- **MTBQFL3[7]** MTBQFL3[7] bit indicates that the entire MTB is full. As memory resources are over assigned among the 31 individual queues then the MTB may be full while some of the individual queues may not be full. When this bit is set, then the entire queue is full and when clear, the queue is not full.
- **MTBQFL3–MTBQFL0** MTBQFL3[6] corresponds to queue 31 and MTBQFL0[0] corresponds to queue 0. When a bit is set, then the queue is full and when clear, the queue is not full.

18.66 MTB QUEUE EMPTY — 0xCC to 0xCF MTBQE3 to MTBQE0

TABLE 86. MTBQE3–MTBQE0

	7	6	5	4	3	2	1	0
MTBQE3 0xCC	Reserved	MTBQE3[6]	MTBQE3[5]	MTBQE3[4]	MTBQE3[3]	MTBQE3[2]	MTBQE3[1]	MTBQE3[0]
MTBQT29 0xCD	MTBQE2[7]	MTBQE2[6]	MTBQE2[5]	MTBQE2[4]	MTBQE2[3]	MTBQE2[2]	MTBQE2[1]	MTBQE2[0]
MTBQE1 0xCE	MTBQE1[7]	MTBQE1[6]	MTBQE1[5]	MTBQE1[4]	MTBQE1[3]	MTBQE1[2]	MTBQE1[1]	MTBQE1[0]
MTBQE0 0xCF	MTBQE0[7]	MTBQE0[6]	MTBQE0[5]	MTBQE0[4]	MTBQE0[3]	MTBQE0[2]	MTBQE0[1]	MTBQE0[0]

Type: Read only

Software Lock: No

Reset Value: 0xFF, except MTBQE3 = 0x7F

The MTBQE3, MTBQE2, MTBQE1 and MTBQE0 registers show which queues are empty.

- **MTBQE3–MTBQE0** MTBQE3[6] corresponds to queue 31 and MTBQE0[0] corresponds to queue 0. When a bit is set, then the queue is empty and when clear, the queue is not empty.

18.67 MTB QUEUE FLUSH — 0xD0 to 0xD3 MTBQF3 to MTBQF0

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18.0 Register Description (Continued)

TABLE 87. MTBQF3–MTBQF0

	7	6	5	4	3	2	1	0
MTBQF3 0xD0	Reserved	MTBQF3[6]	MTBQF3[5]	MTBQF3[4]	MTBQF3[3]	MTBQF3[2]	MTBQF3[1]	MTBQF3[0]
MTBQF2 0xD1	MTBQF2[7]	MTBQF2[6]	MTBQF2[5]	MTBQF2[4]	MTBQF2[3]	MTBQF2[2]	MTBQF2[1]	MTBQF2[0]
MTBQF1 0xD2	MTBQF1[7]	MTBQF1[6]	MTBQF1[5]	MTBQF1[4]	MTBQF1[3]	MTBQF1[2]	MTBQF1[1]	MTBQF1[0]
MTBQF0 0xD3	MTBQF0[7]	MTBQF0[6]	MTBQF0[5]	MTBQF0[4]	MTBQF0[3]	MTBQF0[2]	MTBQF0[1]	MTBQF0[0]

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Type: Read/Write

Software Lock: Yes

Reset Value: 0x00

The MTBQF3, MTBQF2, MTBQF1 and MTBQF0 registers allow each of the queues to be flushed. Flushing a queue removes all PDU cells from the queue. The processor sets the appropriate bit in the MTBQF register to flush a queue. When this has been completed, the hardware will clear the bit. So after setting a bit to flush a queue, the processor should poll the MTBQF register to determine when the flushing has been completed.

- **MTBQF3–MTBQF0** MTBQF3[6] corresponds to queue 31 and MTBQF0[0] corresponds to queue 0. When a bit is set, then a flush of the corresponding queue is initiated and when the queue flush is completed and the queue is now in normal operation.

18.68 MTB CELL FLUSH—0xD4 to 0xD7 MTBCF3 to MTBCF0

TABLE 88. MTBCF3–MTBCF0

	7	6	5	4	3	2	1	0
MTBCF3 0xD4	Reserved	MTBCF3[6]	MTBCF3[5]	MTBCF3[4]	MTBCF3[3]	MTBCF3[2]	MTBCF3[1]	MTBCF3[0]
MTBCF2 0xD5	MTBCF2[7]	MTBCF2[6]	MTBCF2[5]	MTBCF2[4]	MTBCF2[3]	MTBCF2[2]	MTBCF2[1]	MTBCF2[0]
MTBCF1 0xD6	MTBCF1[7]	MTBCF1[6]	MTBCF1[5]	MTBCF1[4]	MTBCF1[3]	MTBCF1[2]	MTBCF1[1]	MTBCF1[0]
MTBCF0 0xD7	MTBCF0[7]	MTBCF0[6]	MTBCF0[5]	MTBCF0[4]	MTBCF0[3]	MTBCF0[2]	MTBCF0[1]	MTBCF0[0]

Type: Read/Write

Software Lock: Yes

Reset Value: 0x00

The MTBCF3, MTBCF2, MTBCF1 and MTBCF0 registers allow the PDU cell at the head of each of the queues to be flushed. This removes the PDU cell from the head of the queue without corrupting the queue. The processor sets the appropriate bit in the MTBCF register to flush a cell from a queue. When this has been completed, the hardware will clear the bit. So after setting a bit to flush a cell from a queue, the processor should poll the MTBCF register to determine when the flush has been completed.

- **MTBCF3–MTBCF0** MTBCF3[6] corresponds to queue 31 and MTBCF0[0] corresponds to queue 0. When a bit is set, then a flush of the PDU cell at the head of the queue is initiated and when clear, the cell flush is completed and the queue is now in normal operation.

18.69 QUEUE FLUSH—0xD8 QFL

TABLE 89. QFL

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FIBFL	MTBFL

Type: Read/Write

Software Lock: Yes

Reset Value: 0x00

The Queue Flush register allows both the MTB and the FIB queues to be completely flushed. This removes all PDU cells from either the MTB or FIB queue. The processor sets the appropriate bit in the QFL register to flush a queue. When this has been completed, the hardware will clear the bit. So after setting a bit to flush a queue the processor should poll the QFL register to determine when the flush has been completed.

- **FIBFL** When set, then a flush of the FIB queue is initiated and when clear, the FIB queue flush is completed and the queue is now in normal operation.
- **MTBFL** When set, then a flush of the MTB queue is initiated and when clear, the MTB queue flush is completed and the queue is now in normal operation.

18.70 MTB QUEUE OVERFLOW—0xD9 to 0xDC MTBQOV3 to MTBQOV0

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18.0 Register Description (Continued)

TABLE 90. MTBQOV3–MTBQOV0

	7	6	5	4	3	2	1	0
MTBQOV3 0xD9	Reserved	MTBQOV3[6]	MTBQOV3[5]	MTBQOV3[4]	MTBQOV3[3]	MTBQOV3[2]	MTBQOV3[1]	MTBQOV3[0]
MTBQT29 0xDA	MTBQOV2[7]	MTBQOV2[6]	MTBQOV2[5]	MTBQOV2[4]	MTBQOV2[3]	MTBQOV2[2]	MTBQOV2[1]	MTBQOV2[0]
MTBQOV1 0xDB	MTBQOV1[7]	MTBQOV1[6]	MTBQOV1[5]	MTBQOV1[4]	MTBQOV1[3]	MTBQOV1[2]	MTBQOV1[1]	MTBQOV1[0]
MTBQOV0 0xDC	MTBQOV0[7]	MTBQOV0[6]	MTBQOV0[5]	MTBQOV0[4]	MTBQOV0[3]	MTBQOV0[2]	MTBQOV0[1]	MTBQOV0[0]

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Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The MTBQOV3, MTBQOV2, MTBQOV1 and MTBQOV0 registers indicate the overflow status of the thirty-one queues in the MTB. If a queue has filled to its threshold defined in the MTBQT31–MTBQT0 registers, and an attempt is made to write another cell to the queue, then the overflow bit for that queue will be set in these registers. These bits reflect that an attempt has been made to write to an already full queue and may be used as an indication of problems with the Flow Control mechanism. Up to seven additional cells will be accepted into the queue before a hard overflow occurs. Once the threshold value plus seven cells has been exceeded any additional cells will be rejected and discarded automatically. A subsequent read of a cell from the specific queue out over the Utopia interface will be successful, and will clear the overflow bit in this register once the number of cells in the queue is below the threshold. If any bit in the MTBQOV3–MTBQOV0 registers is set then the MTBSOVA bit of the UAA register will be set and may raise an interrupt.

- **MTBQOV3–MTBQOV0** MTBQOV3[6] corresponds to queue 31 and MTBQOV0[0] corresponds to queue 0. When a bit is set, then there was an attempt to overflow the corresponding queue.

18.71 ATM DOWN2UP LOOPBACK CELL COUNT — 0xE0 D2ULBCC

TABLE 91. D2ULBCC

7	6	5	4	3	2	1	0
D2ULBCC[7]	D2ULBCC[6]	D2ULBCC[5]	D2ULBCC[4]	D2ULBCC[3]	D2ULBCC[2]	D2ULBCC[1]	D2ULBCC[0]

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The ATM Down2Up Loopback Cell Count register counts the number of outgoing loopback cells detected on the UTOPIA interface when Down2Up loopback is enabled with the D2ULB bit of the ALBC register, see *Section 18.18 ATM AND LVDS LOOPBACK CONTROL — 0x1A ALBC*. Note that this counter is only incremented when a loopback cell is read out of the device.

- **D2ULBCC[7:0]** Down2Up Loopback Cell Count value. This register will not roll-over from 0x00 to 0xFF but will stick at 0xFF.

18.72 UTOPIA AND ATM ALARMS — 0xE1 UAA

TABLE 92. UAA

7	6	5	4	3	2	1	0
PDULA	CTFRA	D2ULBC	U2DLBC	UPRTY	FIBOVA	MTBSOVA	MTBHOVA

Type: Read only/Clear on Read

Software Lock: No

Reset Value: 0x00

The UTOPIA and ATM Alarms register monitors the UTOPIA interface, loopbacks and queue overflows. When set these bits will raise an interrupt if the corresponding interrupt enables are set.

- **PDULA** PDU Length Alarm bit. Set = PDU length as defined by the PDUCFG register is greater than the maximum PDU cell length of 64 bytes. Clear = PDU length is less than or equal to maximum of 64 bytes.
- **CTFRA** Cell Transfer Alarm bit. This alarm is only valid when the device is configured as a PHY layer by setting the UMODE bit of the UCFG register. It indicates that the controlling ATM layer device has caused an incorrect cell transfer to or from the DS92UT16. An incorrect cell transfer can only occur when a suspended cell transfer is restarted with an different MPhy address than initially selected. Set = Incorrect cell transfer has occurred on the UTOPIA transmit or receive interface.
- **D2ULBC** Set = D2ULBCC count register has changed value.
- **U2DLBC** Set = RAU2DLBC or RBU2DLBC count registers have changed value.
- **UPRTY** Set = A parity error has occurred on an incoming ATM cell byte.

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18.0 Register Description (Continued)

- **FIBOV** Set = FIB queue attempted to overflow (Equivalent functionality as the MTBQOV3–0 register bits).
- **MTBSOV** MTB Soft Overflow Alarm bit. Set = One or more of the bits in the MTBQOV3–MTBQOV0 registers are set. Clear = The MTBQOV3–MTBQOV0 registers are clear.
- **MTBHOV** MTB Hard Overflow Alarm bit. Set = MTB queue has attempted to overflow. This is a hard overflow as the overall MTB has attempted to fill beyond it's hard limit of 159 cells.

18.73 UTOPIA AND ATM INTERRUPT ENABLES — 0xE2 UAIE

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TABLE 93. UAIE

7	6	5	4	3	2	1	0
PDULIE	CTFRIE	D2ULBCIE	U2DLBCIE	UPRTYIE	FIBOVIE	MTBSOVAIE	MTBHOVIE

Type: Read/Write

Software Lock: No

Reset Value: 0x00

This register contains the interrupt enables for the alarms in the UAA register. Set = interrupt enabled and Clear = interrupt disabled.

18.74 ATM LOOPBACK CELL FILTER — 0xF7 to 0xFA ALFLT3 to AFLT0

TABLE 94. ALFLT3–ALFLT0

	7	6	5	4	3	2	1	0
ALFLT3 0xF7	ALFLT3[7]	ALFLT3[6]	ALFLT3[5]	ALFLT3[4]	ALFLT3[3]	ALFLT3[2]	ALFLT3[1]	ALFLT3[0]
ALFLT2 0xF8	ALFLT2[7]	ALFLT2[6]	ALFLT2[5]	ALFLT2[4]	ALFLT2[3]	ALFLT2[2]	ALFLT2[1]	ALFLT2[0]
ALFLT1 0xF9	ALFLT1[7]	ALFLT1[6]	ALFLT1[5]	ALFLT1[4]	ALFLT1[3]	ALFLT1[2]	ALFLT1[1]	ALFLT1[0]
ALFLT0 0xFA	ALFLT0[7]	ALFLT0[6]	ALFLT0[5]	ALFLT0[4]	ALFLT0[3]	ALFLT0[2]	ALFLT0[1]	ALFLT0[0]

Type: Read/Write

Software Lock: No

Reset Value: 0xFF

The ALBCF3, ALBCF2, ALBCF1 and ALBCF0 registers (See Section 7.20) define the cell header bytes filter for detecting ATM loopback cells. Incoming ATM cells are compared against the loopback cell header format defined in the ALBCF3–ALBCF0 registers to determine if they are loopback cells. The filter defined in the ALFLT3–ALFLT0 registers is used to determine which bits of the four byte cell header are compared. If a bit is set then that bit in the incoming cell header is compared against the corresponding bit in the ALBCF3–ALBCF0 registers. Only those bits which are set in the ALFLT3–ALFLT0 registers are compared to determine if a cell is a loopback cell.

- **ALBCF3[7:0]** Loopback Cell header byte H1 filter.
- **ALBCF2[7:0]** Loopback Cell header byte H2 filter.
- **ALBCF1[7:0]** Loopback Cell header byte H3 filter.
- **ALBCF0[7:0]** Loopback Cell header byte H4 filter.

19.0 Test Features

19.1 TEST STRUCTURES

The DS92UT16 device has the following test structures in place.

- Internal SCAN (manufacturing test only)
- RAM BIST (manufacturing test only)
- Boundary SCAN

As shown, the device has a AP controller which was generated using the LOGICVISION tool suite. This AP controller is used to configure the device for scan testing, RAM BIST and Boundary Scan. The Instruction Register is shown in *Figure 23*. Bits 12–18 are not used. A more detailed description of the operation of the TAP controller can be found in the LOGICVISION document: Adding Logic Test — A Hardware Reference July 2000. (**NOTE:** The Internal SCAN and RAM BIST functions are not user accessible. Therefore, the device user should never assert the Test_se pin.)

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19.0 Test Features (Continued)

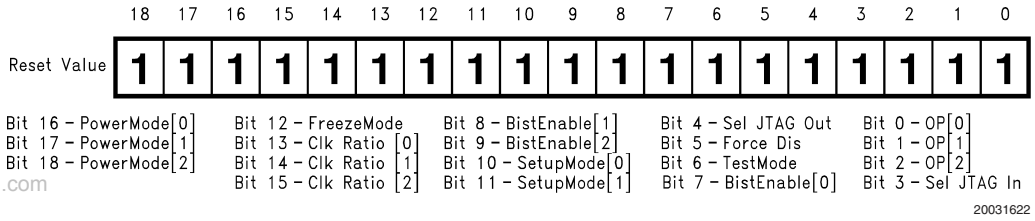

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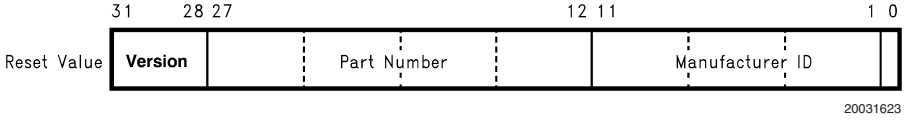
FIGURE 23. LOGICVISION TAP Instruction Register

The TAP controller contains a device ID register which holds the device identification. *Figure 24* shows the makeup of the device ID register and the device ID value for the DS92UT16 device.



DEVICE ID = 0FC2801F

FIGURE 24. Device Identification Register

19.2 BOUNDARY SCAN

The DS92UT16 device contains boundary scan (BS) cells on all inputs, outputs, bi-directs, and direction control signals. There are no boundary scan cells on any of the inputs or outputs from the pins to the LVDS Interface block. The boundary scan order is shown in *Table 95* along with the type and controlling BS cell for bidirectional BS cells.For bidirectional pins, if the controlling cell is a logic '1' then they are outputs.

TABLE 95.

No.	Pin Name	Type	Ctrl.
1	RBPWDN	INPUT	N/A
2	TXADEN	INPUT	N/A
3	TXBDEN	INPUT	N/A
4	TPWDN	INPUT	N/A
5	TXSYNC	INPUT	N/A
6	TXCLK	INPUT	N/A
7	CPU_BUSMODE	INPUT	N/A
8	CPU_CS_N	INPUT	N/A
9	CPU_RD_N	INPUT	N/A
10	CPU_WR_N	INPUT	N/A
11	CPU_INT_N	OUTPUT	N/A
12	CPU_DATA_TRI	ENABLE	N/A
13	CPU_DATA_7	BIDIR	12
14	CPU_DATA_6	BIDIR	12
15	CPU_DATA_5	BIDIR	12
16	CPU_DATA_4	BIDIR	12
17	CPU_DATA_3	BIDIR	12
18	CPU_DATA_2	BIDIR	12
19	CPU_DATA_1	BIDIR	12
20	CPU_DATA_0	BIDIR	12
21	CPU_ADDR_7	INPUT	N/A
22	CPU_ADDR_6	INPUT	N/A
23	CPU_ADDR_5	INPUT	N/A
24	CPU_ADDR_4	INPUT	N/A
25	CPU_ADDR_3	INPUT	N/A
26	CPU_ADDR_2	INPUT	N/A
27	CPU_ADDR_1	INPUT	N/A
28	CPU_ADDR_0	INPUT	N/A
29	GPIO_TRI_3	ENABLE	N/A
30	GPIO_3	BIDIR	29
31	GPIO_TRI_2	ENABLE	N/A
32	GPIO_2	BIDIR	31
33	GPIO_TRI_1	ENABLE	N/A
34	GPIO_1	BIDIR	33
35	GPIO_TRI_0	ENABLE	N/A
36	GPIO_0	BIDIR	35
37	RESET_N	INPUT	N/A
38	UTFC_MODE	ENABLE	N/A
39	U_TXDATA_15	BIDIR	38
40	U_TXDATA_14	BIDIR	38
41	U_TXDATA_13	BIDIR	38
42	U_TXDATA_12	BIDIR	38
43	U_TXDATA_11	BIDIR	38
44	U_TXDATA_10	BIDIR	38
45	U_TXDATA_9	BIDIR	38

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19.0 Test Features (Continued)

TABLE 95. (Continued)

No.	Pin Name	Type	Ctrl.
46	U_TXDATA_8	BIDIR	38
47	U_TXDATA_7	BIDIR	38
48	U_TXDATA_6	BIDIR	38
49	U_TXDATA_5	BIDIR	38
50	U_TXDATA_4	BIDIR	38
51	U_TXDATA_3	BIDIR	38
52	U_TXDATA_2	BIDIR	38
53	U_TXDATA_1	BIDIR	38
54	U_TXDATA_0	BIDIR	38
55	U_TXPARITY	BIDIR	38
56	U_TXCLAV_6	INPUT	N/A
57	U_TXCLAV_5	INPUT	N/A
58	U_TXCLAV_4	INPUT	N/A
59	U_TXCLAV_3	INPUT	N/A
60	U_TXCLAV_2	INPUT	N/A
61	U_TXCLAV_1	INPUT	N/A
62	U_TXCLAV_0	INPUT	N/A
63	U_TXCLAV_L_TRI	ENABLE	N/A
64	U_TXCLAV_L	BIDIR	63
65	U_TXENB_6	OUTPUT	N/A
66	U_TXENB_5	OUTPUT	N/A
67	U_TXENB_4	OUTPUT	N/A
68	U_TXENB_3	OUTPUT	N/A
69	U_TXENB_2	OUTPUT	N/A
70	U_TXENB_1	OUTPUT	N/A
71	U_TXENB_0	OUTPUT	N/A
72	UDB_CLK	INPUT	N/A
73	U_TXENB_L	BIDIR	38
74	U_TXSOC	BIDIR	38
75	U_TXADDR_4	BIDIR	38
76	U_TXADDR_3	BIDIR	38
77	U_TXADDR_2	BIDIR	38
78	U_TXADDR_1	BIDIR	38
79	U_TXADDR_0	BIDIR	38
80	U_RXDATA_TRI	ENABLE	N/A
81	U_RXDATA_15	BIDIR	80
82	U_RXDATA_14	BIDIR	80
83	U_RXDATA_13	BIDIR	80
84	U_RXDATA_12	BIDIR	80
85	U_RXDATA_11	BIDIR	80
86	U_RXDATA_10	BIDIR	80
87	U_RXDATA_9	BIDIR	80
88	U_RXDATA_8	BIDIR	80
89	U_RXDATA_7	BIDIR	80
90	U_RXDATA_6	BIDIR	80
91	U_RXDATA_5	BIDIR	80
92	U_RXDATA_4	BIDIR	80
93	U_RXDATA_3	BIDIR	80
94	U_RXDATA_2	BIDIR	80
95	U_RXDATA_1	BIDIR	80
96	U_RXDATA_0	BIDIR	80
97	U_RXOSC	BIDIR	80
98	U_RXENB_U_6	OUTPUT	N/A
99	U_RXENB_U_5	OUTPUT	N/A
100	U_RXENB_U_4	OUTPUT	N/A
101	UUB_CLK	INPUT	N/A
102	U_RXENB_U_3	OUTPUT	N/A
103	U_RXENB_U_2	OUTPUT	N/A
104	U_RXENB_U_1	OUTPUT	N/A
105	U_RXENB_U_0	OUTPUT	N/A
106	U_RXENB_L	BIDIR	38
107	U_RXCLAV_U_6	INPUT	N/A
108	U_RXCLAV_U_5	INPUT	N/A
109	U_RXCLAV_U_4	INPUT	N/A
110	U_RXCLAV_U_3	INPUT	N/A
111	U_RXCLAV_U_2	INPUT	N/A
112	U_RXCLAV_U_1	INPUT	N/A
113	U_RXCLAV_U_0	INPUT	N/A
114	U_RXCLAV_L_TRI	ENABLE	N/A
115	U_RXCLAV_L	BIDIR	114
116	U_RXPARITY	BIDIR	80
117	U_RXADDR_4	BIDIR	38
118	U_RXADDR_3	BIDIR	38
119	U_RXADDR_2	BIDIR	38
120	U_RXADDR_1	BIDIR	38
121	U_RXADDR_0	BIDIR	38
122	TEST_SE	INPUT	N/A
123	RAPWDN	INPUT	N/A

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20.0 Package

196-ball LBGA. Dimensions 15 x 15 x 1.37 mm, 1.0 mm ball pitch.

TABLE 96. Pin Locations—BGA196 Package

Ball	Pin Name	Signal Type	Description
A2	AGND	GND	Analog GND for LVDS I/O
A12	AGND	GND	Analog GND for LVDS I/O
B11	AGND	GND	Analog GND for LVDS I/O
B13	AGND	GND	Analog GND for LVDS I/O
C4	AGND	GND	Analog GND for LVDS I/O
C7	AGND	GND	Analog GND for LVDS I/O
C13	AGND	GND	Analog GND for LVDS I/O
E7	AGND	GND	Analog GND for LVDS I/O
B3	AV_{DD}	3.3V	Analog V_{DD} for LVDS I/O
B4	AV_{DD}	3.3V	Analog V_{DD} for LVDS I/O
B12	AV_{DD}	3.3V	Analog V_{DD} for LVDS I/O
B14	AV_{DD}	3.3V	Analog V_{DD} for LVDS I/O
C10	AV_{DD}	3.3V	Analog V_{DD} for LVDS I/O
D7	AV_{DD}	3.3V	Analog V_{DD} for LVDS I/O
J2	CPU_Addr[0]	Input LVTTL	Address Bus
J3	CPU_Addr[1]	Input LVTTL	Address Bus
J1	CPU_Addr[2]	Input LVTTL	Address Bus
H2	CPU_Addr[3]	Input LVTTL	Address Bus
H1	CPU_Addr[4]	Input LVTTL	Address Bus
G1	CPU_Addr[5]	Input LVTTL	Address Bus
F1	CPU_Addr[6]	Input LVTTL	Address Bus
E1	CPU_Addr[7]	Input LVTTL	Address Bus
E6	CPU_BusMode	Input LVTTL	Mode Select for CPU Bus Protocol
E5	CPU_cs	Input LVTTL	Select Signal to Validate the Address Bus for R/W Transfers
J4	CPU_Data[0]	BiDir LVTTL	Data Bus
H3	CPU_Data[1]	BiDir LVTTL	Data Bus
F2	CPU_Data[2]	BiDir LVTTL	Data Bus
H4	CPU_Data[3]	BiDir LVTTL	Data Bus
F3	CPU_Data[4]	BiDir LVTTL	Data Bus
G3	CPU_Data[5]	BiDir LVTTL	Data Bus
G4	CPU_Data[6]	BiDir LVTTL	Data Bus
E2	CPU_Data[7]	BiDir LVTTL	Data Bus
F4	CPU_int	Output LVTTL	Interrupt Request Line
E3	CPU_rd (CPU_ds)	Input LVTTL	Read or Data Strobe, Depending on CPU_BusMode
F5	CPU_wr (CPU_rnw)	Input LVTTL	Write or Read/Write, Depending on CPU_BusMode
B7	DGND	GND	Digital GND
C2	DGND	GND	Digital GND
D11	DGND	GND	Digital GND
E11	DGND	GND	Digital GND
F6	DGND	GND	Digital GND
F9	DGND	GND	Digital GND
G5	DGND	GND	Digital GND
H7	DGND	GND	Digital GND
H8	DGND	GND	Digital GND
H9	DGND	GND	Digital GND
K14	DGND	GND	Digital GND
L1	DGND	GND	Digital GND

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20.0 Package (Continued)

TABLE 96. Pin Locations — BGA196 Package (Continued)

Ball	Pin Name	Signal Type	Description
N8	DGND	GND	Digital GND
K1	$DV_{DD}25$	2.5V	V_{DD} for Core Logic
K13	$DV_{DD}25$	2.5V	V_{DD} for Core Logic
P10	$DV_{DD}25$	2.5V	V_{DD} for Core Logic
A1	$DV_{DD}33$	3.3V	Digital V_{DD}
A11	$DV_{DD}33$	3.3V	Digital V_{DD}
D10	$DV_{DD}33$	3.3V	Digital V_{DD}
F7	$DV_{DD}33$	3.3V	Digital V_{DD}
F8	$DV_{DD}33$	3.3V	Digital V_{DD}
G2	$DV_{DD}33$	3.3V	Digital V_{DD}
G6	$DV_{DD}33$	3.3V	Digital V_{DD}
G7	$DV_{DD}33$	3.3V	Digital V_{DD}
G14	$DV_{DD}33$	3.3V	Digital V_{DD}
J7	$DV_{DD}33$	3.3V	Digital V_{DD}
J11	$DV_{DD}33$	3.3V	Digital V_{DD}
H6	GPIO [0]	BiDir LVTTL	General Purpose Input and Output
H5	GPIO [1]	BiDir LVTTL	General Purpose Input and Output
K2	GPIO [2]	BiDir LVTTL	General Purpose Input and Output
J6	GPIO [3]	BiDir LVTTL	General Purpose Input and Output
E9	JTAG_CLK	Input LVTTL	Boundary Scan Test Clock
E8	JTAG_Reset	Input LVTTL	Boundary Scan Test Circuit Reset
F12	JTAG_TDI	Input LVTTL	Boundary Scan Test Data In
E13	JTAG_TDO	Output LVTTL	Boundary Scan Test Data Out
E10	JTAG_TMS	Input LVTTL	Boundary Scan Test Mode Select
C1	LVDS_ADen	Input LVTTL	Driver Enable for Transmit A
A14	LVDS_ADin[–]	Diff. Input	Input for Receiver Port A
A13	LVDS_ADin[+]	Diff. Input	Input for Receiver Port A
A9	LVDS_ADout[–]	Diff. Output	Output for Driver A
A10	LVDS_ADout[+]	Diff. Output	Output for Driver A
C14	LVDS_ALock_n	Output LVTTL	Lock Signal from Receive Port A
E14	LVDS_APwdn	Input LVTTL	Receive Port A and Deserializer Power Down
B10	LVDS_ARefClk	Input LVTTL	Reference Clock for Receiver A PLL
D14	LVDS_ARxClk	Output LVTTL	Recovered Clock Output from Receive Port A
D2	LVDS_BDen	Input LVTTL	Driver Enable for Transmit B
A3	LVDS_BDin[–]	Diff. Input	Input for Receive Port B
A4	LVDS_BDin[+]	Diff. Input	Input for Receive Port B
A6	LVDS_BDout[–]	Diff. Output	Output for Driver B
A7	LVDS_BDout[+]	Diff. Output	Output for Driver B
C3	LVDS_BLock_n	Output LVTTL	Lock Signal from Receive Port B
B1	LVDS_BPwdn	Input LVTTL	Receive Port B and Deserializer Power Down
D4	LVDS_BRefClk	Input LVTTL	Reference Clock for Receiver B PLL
B2	LVDS_BRxClk	Output LVTTL	Recovered Clock Output from Receive Port B
E4	LVDS_Synch	Input LVTTL	Force SYNC patterns on Transmit A and B
D1	LVDS_TxClk	Input LVTTL	Reference Clock for Driving Transmission Function
D3	LVDS_TxPwdn	Input LVTTL	Powerdown for LVDS Serializer
G8	NC		NO CONNECT
J8	NC		NO CONNECT
K8	NC		NO CONNECT

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20.0 Package (Continued)

TABLE 96. Pin Locations — BGA196 Package (Continued)

Ball	Pin Name	Signal Type	Description
B8	PGND	GND	GND for Transmit PLL
C8	PGND	GND	GND for Transmit PLL
D8	PGND	GND	GND for Transmit PLL
C9	PGNDA	GND	GND for PLL A
C11	PGNDA	GND	GND for PLL A
C12	PGNDA	GND	GND for PLL A
G9	PGNDA	GND	GND for PLL A
B5	PGNDB	GND	GND for PLL B
B6	PGNDB	GND	GND for PLL B
C5	PGNDB	GND	GND for PLL B
C6	PGNDB	GND	GND for PLL B
A8	PV_{DD}	3.3V	Transmit PLL V_{DD}
B9	PV_{DD}	3.3V	Transmit PLL V_{DD}
D9	PV_{DDA}	3.3V	V_{DD} for PLL A
D12	PV_{DDA}	3.3V	V_{DD} for PLL A
E12	PV_{DDA}	3.3V	V_{DD} for PLL A
A5	PV_{DDB}	3.3V	V_{DD} for PLL B
D5	PV_{DDB}	3.3V	V_{DD} for PLL B
D6	PV_{DDB}	3.3V	V_{DD} for PLL B
L2	Reset_n	Input LVTTL	Chip Reset Control
D13	Test_se	Input LVTTL	Scan Enable
F11	U_RxAddr[0]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
F10	U_RxAddr[1]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
F13	U_RxAddr[2]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
G11	U_RxAddr[3]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
G12	U_RxAddr[4]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
H11	U_RxCLAV [0]	BiDir LVTTL	Receive Cell Available — Normal/Extended PHY Port Control
G13	U_RxCLAV [1]	Input LVTTL	Receive Cell Available — Normal/Extended PHY Port Control
H12	U_RxCLAV [2]	Input LVTTL	Receive Cell Available — Normal/Extended PHY Port Control
F14	U_RxCLAV [3]	Input LVTTL	Receive Cell Available — Normal/Extended PHY Port Control
H13	U_RxCLAV [4]	Input LVTTL	Receive Cell Available — Extended PHY Port Control
H14	U_RxCLAV [5]	Input LVTTL	Receive Cell Available — Extended PHY Port Control
J13	U_RxCLAV [6]	Input LVTTL	Receive Cell Available — Extended PHY Port Control
J14	U_RxCLAV [7]	Input LVTTL	Receive Cell Available — Extended PHY Port Control
N13	U_RxData [0]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
N14	U_RxData [1]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
P14	U_RxData [2]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
L11	U_RxData [3]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
P13	U_RxData [4]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
M12	U_RxData [5]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
P12	U_RxData [6]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
K10	U_RxData [7]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
N12	U_RxData [8]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
P11	U_RxData [9]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
N11	U_RxData [10]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
M11	U_R xData [11]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
M10	U_RxData [12]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
J10	U_RxData [13]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)

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20.0 Package (Continued)

TABLE 96. Pin Locations — BGA196 Package (Continued)

Ball	Pin Name	Signal Type	Description
K9	U_RxData [14]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
L9	U_RxData [15]	BiDir LVTTL	Receive Data Bus, from the PHY Layer Device(s)
J12	U_RxENB [0]	BiDir LVTTL	Enable Data Transfers — Normal/Extended PHY Port Control
L14	U_RxENB [1]	Output LVTTL	Enable Data Transfers — Extended PHY Port Control
M14	U_RxENB [2]	Output LVTTL	Enable Data Transfers — Extended PHY Port Control
L13	U_RxENB [3]	Output LVTTL	Enable Data Transfers — Extended PHY Port Control
G10	U_RxENB [4]	Output LVTTL	Enable Data Transfers — Extended PHY Port Control
J9	U_RxENB [5]	Output LVTTL	Enable Data Transfers — Extended PHY Port Control
K11	U_RxENB [6]	Output LVTTL	Enable Data Transfers — Extended PHY Port Control
L12	U_RxENB [7]	Output LVTTL	Enable Data Transfers — Extended PHY Port Control
H10	U_RxParity	BiDir LVTTL	Receive Data Bus Parity Bit
M13	U_RxSOC	BiDir LVTTL	Receive Start of Cell
L10	U_TxAddr[0]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
N10	U_TxAddr[1]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
M9	U_TxAddr[2]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
L8	U_TxAddr[3]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
N9	U_TxAddr[4]	BiDir LVTTL	Address of MPHY Device Being Polled or Selected
M6	U_TxCLAV [0]	Bidir LVTTL	Utopia Transmit Cell Available — Normal/Extended PHY Control
P4	U_TxCLAV [1]	Input LVTTL	Utopia Transmit Cell Available — Normal/Extended PHY Control
N6	U_TxCLAV [2]	Input LVTTL	Utopia Transmit Cell Available — Normal/Extended PHY Control
K7	U_TxCLAV [3]	Input LVTTL	Utopia Transmit Cell Available — Normal/Extended PHY Control
K6	U_TxCLAV [4]	Input LVTTL	Utopia Transmit Cell Available — Extended PHY Port Control
L5	U_TxCLAV [5]	Input LVTTL	Utopia Transmit Cell Available — Extended PHY Port Control
K5	U_TxCLAV [6]	Input LVTTL	Utopia Transmit Cell Available — Extended PHY Port Control
N5	U_TxCLAV [7]	Input LVTTL	Utopia Transmit Cell Available — Extended PHY Port Control
M5	U_TxData [0]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
P3	U_TxData [1]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
N4	U_TxData [2]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
P2	U_TxData [3]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
M4	U_TxData [4]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
L4	U_TxData [5]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
N3	U_TxData [6]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
P1	U_TxData [7]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
M3	U_TxData [8]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
M2	U_TxData [9]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
N2	U_TxData [10]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
N1	U_TxData [11]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
M1	U_TxData [12]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
L3	U_TxData [13]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
K4	U_TxData [14]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
K3	U_TxData [15]	BiDir LVTTL	Transmit Data Bus, toward the PHY Layer Device(s)
P9	U_TxENB [0]	BiDir LVTTL	Utopia Enable Data Transfers — Normal/Extended PHY Control
P7	U_TxENB [1]	Output LVTTL	Utopia Enable Data Transfers — Extended PHY Control
P6	U_TxENB [2]	Output LVTTL	Utopia Enable Data Transfers — Extended PHY Control
P5	U_TxENB [3]	Output LVTTL	Utopia Enable Data Transfers — Extended PHY Control
N7	U_TxENB [4]	Output LVTTL	Utopia Enable Data Transfers — Extended PHY Control
L7	U_TxENB [5]	Output LVTTL	Utopia Enable Data Transfers — Extended PHY Control
M7	U_TxENB [6]	Output LVTTL	Utopia Enable Data Transfers — Extended PHY Control

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20.0 Package (Continued)

TABLE 96. Pin Locations — BGA196 Package (Continued)

Ball	Pin Name	Signal Type	Description
L6	U_TxENB [7]	Output LVTTL	Utopia Enable Data Transfers — Extended PHY Control
J5	U_TxParity	BiDir LVTTL	Utopia Transmit Data Bus Parity Bit
M8	U_TxSOC	BiDir LVTTL	Transmit Start of Cell
P8	U_UDBClk	Input LVTTL	Utopia Down Bridge Clock Input
K12	U_UUBClk	Input LVTTL	Utopia Up-Bridge Clock Input

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21.0 References

1. The ATM Forum UTOPIA Level 2, Version 1.0 Specification, af-phy-0039.000, June 1995
2. ITU-T I.432.1, B-ISDN User Network Interface–Physical Layer Specification: General Characteristics, August 1996.
3. The ATM Forum User-Network Interface Specification, Version 3.1, Sept. 1994.
4. IEEE 1149.1 Standard–JTAG.

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22.0 Absolute Maximum Ratings (Note 13)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage I/O (V_{CCIO})	−0.3V to 4V
Supply Voltage Core Internal (V_{CCINT})	−0.3V to 3.2V
CMOS/TTL Input and I/O Voltage	−0.3V to 3.6V
CMOS/TTL Output Voltage	−0.3V to (V_{CC} +0.3V)
LVDS DO/RIN Voltage	−0.3V to 3.6V
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +125˚C
Lead Temperature (soldering, 10 seconds)	+225˚C
Max. Package Power Dissipation Capacity	3.5 W
Package Derating	28.6 mW/˚C
ESD Rating LVDS I/O	>3 kV HBM
ESD Rating CMOS I/O	>2 kV HBM

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23.0 Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage 3.3V	3.0	3.3	3.6	V
Supply Voltage 2.5V	2.37	2.5	2.63	V
Operating Free Temperature	−40	+25	+85	˚C
CMOS/TTL Input and I/O Voltage	0	-	+3.6	V
LVDS Input/Output Voltage	0	-	+3.3	V

24.0 Electrical Characteristics

CMOS DC Specifications
Microprocessor Pins, LVDS Control Pins, and Clocks

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		Inputs	2		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage				−0.7	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V		−10	±2	+10	µA
I_{INH}	Input Current for Pulldown pins	V_{IN} = 0V			80	160	µA
I_{INL}	Input Current for Pullup pins	V_{IN} = 3.6V			−90	−160	µA
V_{OH}	High Level Output Voltage	I_{OH} = 6 mA	Outputs	2.4		V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 6 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−15	−18	−85	mA
I_{OZ}	TRI-STATE Output Current	PD* or REN = 0.8V, V_{OUT} = 0V or V_{CC} V		−10	±0.4	+10	µA

UTOPIA Bus DC Specifications

Pin types are defined in *Table 97*. Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		Inputs, BiDir	2		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage				−0.7	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V		−10	±2	+10	µA
V_{OH}	High Level Output Voltage	I_{OH} = 8 mA	Output, BiDir	2.4		V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 8 mA		GND		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−15		−85	mA
I_{OZ}	TRI-STATE Output Current	PD* or REN = 0.8V, V_{OUT} = 0V or V_{CC} V		−10	±0.4	+10	µA

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24.0 Electrical Characteristics (Continued)

Bus LVDS DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14) LVDS Specifications are for LVDS Input and Output pins only. Control inputs and clocks are specified under Control Pin and Clocks DC Specifications.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
V_{TH}	Differential Threshold High Voltage	V_{CM} = 1.1V	LVDS_ADin[+,–] LVDS_BDin[+,–]		+50	+100	mV
V_{TL}	Differential Threshold Low Voltage			–100 mV	–50		mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V or 0V		–10	±5	+10	µA
		V_{IN} = 0V, V_{CC} = 3.6V or 0V		–10	±5	+10	µA
V_{OD}	Output Differential Voltage (DO+)–(DO–)	R_L = 100Ω	LVDS_ADout[+,–] LVDS_BDout[+,–]	350	450	550	mV
DV_{OD}	Output Differential Voltage Unbalance				2	35	mV
V_{OS}	Offset Voltage			0.9	1.0	1.3	V
I_{OS}	Output Short Circuit Current	DO = 0V, D_{IN} = H, TXPWDN* and DEN = 2.4V		–35	–50	–70	mA
I_{OZ}	TRI-STATE Output Current	TXPWDN* or DEN = 0.8V, DO = 0V or V_{DD}		–10	±1	10	µA
I_{OX}	Power-Off Output Current	V_{DD} = 0V, DO = 0V or 3.6V		–10	±1	10	µA

Supply Current, V_{CC} = 2.5V

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
I_{CCR}	Worst Case Supply Current	Utopia C_L = 15 pF, Bus LVDS R_L = 100Ω, Checker Pattern, CVDD = 2.63V	52 MHz		200	260	mA
I_{CCT}	Typical Loading and Switching	C_L = 15 pF, PRBS7 Data Pattern	33 MHz		112	140	mA

Supply Current, V_{CC} = 3.3V

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
I_{CCR}	Worst Case Supply Current	Utopia C_L = 15 pF, Bus LVDS R_L = 100Ω, Checker Pattern, VDD = 3.6V	52 MHz		270	360	mA
I_{CCT}	Typical Loading and Switching	C_L = 15 pF, PRBS7 Data Pattern	33 MHz		140	165	mA

UTOPIA Bus Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{UCP}	Input Clock Period		U_UUBClk, U_UDBClk	20			ns
t_{UDC}	Input Clock Duty Cycle			40	50	60	%
t_{UJIT}	Input Clock Jitter				1	5	%

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24.0 Electrical Characteristics (Continued)

UTOPIA Bus Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{USETUP}	Input Data Valid before CLK	C_L = 30 pF, (*Figure 31*)	Inputs	4			ns
t_{UHOLD}	Input Data Valid after CLK	C_L = 30 pF, (*Figure 31*)		1			ns
t_{ULH}	Output Low-to-High Transition Time	C_L = 30 pF, (*Figure 31*)	Outputs	1		8	ns
t_{UHL}	Output High-to-Low Transition Time	C_L = 30 pF, (*Figure 31*)		1		8	ns
t_{UROS}	Output Data Valid before CLK	C_L = 30 pF, (*Figure 31*)		4			ns
t_{UROH}	Output Data Valid after CLK	C_L = 30 pF, (*Figure 31*)		1			ns
t_{UHZR}	High to TRI-STATE Delay	(*Figure 32*)		1		16	ns
t_{ULZR}	Low to TRI-STATE Delay			1		16	ns
t_{UZHR}	TRI-STATE to High Delay			1		16	ns
t_{UZLR}	TRI-STATE to Low Delay			1		16	ns

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Pin Name	ATM Mode	PHY Mode
U_TxData[15:0]	Output	Input
U_Tx Parity	Output	Input
U_Tx CLAV[7:4]	Input	*
U_TxCLAV[3:0]	Input	Output
U_TxENB[7:1]	Output	*
U_TxENB[0]	Output	Input
U_TxSOC	Output	Input
U_TxAddr[4:0]	Output	Input
U_RxData[15:0]	Input	Output
U_Rx Parity	Input	Output
U_Rx CLAV[7:4]	Input	*
U_RxCLAV[3:0]	Input	Output
U_RxENB[7:1]	Output	*
U_RxENB[0]	Output	Input
U_RxSOC	Input	Output
U_RxAddr[4:0]	Output	Input

*The extended addressing pins U_TxCLAV[7:4], U_RxCLAV[7:4], U_TxENB[7:1], and U_RxENB[7:1] are defined for ATM mode only.

LVDS Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{LLH}	LVDS Low-to-High Transition Time	R_L = 100, C_L = 10 pF, (*Figure 25*)	LVDS_ADout[+,–], LVDS_BDout[+.,–]		300	400	ps
t_{LHL}	LVDS High-to-Low Transition Time	R_L = 100, C_L = 10 pF, (*Figure 25*)			300	400	ps
t_{RJIT}	Random Jitter of LVDS Tx Clock				60	150	ps
t_{DJIT}	Deterministic Jitter of LVDS Tx Data					150	ps

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24.0 Electrical Characteristics (Continued)

LVDS Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{DSR1}	Deserializer PLL Lock Time from PWRDN (with SYNCPAT)	(*Figure 28*)	LVDS_ADin[+,–], LVDS_BDin[+.,–]			30	µs
t_{DRS2}	Deserializer PLL Lock Time from SYNCPAT	(*Figure 29*)				12	µs
t_{RNM}	Deserializer Noise Margin	(*Figure 30*)		400			ps

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Timing Requirements for Input Clock LVDS_TxClk, LVDS_ARefClk, LVDS_BRefClk

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RFCP}	REFCLK Period			19.2			ns
t_{RFDC}	REFCLK Duty Cycle			40	50	60	%
t_{RFCP}/t_{TCP}	Ratio of REFCLK to TCLK			–5		5	%
t_{RFTT}	REFCLK Transition Time	(*Figure 27*)				8	ns
t_{JIT}	Input Jitter	Jitter Frequency < 250 kHz				15	UI
		Jitter Frequency < 250 kHz				1.5	UI
		Jitter Frequency < 250 kHz				0.15	UI

Microprocessor Interface Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 14)

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{LLH}	Low-to-High Transition Time	C_L = 15 pF (*Figure 26*)	Outputs			6	ns
t_{LHL}	High-to-Low Transition Time	C_L = 15 pF (*Figure 26*)				6	ns
t_{SETUP}		See *Section 17.0 Microprocessor Interface Operation*	Inputs				
t_{HOLD}							

Note 13: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 14: Typical values are given for V_{CC} = 3.3V and T_A = 25˚C

Note 15: Current into the device is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except V_{OD}, V_{TH} and V_{TL} which are differential voltages.

Note 16: For the purpose of specifying deserializer P_{LL} performance t_{DSR1} and t_{DSR2} are specified with the REFCLK running and stable, and specific conditions of the incoming data stream (SYNCPATs). t_{DSR1} is the time required for the deserializer to indicate lock upon power-up or when the power-down mode. t_{DSR2} is the time required to indicate lock for the powered-up and enabled deserializer when the input (RI+ and RI–) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs). The time to lock to random data is dependent upon the incoming data.

Note 17: t_{RNM} is a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur.

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24.0 Electrical Characteristics (Continued)

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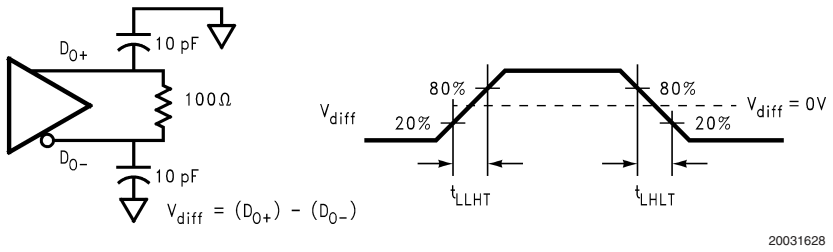

FIGURE 25. LVDS Rise and Fall times

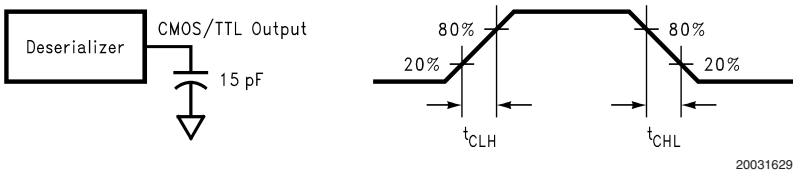

FIGURE 26. CMOS Rise and Fall times

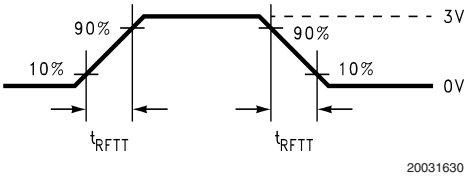

FIGURE 27. REFCLK Transition time

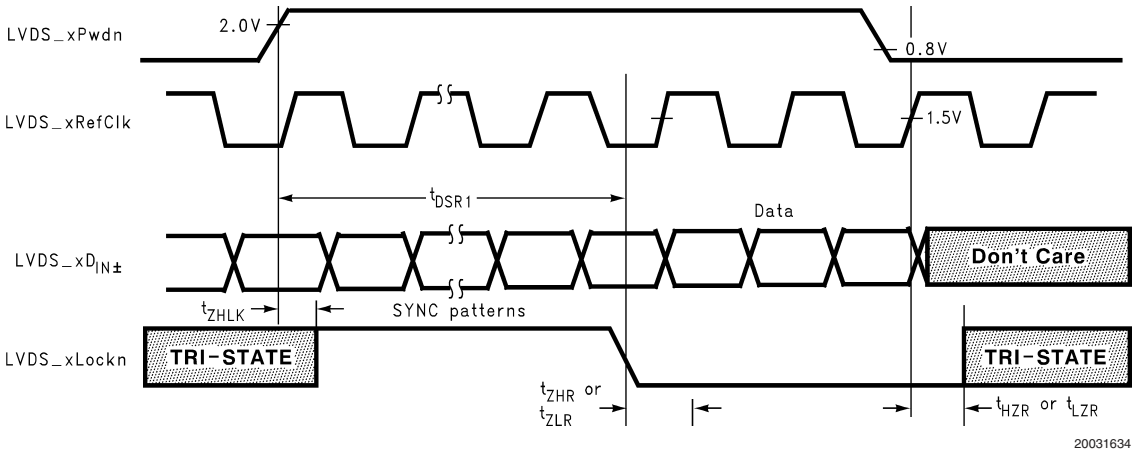

FIGURE 28. Deserializer lock time t_{DSR1}

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24.0 Electrical Characteristics (Continued)

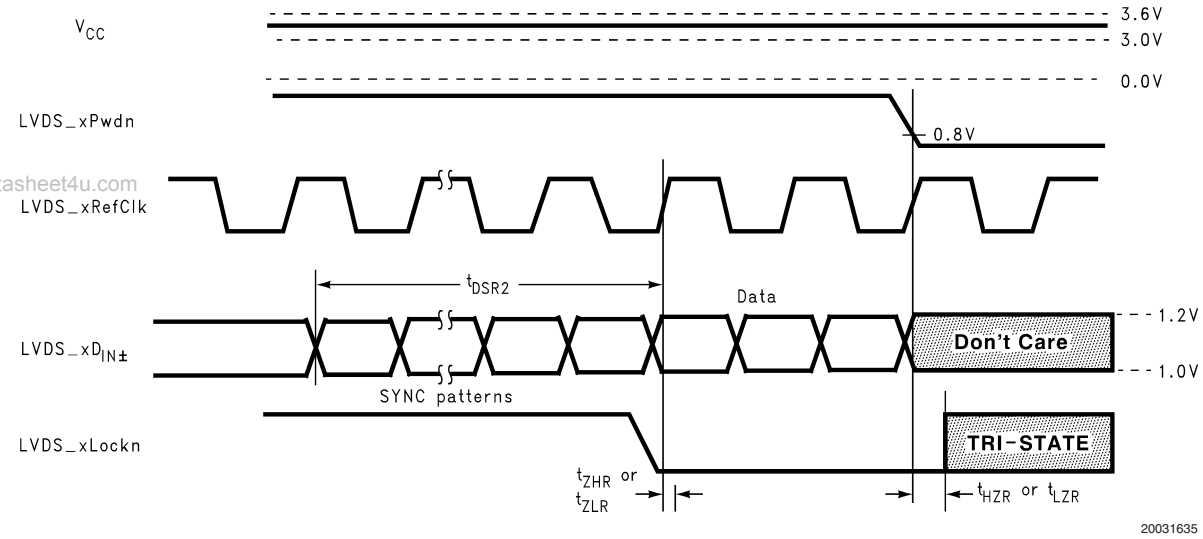

FIGURE 29. Deserializer lock time t_{DSR2}

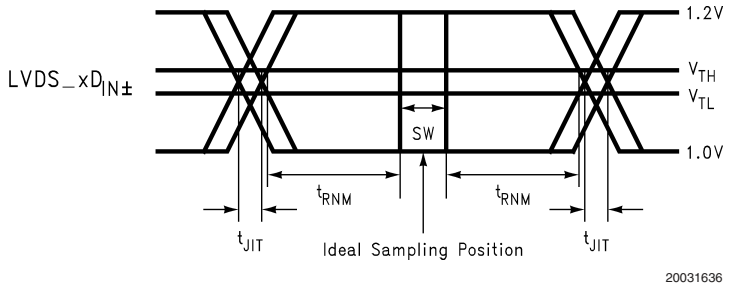

FIGURE 30. Deserializer Noise Margin

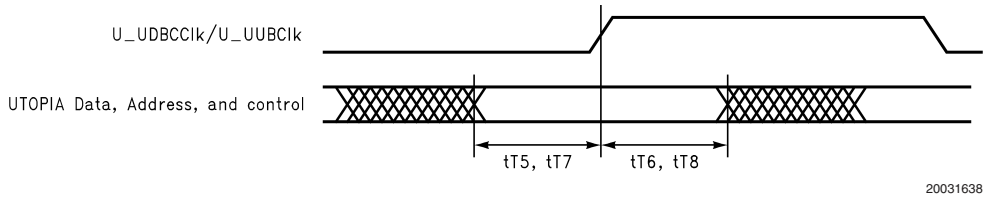

FIGURE 31. UTOPIA Setup and Hold Time Definition

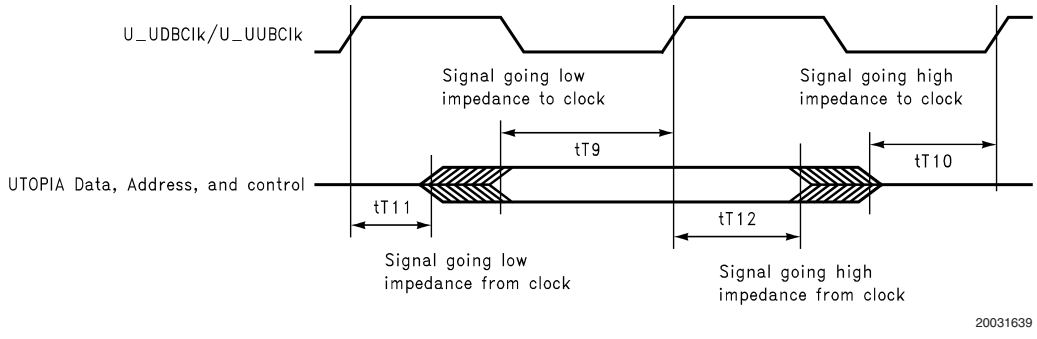

FIGURE 32. UTOPIA TRI-STATE Timing

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24.0 Electrical Characteristics (Continued)

TABLE 97. UTOPIA Transmit Timing

Signal Name	DIR	Item	Description	Min	Max
U_UDBClk, U_UUBClk	A → P	f1	TxClk Frequency (nominal)	0	50 MHz
		tT2	TxClk Duty Cycle	40%	60%
		tT3	TxClk Peak-to-Peak Jitter	—	5%
		tT4	TxClk Rise/Fall Time	—	2 ns
U_TxData[15:0], U_TxPrty, U_TxSOC, U_TxEnb[7:0], U_TxAddr[4:0]	A → P	tT5	Input Setup to TxClk	4 ns	—
		tT6	Input Hold from TxClk	1 ns	—
U_TxClav [7:0]	A ← P	tT7	Input Setup to TxClk	4 ns	—
		tT8	Input Hold from TxClk	1 ns	—
		tT9	Signal Going Low Impedance to TxClk	4 ns	—
		tT10	Signal Going High Impedance to TxClk (1)	0 ns	—
		tT11	Signal Going Low Impedance from TxClk	1 ns	—
		tT12	Signal Going High Impedance from TxClk	1 ns	—

TABLE 98. UTOPIA Receive Timing

Signal Name	DIR	Item	Description	Min	Max
U_UDBClk, U_UUBClk	A → P	f1	RxClk Frequency (nominal)	0	50 MHz
		tT2	RxClk Duty Cycle	40%	60%
		tT3	RxClk Peak-to-Peak Jitter	—	5%
		tT4	RxClk Rise/Fall Time	—	2 ns
U_RxEnb[7:0], U_RxAddr[4:0]	A → P	tT5	Input Setup to RxClk	4 ns	—
		tT6	Input Hold from RxClk	1 ns	—
U_RxData[15:0], U_RxParity, U_RxSOC, U_RxClav [7:0]	A ← P	tT7	Input Setup to RxClk	4 ns	—
		tT8	Input Hold from RxClk	1 ns	—
		tT9	Signal Going Low Impedance to RxClk	4 ns	—
		tT10	Signal Going High Impedance to RxClk (2)	0 ns	—
		tT11	Signal Going Low Impedance from RxClk	1 ns	—
		tT12	Signal Going High Impedance from RxClk	1 ns	—

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25.0 Appendix A: Layout and Connection Guidelines

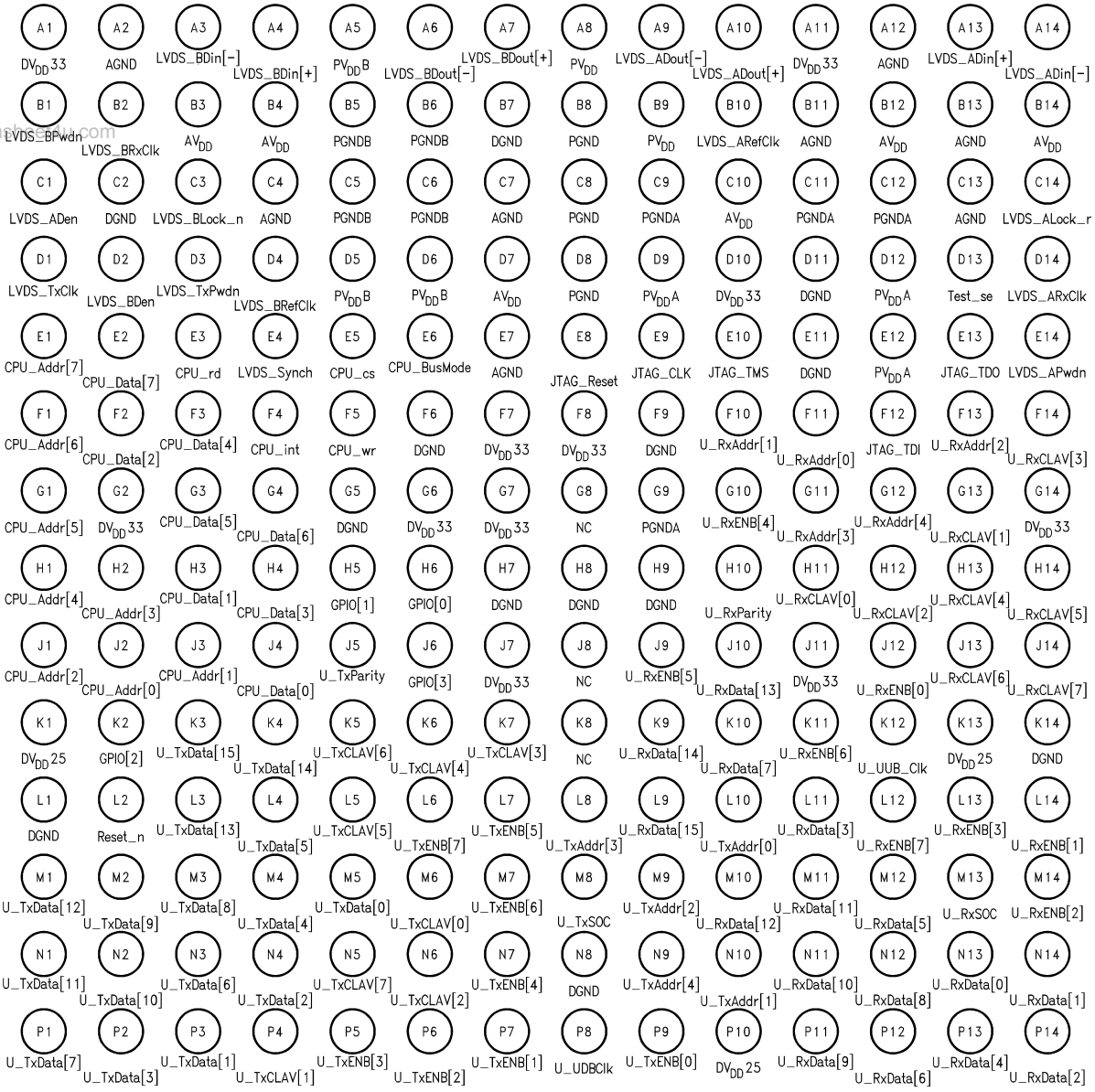

FIGURE 33. Block Diagram Is a Top View of 196 LBGA Ball Assignment.

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25.0 Appendix A: Layout and Connection Guidelines (Continued)

25.1 POWER CONNECTIONS

25.1.1 Digital Supplies (DV_{DD} and DGND)

The digital supply pins provide power to the digital section of the device. Since the digital supplies are subject to switching noise, the bypass considerations are important. The DV_{DD} and DGND balls are located mostly in the center of the ball array. If the PCB stack-up and signal routing allows placing bypass caps on the bottom of the board close to the digital supply pins, then an array of capacitors will provide wide band bypassing. The total bypass capacitance should be at least 0.3 µF.

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The 2.5V supply pins are located near the edge of the package, which is more convenient for placement of bypass capacitors. If a power plane supplies the 2.5V, then standard bypass capacitors of 0.1 µF in parallel with 0.01 µF is sufficient. If the PCB traces connect the 2.5V to the part, then additional bulk decoupling capacitance should account for the added trace inductance.

25.1.2 Analog Supplies (AV_{DD} and AGND)

The analog V_{DD} and GND power the LVDS driver and receiver section of the device. High frequency bypassing such as 0.001 µF capacitance is required due to the very high data rates of the LVDS signals. See *Figure 34*.

25.1.3 PLL Supplies (PV_{DD} and PGND)

The PLL supply pins provide power for the PLL(s) in the circuit. The most important function of bypassing or filtering for the PLL inputs is to attenuate low frequency noise from entering the PV_{DD} pins. A common source of low frequency noise is switching power supplies. Power distribution networks should be designed to attenuate any harmonics created by the switching supply. The addition of a PI filter network at the PV_{DD} pins is optional. See *Figure 34*.

25.2 LAYOUT GUIDELINES

25.2.1 Digital Supplies (DV_{DD} and DGND)

Digital supply connection to bypass capacitors can be difficult, but the more layers in the PCB the easier it is to place the capacitors near the device. Therefore, the recommendation is to use full power planes to distribute power to these pins. Using the minimum manufacturing thickness between the ground and power planes creates a distributed bypass capacitance. Due to the potentially high inrush currents caused by Utopia bus output switching, using traces routed through the array to connect bypass caps to the balls is not recommended. This is because the inductance of the traces will negate the affect of the bypass capacitors.

25.2.2 Analog Supplies (AV_{DD} and AGND)

In general, the analog supply pins can be connected to the digital power planes. The AGND pins should be connected to a ground plane that connects them directly to the AGND pins of the sending device. This provides for minimum ground offset between the devices and provides a return path for the minute return currents from the LVDS receivers.

25.2.3 PLL Supplies (PV_{DD} and PGND)

The PLL supply pins should be isolated from the shared digital and analog power planes. PV_{DD} and PGND pins are generally grouped together to allow them to be connected to a split plane or to a “copper pour” on the top layer. The split plane or copper pour is connected to the power planes through a PI filter to block low frequency noise. High frequency bypassing should be provided on the PLL side of the filter to supply switching current to the PLL. A separate filter for each PLL is recommended. If filters are not desired use a high value (5 µF to 400 nF) capacitor connected to the PV_{DD} pins to limit low frequency noise.

25.2.4 LVDS I/O

The LVDS I/O pins are located on the outer ring of balls so they can be routed on the surface layer to minimize added capacitance. Use surface mount resistors to terminate transmission lines as close to the LVDS inputs as possible. The LVDS drivers on the DS92UT16 are designed to drive 100Ω differential lines.

The LVDS A driver outputs (LVDS_Adin[+/–]) are swapped in position compared to the other LVDS I/O pairs. This allows them to be “wrapped around ” a connector pin array so that all of the LVDS signals can be routed on the surface layer. See *Figure 35*.

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25.0 Appendix A: Layout and Connection Guidelines (Continued)

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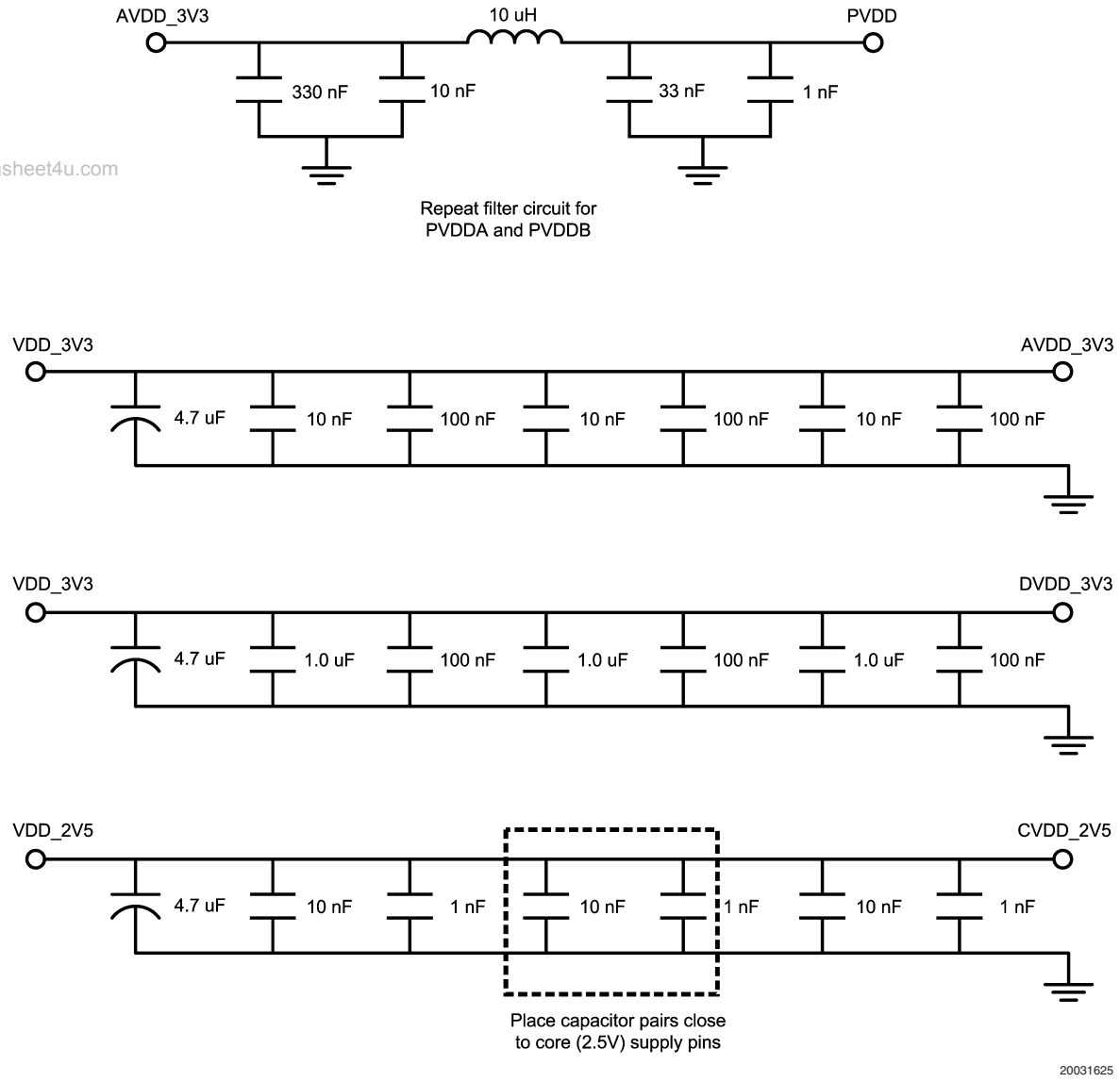

FIGURE 34. Recommended bypassing and filtering for the Analog and PLL power supplies on the DS92UT16 Utopia-LVDS Bridge.

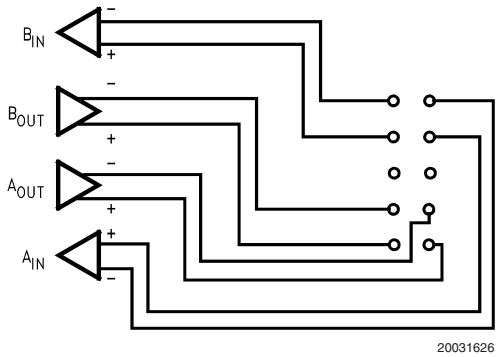

FIGURE 35. Diagram shows routing high-speed LVDS lines on one layer to a connector header.

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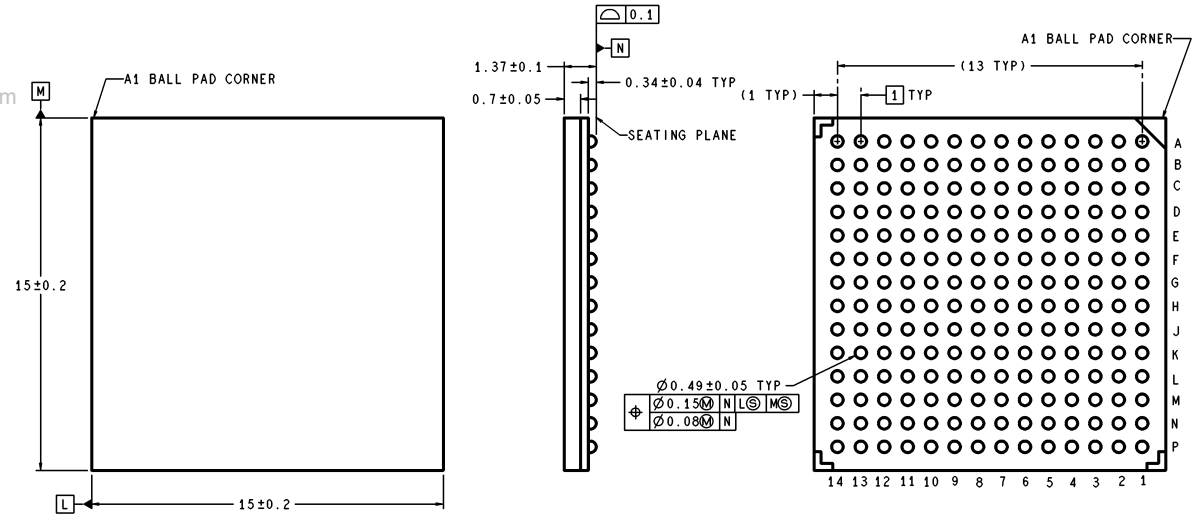
26.0 Physical Dimensions inches (millimeters) unless otherwise noted



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