

### General Description

The QPL9095 is a high-linearity, ultra-low noise gain block amplifier with a bypass mode functionality integrated in the product. At 900MHz, the amplifier typically provides 22 dB gain, +33 dBm OIP3, and 0.6 dB noise figure while drawing 50 mA current from a +4.2 V supply.

The QPL9095 is internally matched using a high performance E-pHEMT process and only requires four external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors. This low noise amplifier contains an internal active bias to maintain high performance over temperature.

The QPL9095 is optimized for the 500MHz–2000MHz frequency band and is targeted for wireless infrastructure. The QPL9095 is packaged in a 2 x 2 mm DFN.



8 Pin 2X2 mm DFN Package

### Product Features

- 500MHz – 2000MHz Operational bandwidth
- LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- Ultra low noise, 0.6 dB at 900MHz
- 22 dB Gain at 900MHz
- +33 dBm Output IP3 in LNA Mode
- +35 dBm Output IP3 in Bypass Mode
- Internally matched
- Positive supply only, +3.3 to +5 V
- 2x2 mm 8-pin DFN plastic package

### Functional Block Diagram



Top View

### Applications

- Base-station Receivers
- Repeaters / DAS
- Tower Mounted Amplifiers
- Mobile Infrastructure
- General Purpose Wireless
- TDD or FDD systems

### Ordering Information

Part No.	Description
QPL9095TR7	2500 pcs on 7" reel
QPL9095EVB01	Evaluation Board

## Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
Supply Voltage (V <sub>DD</sub> )	+7 V
RF Input Power, CW, 50Ω, T=25°C	+30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V <sub>DD</sub> )	3.0	4.2	5.25	V
T <sub>CASE</sub>	-40		+105	°C
T <sub>j</sub> at T <sub>CASE</sub> = 125°C			+142	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Test conditions unless otherwise noted: V<sub>DD</sub> = +4.2 V, Temp.=+25°C.

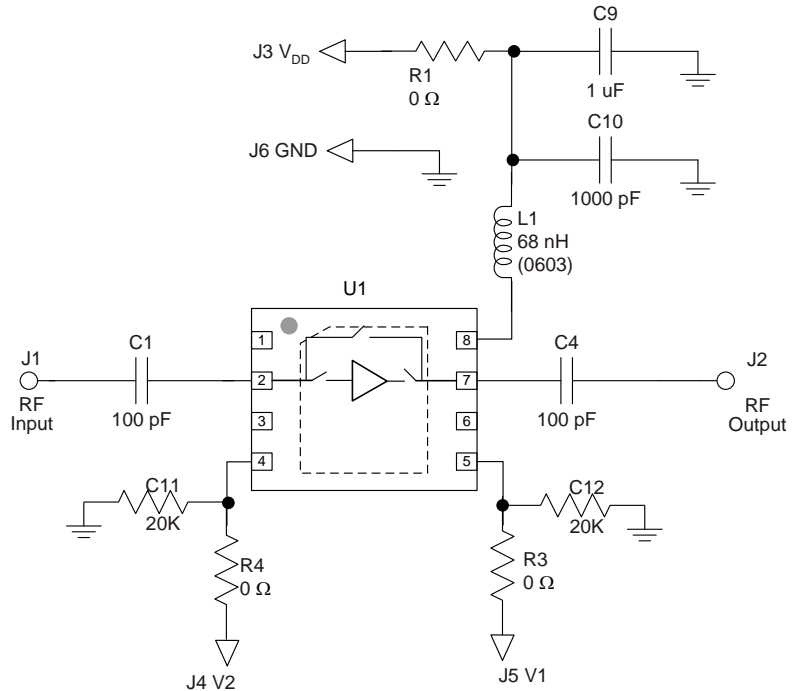
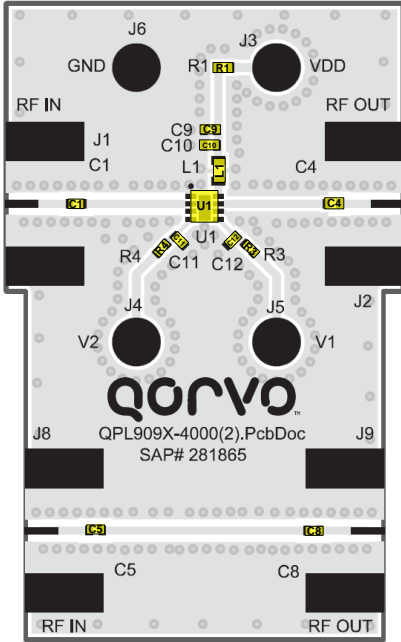
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		500		2000	MHz
Test Frequency			900		MHz
Gain	LNA ON, Bypass OFF	20.5	22	23.5	dB
Input Return Loss	LNA ON, Bypass OFF		8.5		dB
Output Return Loss	LNA ON, Bypass OFF		11		dB
Noise Figure <sup>(2)</sup>	LNA ON, Bypass OFF		0.6	0.9	dB
Output P1dB <sup>(1)</sup>	LNA ON, Bypass OFF	+18.5	+20		dBm
Output IP3	LNA ON, Bypass OFF, P <sub>out</sub> =+2 dBm/tone, Δf=1 MHz	+30	+33		dBm
Insertion Loss	LNA OFF, Bypass ON		1.2	2.5	dB
Return Loss	LNA OFF, Bypass ON		12		dB
Isolation <sup>(1)</sup>	LNA OFF, Bypass OFF	15	18		dB
Output IP3	LNA OFF, Bypass ON Pin=+2 dBm/tone, Δf=1 MHz	+30	+35		dBm
Control Voltage, V <sub>1</sub> , V <sub>2</sub>	V <sub>IH</sub>	1.17		V <sub>DD</sub>	V
	V <sub>IL</sub>	0		0.63	V
Current, I <sub>D</sub>	Bypass OFF	40	53	75	mA
	Bypass ON		5		mA
Switching Speed	LNA-Bypass (50% V <sub>ctrl</sub> to 10% RF)		40		ns
	Bypass-LNA(50% V <sub>ctrl</sub> to 90% RF)		185		ns
	LNA-OFF(50% V <sub>ctrl</sub> to 10% RF)		40		ns
	OFF-LNA(50% V <sub>ctrl</sub> to 90% RF)		65		ns
Thermal Resistance, θ <sub>jc</sub>	Channel to case		44		°C/W

1. Minimum specification listed is guaranteed by design. Not tested in production.
2. Input trace loss de-embedded from Noise Figure data.

## Control Truth Table

V <sub>BYP</sub>	V <sub>SD</sub>	State
0	0	LNA ON, Bypass OFF
0	1	LNA OFF, Bypass OFF
1	x	LNA OFF, Bypass ON

**QPL9095 Evaluation Board**



Notes:

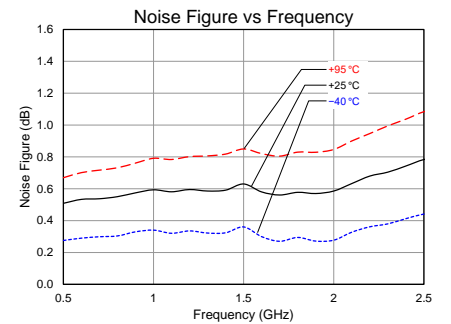
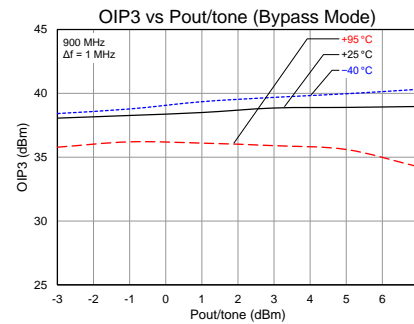
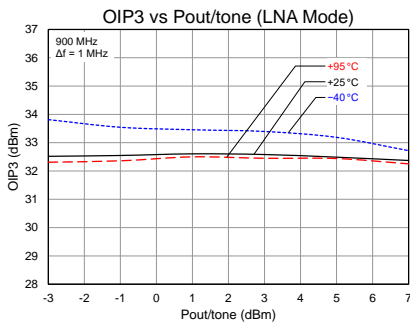
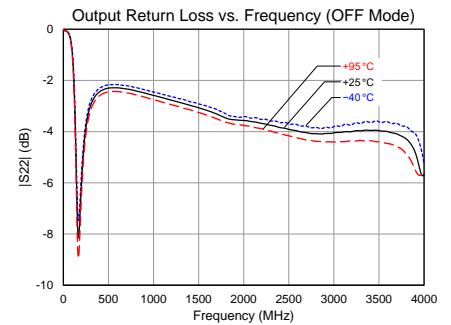
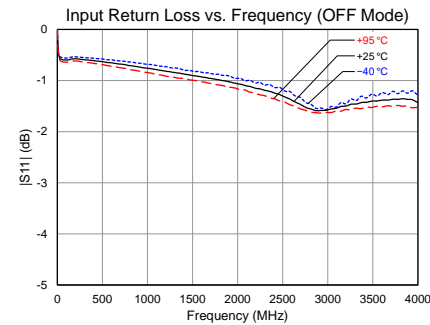
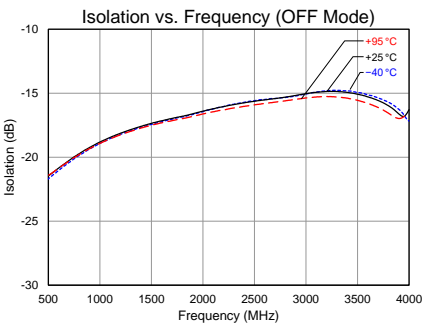
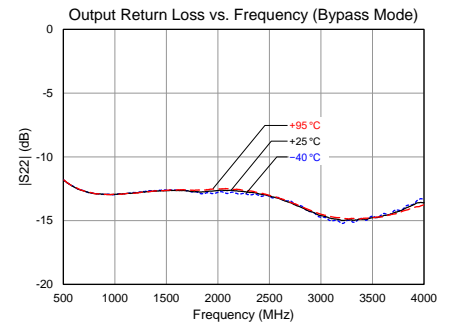
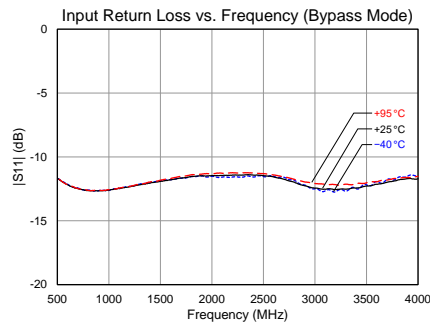
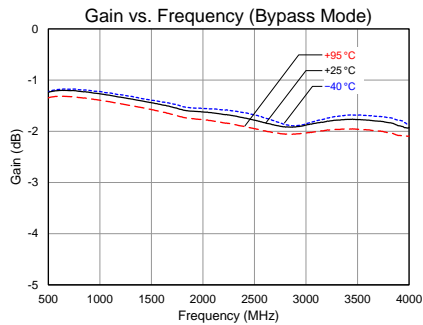
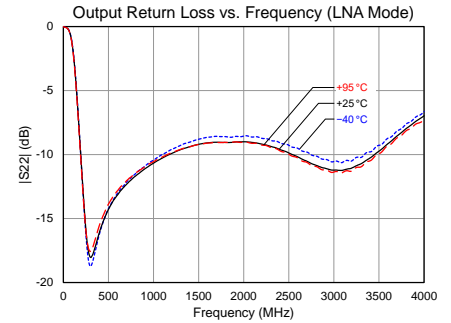
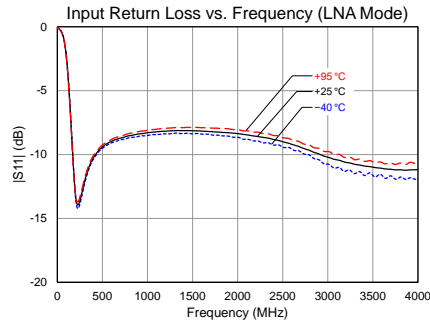
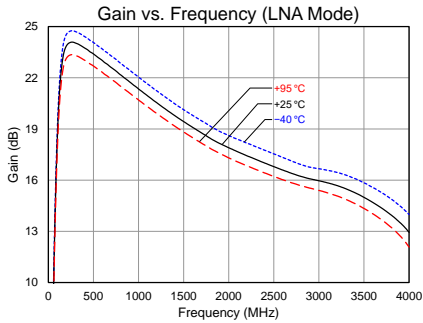
- 1. A through line is included on the evaluation board to de-embed the board losses.

**Bill of Material – QPL9095 Evaluation Board**

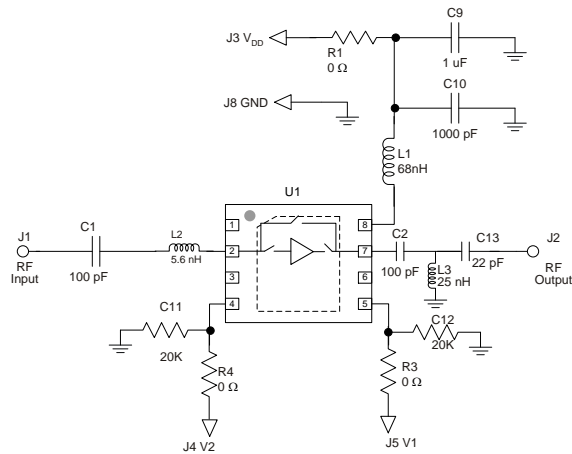
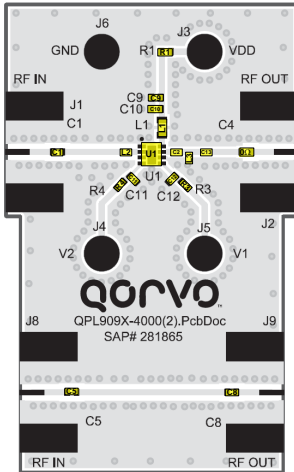
Reference Des.	Value	Description	Manuf.	Part Number
N/A	N/A	Printed Circuit Board	Qorvo	
U1	n/a	Ultra Low Noise, Bypass LNA	Qorvo	QPL9095
C10	1000 pF	CAP, 0402, 10%, 50V, X7R	Murata	GRM155R71H102KA01D (1067924)
C9	1.0 uF	Cap., 0402, 10%, 6.3V, X5R	Murata	GRM155R60J105KE19D (1068381)
C1, C4, C5, C8	100 pF	Cap., 0402, 5%, 50V, NPO/COG	Murata	GRM1555C1H101JZ01D (1068365)
R1, 3, 4	0 Ω	Resistor, Chip, 0402, 5%, 1/16W	Various	
C11, C12	20K	Resistor, Chip, 0402, 5%, 1/16W	Various	
L1	68 nH	Inductor, 0603, 5%, coil	Coilcraft	

## Performance Plots

Test conditions unless otherwise noted:  $V_{DD} = +4.2\text{ V}$ ,  $Temp. = +25\text{ }^{\circ}\text{C}$

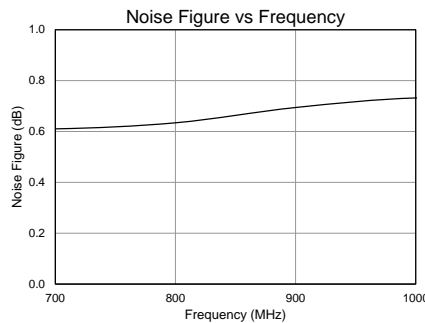
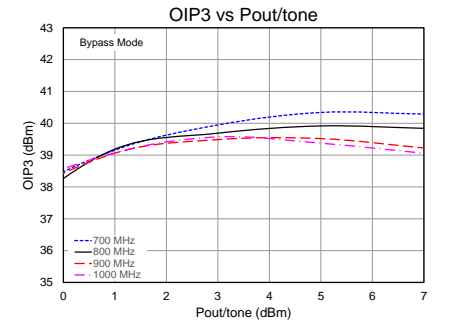
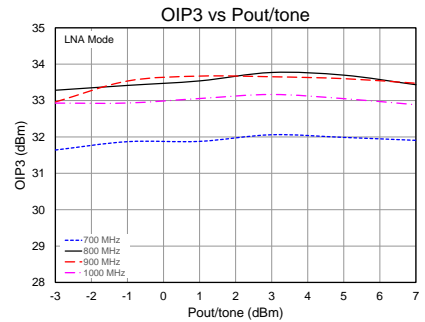
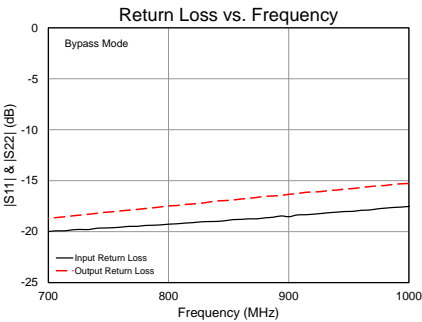
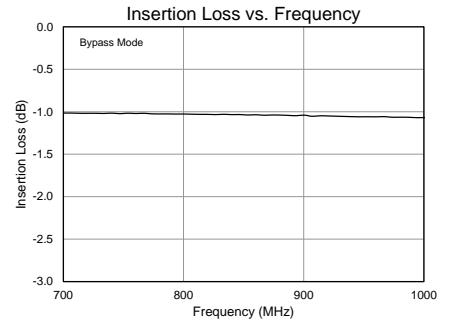
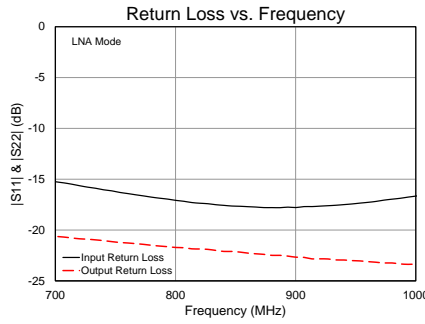
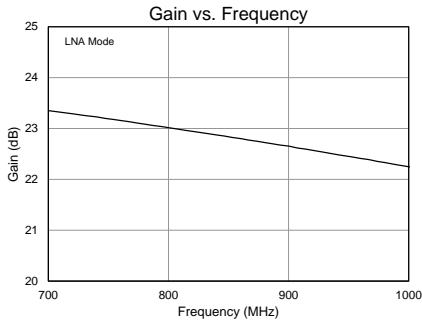


**QPL9095 Improved Return Loss Tune**

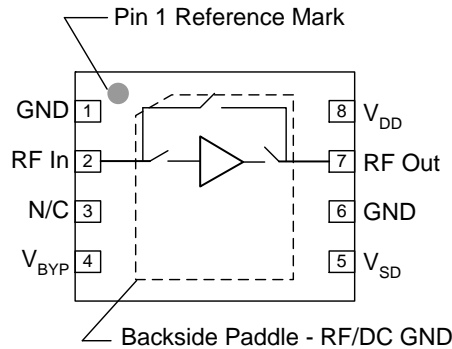


**Performance Plots**

Test conditions unless otherwise noted:  $V_{DD} = +4.2\text{ V}$ ,  $\text{Temp.} = +25\text{ }^\circ\text{C}$



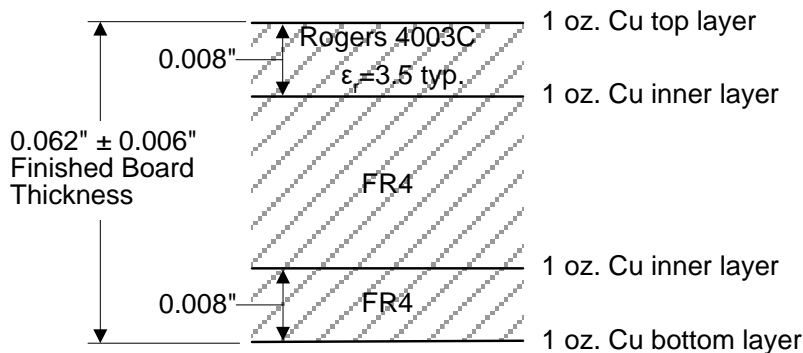
## Pin Configuration and Description



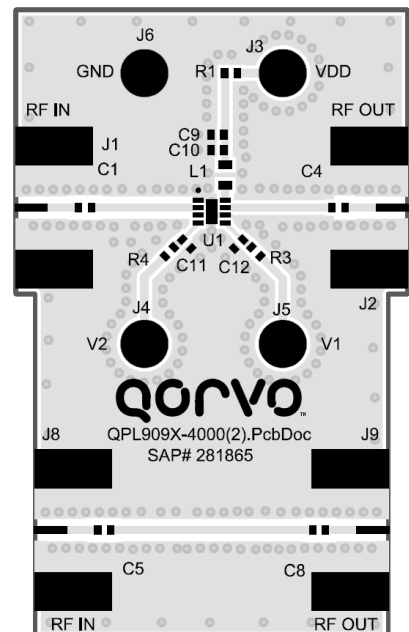
Pin No.	Label	Description
1, 6	GND	RF/DC Ground pin.
2	RFin	RF input pin. DC block required.
3	N/C	No internal connection. Provide grounded PCB land pads for mounting integrity.
4	V <sub>BYP</sub>	Control pin for bypass mode. The LNA is automatically turned off when the bypass mode is activated. Refer to truth table on pg 2.
5	V <sub>SD</sub>	Control pin to disable the LNA. Refer to truth table on pg. 2.
7	RFout	RF output pin. DC block required.
8	V <sub>DD</sub>	Supply voltage pin. External choke and bypass capacitors needed.
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

## Evaluation Board PCB Information

### Qorvo PCB 281865 Material and Stack-up

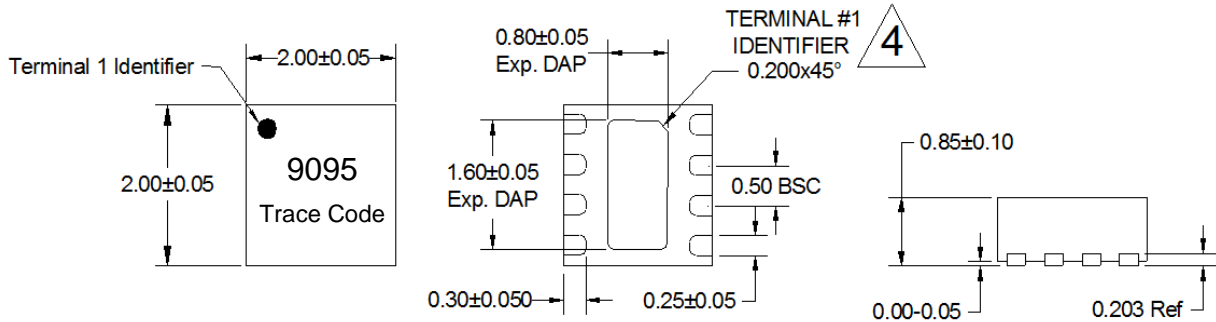


50 ohm line dimensions: width = 0.0182", spacing = 0.020"



**Mechanical Information**

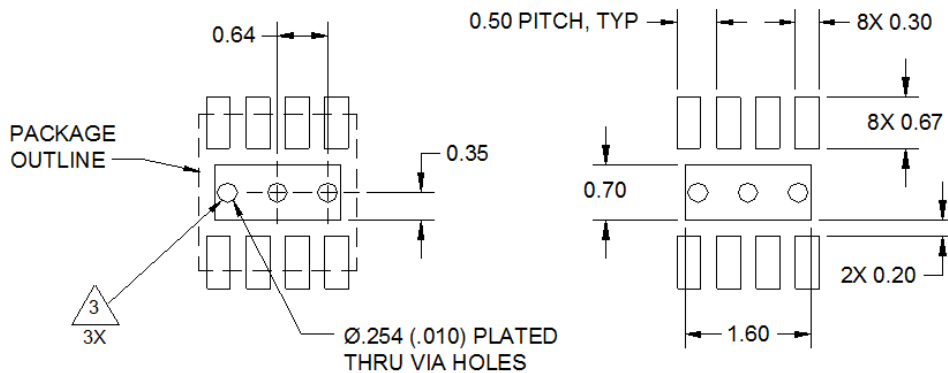
**Package Marking and Dimensions**



**Notes:**

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

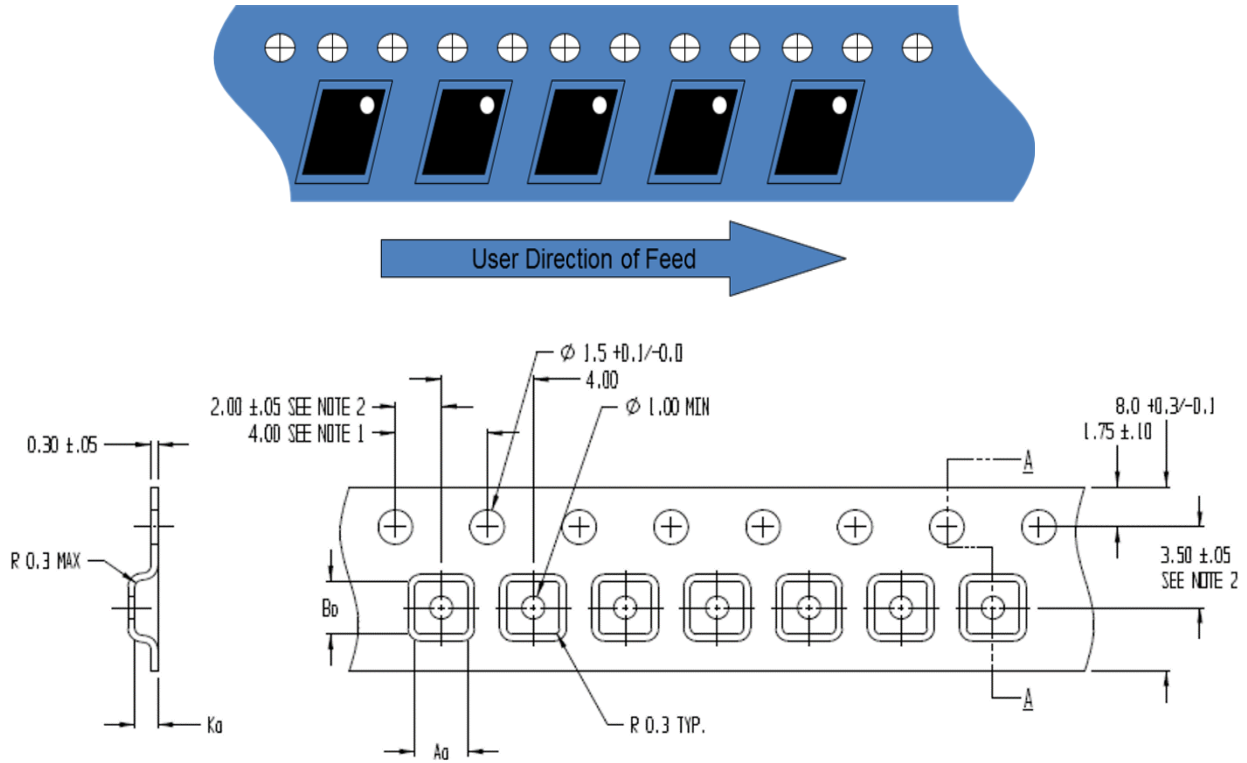
**PCB Mounting Pattern**



**Notes:**

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a  $0.35$  mm ( $\#80/.0135$ " ) diameter bit for drilling via holes and a final plated thru diameter of  $0.25$  mm ( $0.10$ " ).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

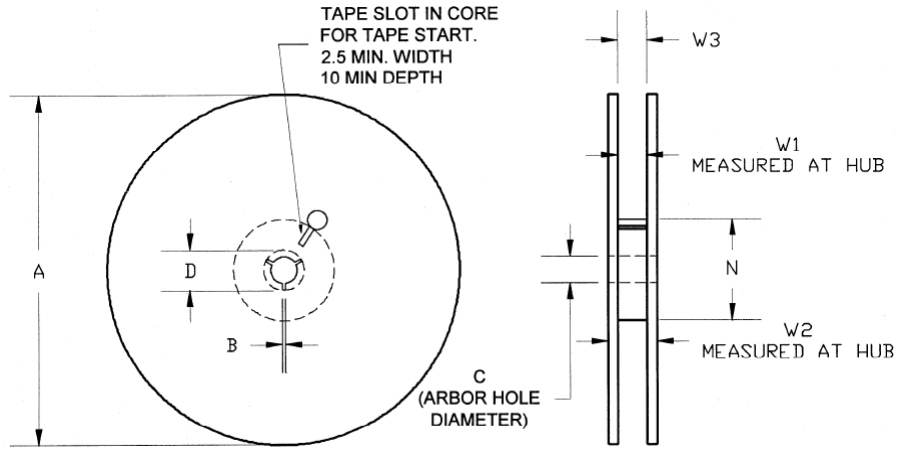


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.051	1.30
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00



**Tape and Reel Information – Reel Dimensions**

Standard T/R size = 2,500 pieces on a 7" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.293	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

**Tape and Reel Information – Tape Length and Label Placement**



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
  2. Labels are placed on the flange opposite the sprockets in the carrier tape.

## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	Class C3	ESDA / JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	1	IPC/JEDEC J-STD-020



Caution!  
ESD-Sensitive Device

## Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.  
Solder profiles available upon request.

Contact plating: NiPdAu

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free



## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.qorvo.com](http://www.qorvo.com)

**Tel:** 1-844-890-8163

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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