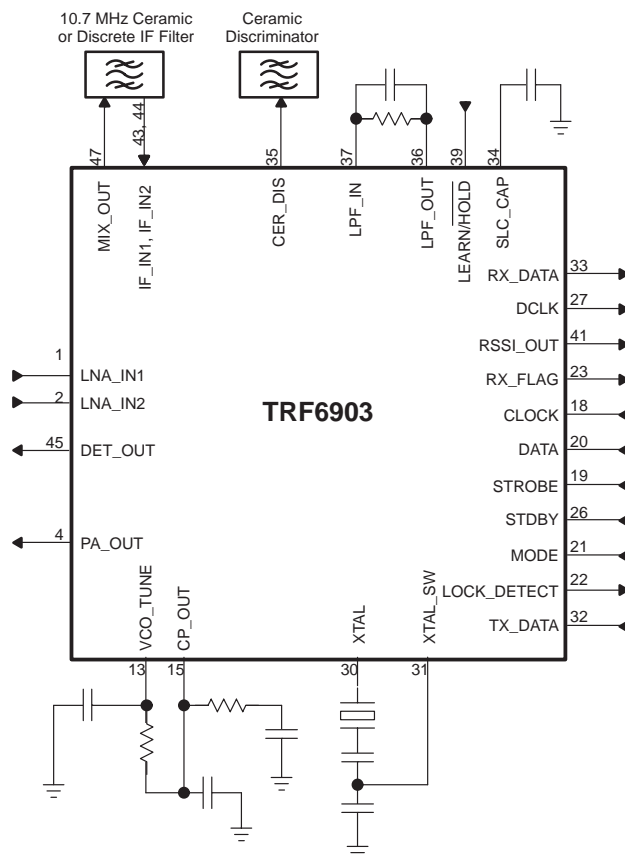


TRF6903 SINGLE-CHIP MULTIBAND RF TRANSCEIVER

SWRS022D – MARCH 2004 – REVISED JUNE 2005

- Single-Chip RF Transceiver for 315-MHz, 433-MHz, 868-MHz, and 915-MHz Industrial, Scientific, and Medical (ISM) Bands
- 2.2-V to 3.6-V Operation
- Low Power Consumption
- FSK/OOK Operation
- Integer-N Synthesizer With Fully Integrated Voltage Controlled Oscillator (VCO)
- On-Chip Reference Oscillator and Phase-Locked Loop (PLL)
- Power Amplifier With 8-dBm Typical Output Power
- Programmable Brownout Detector
- Clock Recovery With Integrated Data Bit Synchronizer and Baud Rate Selection
- Linear Receive Strength Signal Indicator (RSSI)
- Flexible 3-Wire Serial Interface
- Minimal Number of External Components Required
- 48-Pin Low-Profile Plastic Quad Flat Package (PQFP)
- Programmable XTAL Trimming
- Lock Detect Indicator
- Programmable Training Sequence Recognition
- Pin Compatible to the TRF6901



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

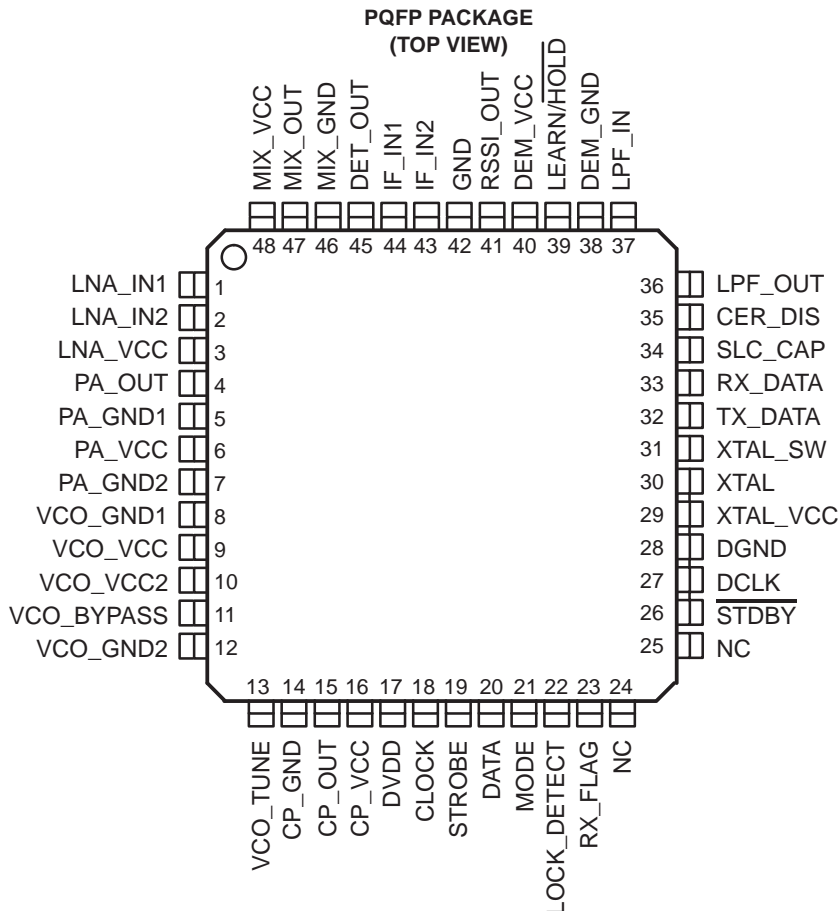
 **TEXAS
INSTRUMENTS**

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TRF6903 SINGLE-CHIP MULTIBAND RF TRANSCEIVER

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description

The TRF6903 single-chip solution is an integrated circuit intended for use as a low-cost multiband FSK or OOK transceiver to establish a frequency-programmable, half-duplex, bidirectional RF link. The multichannel transceiver is intended for digital (FSK, OOK) modulated applications in the North American and European 315-MHz, 433-MHz, 868-MHz, and 915-MHz ISM bands. The single-chip transceiver operates down to 2.2 V and is designed for low power consumption. The synthesizer has a typical channel spacing of better than 200 kHz and features a fully-integrated VCO. Only the PLL loop filter is external to the device.

Two fully-programmable operation modes, Mode0 and Mode1, allow extremely fast switching between two preprogrammed settings (for example, receive (RX)/transmit (TX); TX_frequency_0/TX_frequency_1; RX_frequency_0/RX_frequency_1; ...) without reprogramming the device.

ISM band standards

Europe has assigned an unlicensed frequency band of 868 MHz to 870 MHz. This band is specifically defined for short range devices with duty cycles from 0.1% to 100% in several subbands. The new European frequency band, due to the duty cycle assignment, allows a reliable RF link and makes many new applications possible.

The North American unlicensed ISM band covers 902 MHz to 928 MHz (center frequency of 915 MHz), and is suitable for short range RF links.



transmitter

The transmitter consists of an integrated VCO and tank circuit, a complete integer-N synthesizer, and a power amplifier. The dividers, prescaler, and reference oscillator require only the addition of an external crystal and a loop filter to provide a complete PLL with a typical frequency resolution of better than 200 kHz.

Since the typical RF output power is approximately 8 dBm, no additional external RF power amplifier is necessary in most applications.

Four attenuation settings for the power amplifier are offered. This feature allows the user to fine tune the amplifier for optimal output power.

receiver

The integrated receiver is intended to be used as a single-conversion FSK/OOK receiver. It consists of a low noise amplifier, mixer, limiter, FM/FSK demodulator with an external LC tank circuit or ceramic resonator, LPF amplifier, and a data slicer with clock recovery and an integrated data bit synchronizer. The received strength signal indicator (RSSI) can also be used for fast carrier sense on/off keying, or amplitude shift keying, (OOK/ASK) demodulator.

baseband interface

The TRF6903 can easily be interfaced to a baseband processor such as the Texas Instruments MSP430 ultralow-power microcontroller (see Figure 1). The TRF6903 serial control registers are programmed by the MSP430 and the MSP430 performs baseband operations in the software.

A synchronized data clock, programmable for most common data rates, is provided by the TRF6903. This feature reduces the need for extensive oversampling and data decision in the microcontroller during receive. During transmit, the data clock can be used to clock the transmit data from the microcontroller to the TRF6903 at predefined data rates.

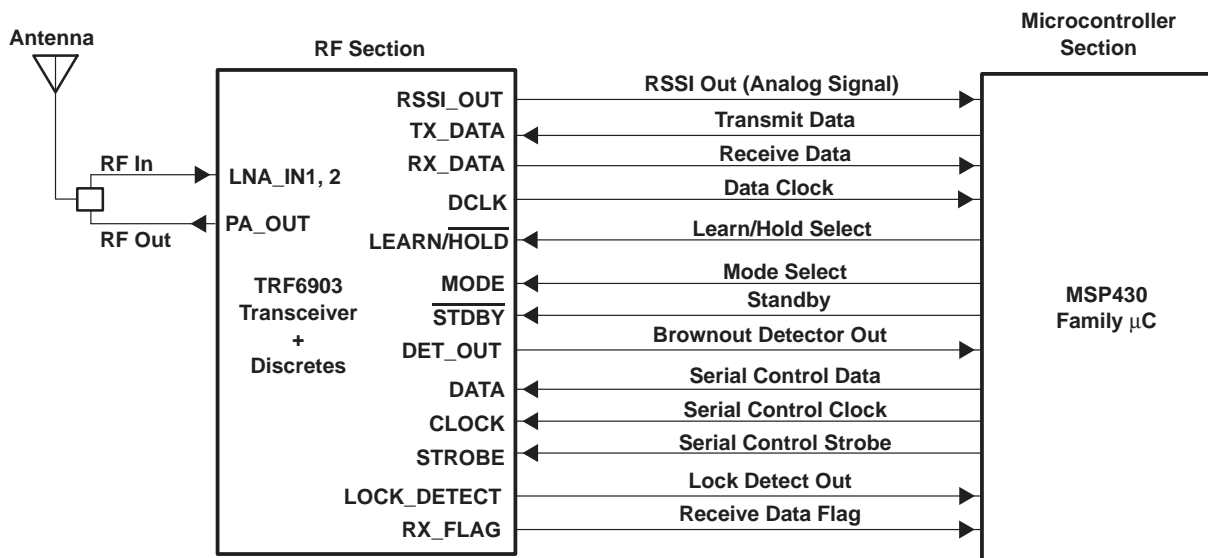
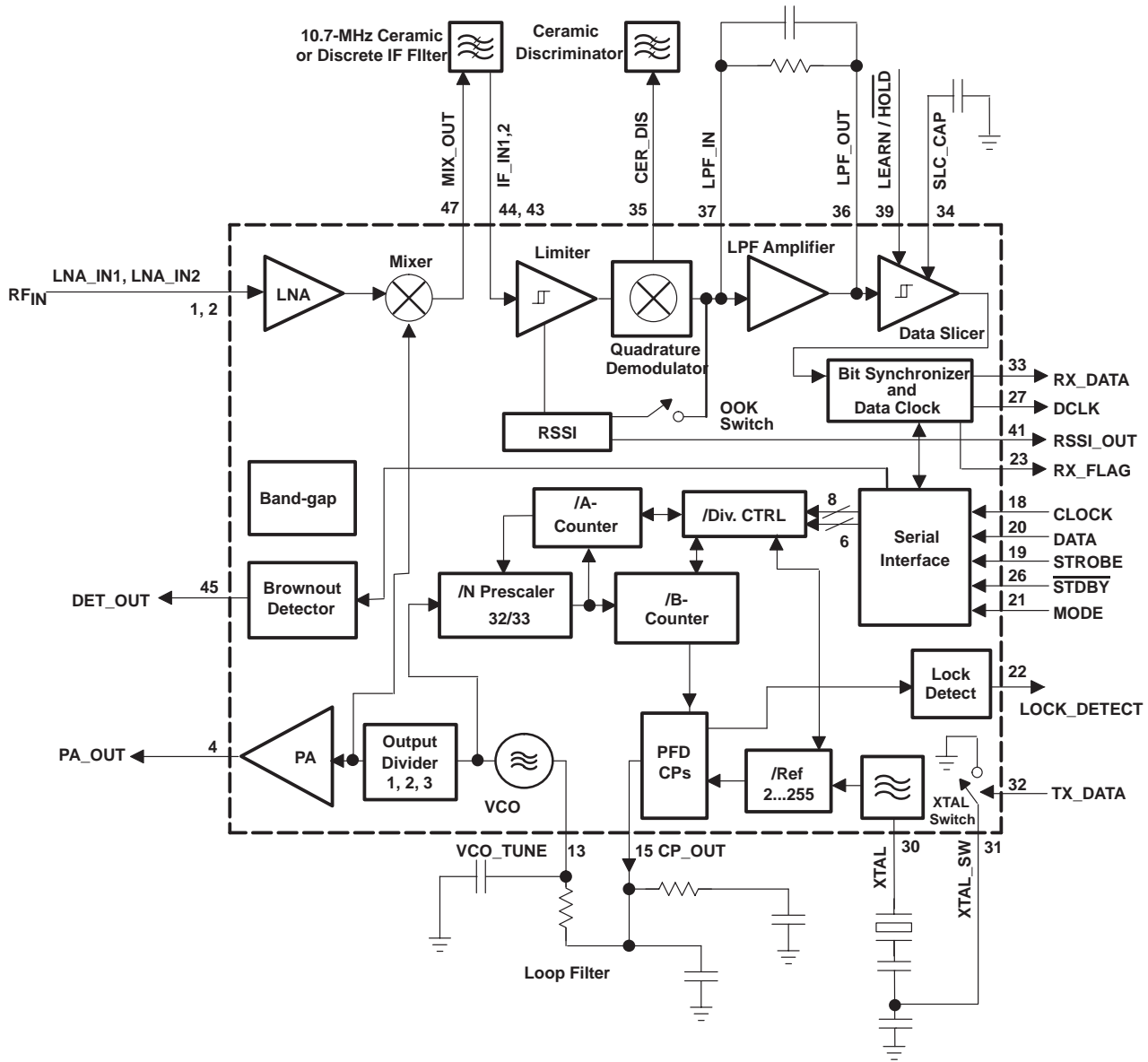


Figure 1. System Block Diagram for Interfacing to the MSP430 Microcontroller

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functional block diagram



Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|---------------|-----|-----|---|
| CER_DIS | 35 | | Connect to external ceramic discriminator |
| CLOCK | 18 | I | Serial interface clock signal input |
| CP_GND | 14 | | Charge pump ground |
| CP_OUT | 15 | O | Charge pump output |
| CP_VCC | 16 | | Charge pump supply voltage |
| DATA | 20 | I | Serial interface data signal input |



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Terminal Functions (Continued)

| TERMINAL | | I/O | DESCRIPTION |
|-------------|--------|-----|--|
| NAME | NO. | | |
| DCLK | 27 | O | Data clock output |
| DEM_GND | 38 | | Demodulator ground |
| DEM_VCC | 40 | | Demodulator supply voltage |
| DET_OUT | 45 | O | Brownout detector output; active high |
| DGND | 28 | | Digital ground |
| DVDD | 17 | | Digital power supply |
| GND | 42 | | Substrate ground |
| IF_IN1 | 44 | I | Limiter amplifier noninverting input |
| IF_IN2 | 43 | I | Limiter amplifier inverting input |
| LEARN/HOLD | 39 | I | Data slicer switch. Controls data slicer reference level |
| LNA_IN1 | 1 | I | LNA noninverting input |
| LNA_IN2 | 2 | I | LNA inverting input |
| LNA_VCC | 3 | | LNA power supply |
| LOCK_DETECT | 22 | O | PLL lock detect signal, active high |
| LPF_IN | 37 | I | Low-pass filter amplifier input |
| LPF_OUT | 36 | O | Low-pass filter amplifier output |
| MIX_GND | 46 | | Mixer ground |
| MIX_OUT | 47 | O | Mixer output |
| MIX_VCC | 48 | | Mixer supply voltage |
| MODE | 21 | I | Mode select input |
| NC | 24, 25 | | No connect |
| PA_GND1 | 5 | | Power amplifier ground |
| PA_GND2 | 7 | | Power amplifier ground |
| PA_OUT | 4 | O | Power amplifier output |
| PA_VCC | 6 | | Power amplifier supply voltage |
| RSSI_OUT | 41 | O | RSSI output signal |
| RX_DATA | 33 | O | Demodulated digital (FSK or OOK) RX data |
| RX_FLAG | 23 | O | Receive data flag |
| SLC_CAP | 34 | I/O | External capacitor for data slicer |
| STDBY | 26 | I | Standby input signal; active low |
| STROBE | 19 | I | Serial interface strobe signal |
| TX_DATA | 32 | I | Buffered TX data input |
| VCO_BYPASS | 11 | I | VCO bypass; connect to ground through a 100-pF capacitor |
| VCO_GND1 | 8 | | VCO ground |
| VCO_GND2 | 12 | | VCO ground |
| VCO_TUNE | 13 | I | Tuning voltage for the integrated VCO |
| VCO_VCC | 9 | | VCO supply voltage |
| VCO_VCC2 | 10 | | VCO core supply voltage |
| XTAL | 30 | I/O | Connection to an external crystal reference |
| XTAL_SW | 31 | I | Connecting to external capacitor, which sets the frequency deviation of the transmitted signal |
| XTAL_VCC | 29 | | Oscillator supply voltage |



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|--|-----------------|
| Supply voltage range | –0.6 to 4.5 Vdc |
| Input voltage, logic signals | –0.6 to 4.5 Vdc |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| ESD protection, human body model (HBM) | 2 kV |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|-----------------|-----|-----|-----|------|
| Analog supply voltage | | 2.2 | | 3.6 | V |
| Digital supply voltage | | 2.2 | | 3.6 | V |
| Operating free-air temperature | | –40 | | 85 | °C |

dc electrical characteristics, $V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$

supply current

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----|-----|-----|---------------|
| Standby current | STDBY low | | 0.6 | 4 | μA |
| RX current, receive chain inactive. Bit synchronizer and data clock inactive. PLL, VCO, dividers, and reference active | 315-MHz band | | 12 | 15 | mA |
| | 433-MHz band | | 11 | 14 | |
| | 868-MHz band | | 10 | 12 | |
| | 915-MHz band | | 10 | 12 | |
| RX current, receive chain active. PLL, VCO, dividers, and reference active. Bit synchronizer and data clock inactive | 315-MHz band | | 20 | 26 | mA |
| | 433-MHz band | | 19 | 25 | |
| | 868-MHz band | | 18 | 23 | |
| | 915-MHz band | | 18 | 23 | |
| RX current, receive chain active. PLL, VCO, dividers, and reference active. Bit synchronizer and data clock active | 315-MHz band | | 20 | 26 | mA |
| | 433-MHz band | | 19 | 25 | |
| | 868-MHz band | | 18 | 23 | |
| | 915-MHz band | | 18 | 23 | |



dc electrical characteristics, $V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$ (continued)

supply current (continued)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------|-----------------|-----|-----|-----|------|
| TX current, PA disabled. PLL, VCO, dividers, and reference active | | 315-MHz band | | 12 | 15 | mA |
| | | 433-MHz band | | 11 | 14 | |
| | | 868-MHz band | | 10 | 12 | |
| | | 915-MHz band | | 10 | 12 | |
| TX current [‡] , PA enabled. PLL, VCO, dividers, reference, and data clock active | 0-dB attenuation | 315-MHz band | | 37 | 43 | mA |
| | 10-dB attenuation | 315-MHz band | | 30 | | |
| | 20-dB attenuation | 315-MHz band | | 29 | | |
| | 0-dB attenuation | 433-MHz band | | 36 | 42 | |
| | 10-dB attenuation | 433-MHz band | | 29 | | |
| | 20-dB attenuation | 433-MHz band | | 28 | | |
| | 0-dB attenuation | 868-MHz band | | 35 | 40 | |
| | 10-dB attenuation | 868-MHz band | | 28 | | |
| | 20-dB attenuation | 868-MHz band | | 27 | | |
| | 0-dB attenuation | 915-MHz band | | 35 | 40 | |
| | 10-dB attenuation | 915-MHz band | | 28 | | |
| | 20-dB attenuation | 915-MHz band | | 27 | | |

[‡] The TX current consumption is dependent upon the external PA matching circuit. The matching network is normally designed to achieve the highest output power at the 0-dB attenuation setting. Changing the external matching components to optimize the output power for other attenuation settings alters the typical current consumption from the typical values noted.

digital interface

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---------------------------|--------------------------|--------------|-------|----------|---------------|
| V_{IH} | High-level input voltage | | $V_{DD}-0.4$ | | V_{DD} | V |
| V_{IL} | Low-level input voltage | | 0 | | 0.4 | V |
| V_{OH} | High-level output voltage | $I_{OH} = 0.5\text{ mA}$ | $V_{DD}-0.4$ | | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 0.5\text{ mA}$ | | | 0.4 | V |
| Digital input leakage current | | | | <0.01 | | μA |

ac electrical characteristics, $V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$

receiver (LNA, mixer, limiter, demod, LPF amplifier, data slicer, VCO, and PLL)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|--|-----|-----------|-----|------|
| RX wake-up time | | | | | 1 | ms |
| BER, FSK | | 315 MHz, 433 MHz, 868 MHz, 915 MHz, IF = 10.7 MHz, BW = 280 kHz FSK deviation: $\pm 32\text{ kHz}$ Bit rate: 19.2 kbit/s Manchester [†] $-103 < P_{RFIN}\text{ (dBm)} < -30$ | | 10^{-3} | | |
| BER, OOK | | 315 MHz, 433 MHz, 868 MHz, 915 MHz, IF = 10.7 MHz, BW = 280 kHz ON-OFF ratio: 50 dB Bit rate: 9.6 kbit/s Manchester [‡] $-103 < P_{RFIN}\text{ (dBm)} < -30$ | | 10^{-3} | | |

[†] 19.2 kbit/s Manchester is equivalent to 38.4 kbit/s NRZ.

[‡] 9.6 kbit/s Manchester is equivalent to 19.2 kbit/s NRZ.

TRF6903 SINGLE-CHIP MULTIBAND RF TRANSCEIVER

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ac electrical characteristics, $V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$

LNA/mixer, 304–316 MHz

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------------------------------|-----|-----|-----|------|
| Frequency range | | 304 | 315 | 316 | dB |
| Conversion gain | | | 21 | | dB |
| SSB noise figure | Includes external matching network | | 6.5 | | dB |
| Input 1-dB compression point | | | -31 | | dBm |
| Input IP3 | | | -21 | | dBm |

LNA/mixer, 430–450 MHz

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------------------------------|-----|-----|-----|------|
| Frequency range | | 430 | 433 | 450 | MHz |
| Conversion gain | | | 21 | | dB |
| SSB noise figure | Includes external matching network | | 6.5 | | dB |
| Input 1-dB compression point | | | -31 | | dBm |
| Input IP3 | | | -21 | | dBm |

LNA/mixer, 868–870 MHz

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------------------------------|-----|-----|-----|------|
| Frequency range | | 868 | 869 | 870 | MHz |
| Conversion gain | | | 19 | | dB |
| SSB noise figure | Includes external matching network | | 6.5 | | dB |
| Input 1-dB compression point | | | -31 | | dBm |
| Input IP3 | | | -20 | | dBm |

LNA/mixer, 902–928 MHz

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------------------------------|-----|-----|-----|------|
| Frequency range | | 902 | 915 | 928 | MHz |
| Conversion gain | | | 18 | | dB |
| SSB noise figure | Includes external matching network | | 6.5 | | dB |
| Input 1-dB compression point | | | -31 | | dBm |
| Input IP3 | | | -19 | | dBm |

IF/limiter amplifier

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|-------------------------|-----|------|-----|------|
| Frequency | | | 10.7 | | MHz |
| Voltage gain | | | 86 | | dB |
| Noise figure | IF frequency = 10.7 MHz | | 4 | | dB |

VCO/output divider

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|----------------------------------|-----|--------------------|-----|--------|
| Frequency range: 315-MHz band | Low-side injection, A<1:0> = 11 | 304 | 315 | 316 | MHz |
| Frequency range: 433-MHz band | High-side injection, A<1:0> = 10 | 430 | 433 | 450 | MHz |
| Frequency range: 868-MHz band | High-side injection, A<1:0> = 01 | 868 | 869 | 870 | MHz |
| Frequency range: 915-MHz band | Low-side injection, A<1:0> = 01 | 902 | 915 | 928 | MHz |
| Closed loop phase noise | Frequency offset = 50 kHz | | -77 | | dBc/Hz |
| | Frequency offset = 200 kHz | | -90 | | |
| Tuning voltage | | 0.1 | VCC at terminal 10 | | V |



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ac electrical characteristics, $V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$ (continued)

RSSI

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|-----|-----|-----|---------------|
| Dynamic range | | | 70 | | dB |
| Rise time | $R_L = 100\text{ k}\Omega$, $C_L = 10\text{ pF}$ | | 2 | 4 | μs |
| Slope | | | 20 | | mV/dB |
| RSSI output current | $R_L = 100\text{ k}\Omega$, $C_L = 10\text{ pF}$ | | 30 | | μA |

impedances and loads

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-----------------|---------------|------|-----|----------|
| LNA_IN | | See Figure 4 | | | |
| MIX_OUT† | | | 1400 | | Ω |
| IF_IN† | Differential | | 2600 | | Ω |
| PA_OUT | | See Figure 10 | | | |

† Does not include external matching network.

transmitter (XTAL, PLL, VCO, and PA), 315-MHz band

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|----------------------|-----|----------|-----|--------|
| TX frequency range | $A<1:0> = 11$ | 304 | 315 | 316 | MHz |
| Output power† | 0-dB attenuation | | 8 | | dBm |
| | 10-dB attenuation | | -2 | | |
| | 20-dB attenuation | | -12 | | |
| | Disabled, $B<3> = 0$ | | -80 | | |
| | Off‡ | | -80 | | |
| Second harmonic | | | -25 | | dBc |
| Third harmonic | | | -30 | | dBc |
| Frequency deviation§ | FSK | | ± 32 | | kHz |
| Power ON-OFF ratio | OOK, 0-dB mode | | 75 | | dB |
| Maximum data rate (NRZ) | FSK | | 64 | | kbit/s |
| | OOK | | 32 | | |

† Matched to $50\ \Omega$ using external matching network.

‡ Not selectable with PA attenuation bits $A<7:6>$, $B<7:6>$, or with $B<3>$. Measured while the TRF6903 device is in RX mode.

§ Dependent upon external circuitry.



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ac electrical characteristics, $V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$ (continued)

transmitter (XTAL, PLL, VCO, and PA), 433-MHz band

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--------------------|-----|-----|-----|--------|
| TX frequency range | A<1:0> = 10 | 430 | 433 | 450 | MHz |
| Output power† | 0-dB attenuation | | 8 | | dBm |
| | 10-dB attenuation | | -2 | | |
| | 20-dB attenuation | | -12 | | |
| | Disabled, B<3> = 0 | | -80 | | |
| | Off‡ | | -80 | | |
| Second harmonic | | | -25 | | dBc |
| Third harmonic | | | -30 | | dBc |
| Frequency deviation§ | FSK | | ±32 | | kHz |
| Power ON-OFF ratio | OOK, 0-dB mode | | 75 | | dB |
| Maximum data rate (NRZ) | FSK | | 64 | | kbit/s |
| | OOK | | 32 | | |

† Matched to 50 Ω using external matching network.

‡ Not selectable with PA attenuation bits A<7:6>, B<7:6>, or with B<3>. Measured while the TRF6903 device is in RX mode.

§ Dependent upon external circuitry.

transmitter (XTAL, PLL, VCO, and PA), 868-MHz band

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--------------------|-----|-----|-----|--------|
| TX frequency range | A<1:0> = 11 | 868 | 869 | 870 | MHz |
| Output power† | 0-dB attenuation | | 8 | | dBm |
| | 10-dB attenuation | | -2 | | |
| | 20-dB attenuation | | -12 | | |
| | Disabled, B<3> = 0 | | -80 | | |
| | Off‡ | | -80 | | |
| Second harmonic | | | -25 | | dBc |
| Third harmonic | | | -30 | | dBc |
| Frequency deviation§ | FSK | | ±32 | | kHz |
| Power ON-OFF ratio | OOK, 0-dB mode | | 75 | | dB |
| Maximum data rate (NRZ) | FSK | | 64 | | kbit/s |
| | OOK | | 32 | | |

† Matched to 50 Ω using external matching network.

‡ Not selectable with PA attenuation bits A<7:6>, B<7:6>, or with B<3>. Measured while the TRF6903 device is in RX mode.

§ Dependent upon external circuitry.



ac electrical characteristics, $V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$ (continued)

transmitter (XTAL, PLL, VCO, and PA), 915-MHz band

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--------------------|-----|-----|-----|--------|
| TX frequency range | A<1:0> = 11 | 902 | 915 | 928 | MHz |
| Output power† | 0-dB attenuation | | 8 | | dBm |
| | 10-dB attenuation | | -2 | | |
| | 20-dB attenuation | | -12 | | |
| | Disabled, B<3> = 0 | | -80 | | |
| | Off‡ | | -80 | | |
| Second harmonic | | | -25 | | dBc |
| Third harmonic | | | -30 | | dBc |
| Frequency deviation§ | FSK | | ±32 | | kHz |
| Power ON-OFF ratio | OOK, 0-dB mode | | 75 | | dB |
| Maximum data rate (NRZ) | FSK | | 64 | | kbit/s |
| | OOK | | 32 | | |

† Matched to 50 Ω using external matching network.

‡ Not selectable with PA attenuation bits A<7:6>, B<7:6>, or with B<3>. Measured while the TRF6903 device is in RX mode.

§ Dependent upon external circuitry.

XTAL

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|-----------------|-----|-----|-----|------|
| Frequency range | | 9.5 | | 20 | MHz |

brownout detector

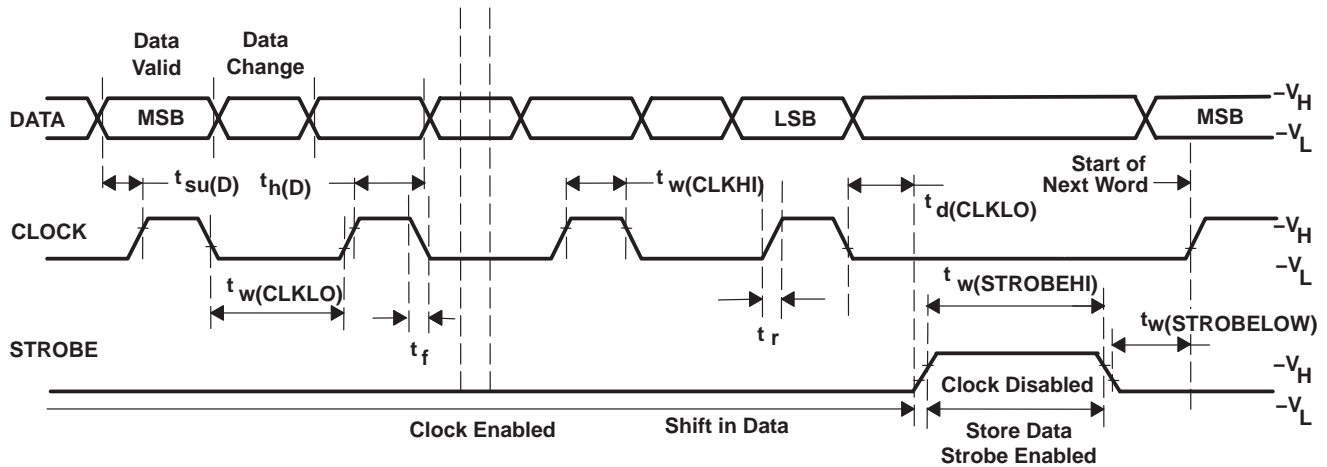
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|-----|------|-----|------|
| Voltage threshold, V_{det} | Set by B<2:1> | 2.2 | | 2.8 | V |
| Voltage steps (ΔV) | | | 200 | | mV |
| Number of steps | | | 4 | | |
| Output level | Connected to typical input port of microcontroller | | CMOS | | |

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timing data for serial interface

| PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------------|--|-----|-----|-----|------|
| $f(\text{CLOCK})$ | Clock frequency | | | 20 | MHz |
| $t_w(\text{CLKHI})$ | Clock high-time pulse width, clock high | | 20 | | ns |
| $t_w(\text{CLKLO})$ | Clock low-time pulse width, clock low | | 20 | | ns |
| $t_{su}(\text{D})$ | Setup time, data valid before CLOCK \uparrow | | 0 | | ns |
| $t_h(\text{D})$ | Hold time, data valid after CLOCK \uparrow | | 10 | | ns |
| $t_d(\text{CLKLO})$ | Delay time of CLOCK low before STROBE high | | 20 | | ns |
| $t_w(\text{STROBEHI})$ | STROBE high-time pulse width, STROBE high | | 20 | | ns |
| $t_w(\text{STROBELO})$ | STROBE low-time pulse width, STROBE low | | 20 | | ns |



Note: Most significant bit (MSB) clocked in first to the synthesizer.

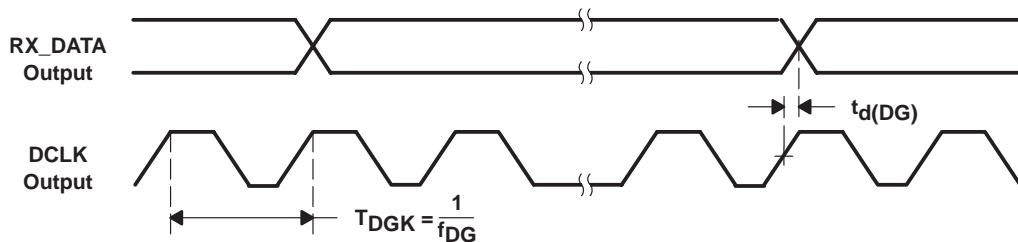
Figure 2. Timing Data for Serial Interface

timing data for DCLK, TX_DATA, RX_FLAG, and RX_DATA

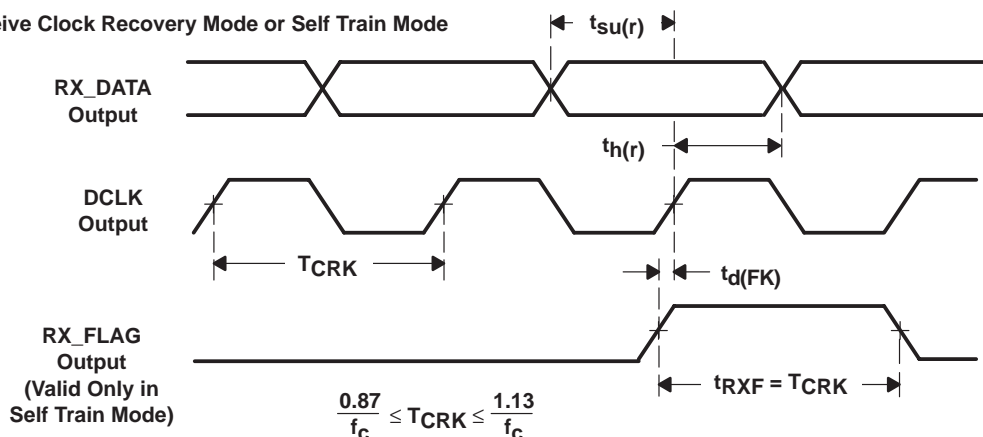
| PARAMETER | | MIN | TYP | MAX | UNIT |
|--------------|---|-------------------|-----|-----|------|
| $t_{d(DG)}$ | Delay time, rising edge of DCLK to transition of RX_DATA | | 3 | | ns |
| $t_{su(r)}$ | Setup time, RX_DATA valid before DCLK \uparrow | $0.4/f_c^\dagger$ | | | |
| $t_{h(r)}$ | Hold time, RX_DATA valid after DCLK \uparrow | $0.4/f_c^\dagger$ | | | |
| $t_{d(FK)}$ | Delay time, rising edge of RX_FLAG before DCLK \uparrow | | 2 | | ns |
| $t_{su(TX)}$ | Setup time, TX_DATA valid before DCLK \uparrow | 100 | | | ns |
| $t_{h(TX)}$ | Hold time, TX_DATA valid after DCLK \uparrow | 100 | | | ns |

\dagger After clock recovered

Receive Deglitch Mode

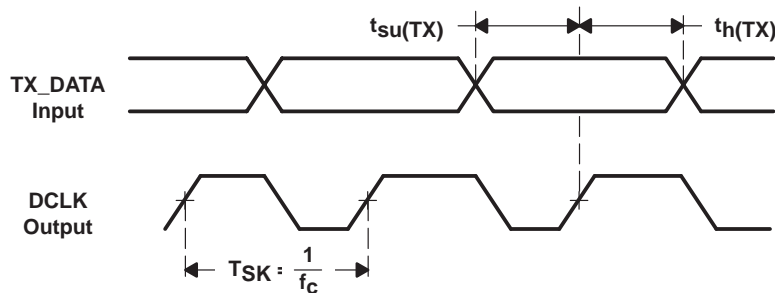


Receive Clock Recovery Mode or Self Train Mode



NOTE: RX_DATA is latched at the falling edge of DCLK.

Transmit



NOTE: TX_DATA is latched at the rising edge of DCLK.

Figure 3. Timing Data for DCLK, TX_DATA, RX_FLAG, and RX_DATA

It can be seen from the timing diagram that in the clock recovery or self train mode, the data transitions (high-to-low or low-to-high) on the RXDATA pin are timed to coincide with the falling edge of DCLK. Any microcontroller using the TRF6903 can then latch RXDATA on the rising edge of DCLK. For more details, see the *data clock* section.

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timing data for DCLK, TX_DATA, RX_FLAG, and RX_DATA (continued)

In high data rate systems (> 38K bps), designers need to be aware of the latency between the rising edge of DCLK and the time the RXDATA logic value is sampled by the microcontroller. This latency needs to be less than half the RXDATA pulse width to prevent bit errors.

If transmit capture mode is selected (by setting bit 13 in word E), the data transitions (high-to-low or low-to-high) on the TXDATA pin are timed to coincide with the falling edge of DCLK. Any microcontroller using the TRF6903 can then latch TXDATA on the rising edge of DCLK. For more details, see the *data clock* section.

low-noise amplifier (LNA)/RF mixer

The LNA has differential inputs. The off-chip input matching network has the dual task of matching a 50-Ω connector (or antenna, switch, filter, etc.) to the differential inputs and providing a 180-degree phase shift between the inputs at terminals 1 and 2. The differential input impedance of the LNA is approximately 500 Ω in parallel with 0.7 pF. The predicted noise figure of the LNA and input matching circuit is 2.5 dB. The cascaded noise figure for the LNA/mixer is listed in the specifications.

The mixer offers good linearity (high IP3). An external matching network is required to transform the output impedance of the mixer (1.4 kΩ) to the input impedance of the IF filter (typically 330 Ω).

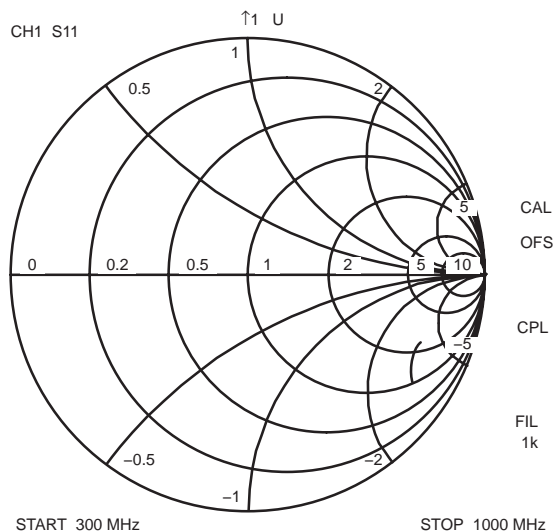


Figure 4. Typical LNA Input Impedance (S11) at Device Terminals LNA_IN1,2

IF amplifier/limiter

The IF amplifier has differential inputs to its first stage. The limiting amplifier provides 68 dB of gain. An external impedance matching network is required between the IF filter output at terminal 47 and the IF amplifier inputs at terminals 43 and 44.

RSSI

The received signal strength indicator (RSSI) voltage at terminal 41 is proportional to the log of the down-converted RF signal at the IF limiting amplifier input. The RSSI circuit is temperature compensated. It is useful for detecting interfering signals, transceiver handshaking, and RF channel selection. In some applications, the RSSI circuitry alone can be used as a demodulator for amplitude-shift keying (ASK) or on-off keying (OOK) modulation with an output at the RSSI_OUT terminal. In OOK mode, the received signal is also fed from the RSSI circuitry to the input of the post-detection LPF amplifier. In this mode, received data is output at the RX_DATA terminal according to the RXM field.

demodulator

The quadrature demodulator decodes digital frequency shift keying (FSK) modulation. An external ceramic discriminator or an equivalent discrete circuit is required at terminal 35. The demodulator is optimized for use with a ceramic discriminator. Thus, the use of a packaged ceramic discriminator is recommended for best performance. Internal resistors can be programmed with D<14:12> to tune the demodulator center frequency. The recommended default setting for the demodulator tuning bits is D<14:12> = 110. The resonant frequency of the discrete-component discriminator can be calculated from the inductor and capacitor values used in the circuit. A parallel resistor may be added to reduce the quality factor (Q) of the tank circuit, depending on the application.

When OOK modulation is selected, the received signal from the RSSI circuitry is connected directly to the post-detection LPF amplifier, therefore bypassing the quadrature demodulator.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

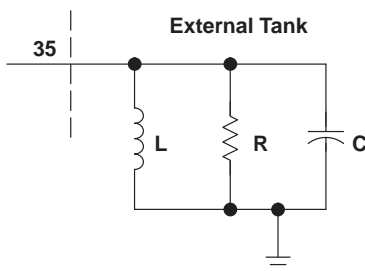


Figure 5. Optional External Discrete Demodulator Tank

post-detection amplifier/low-pass filter

The post-detection amplifier operates as a low-pass transimpedance amplifier. The external low-pass filter circuit must be optimized for the data rate. The 3-dB corner frequency of the low-pass filter should be greater than twice the data rate. Various low-pass filter designs use two to five components and may be first- or second-order designs. Simple 2-element filter component values and 3-dB bandwidths are contained in Table 1.

$$f_{3dB} = \frac{1}{2\pi R2(C2 + C1)}$$

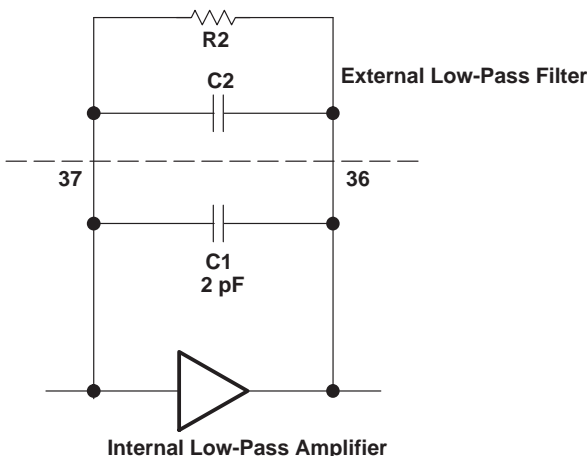


Figure 6. Post-Detection Amplifier/Low-Pass Filter

post-detection amplifier/low-pass filter (continued)

Table 1. Various Post-Detection Amplifier/Low-Pass Filter 3-dB Bandwidth and Corresponding Component Values for FSK Operation

| f _{3dB} (kHz) | 10 | 20 | 30 | 60 |
|------------------------|-----|-----|-----|-----|
| R2 (kΩ) | 220 | 220 | 220 | 220 |
| C2 (pF) | 68 | 33 | 22 | 10 |

NOTE: For OOK operation, it is recommended that R2 be set to 27 kΩ and C2 is not placed.

data slicer and bit synchronizer

The data slicer is a comparator circuit for received digital (FSK and OOK) data. The data slicer output voltage depends on the difference between the received signal and a reference voltage (at the sample-and-hold (S&H) capacitor) used as a decision threshold. During the learn mode, the S&H capacitor connected to terminal 34 is charged up to the average dc voltage of a training sequence of alternating ones and zeroes; this establishes the reference voltage to be used as a decision level before a sequence of actual data is received in the hold mode. During long data transmissions, more training sequences may be necessary to recharge the S&H capacitor.

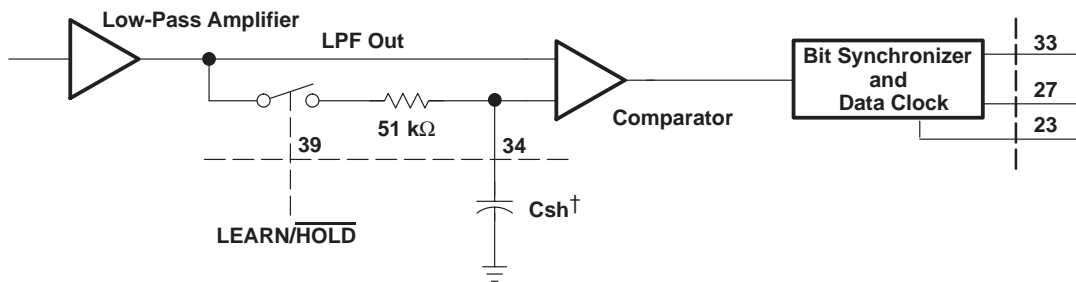
If the modulation scheme is dc-free (Manchester coding) or constant-dc, the TRF6903 may be operated continuously in the learn mode and no training sequence is necessary before the transmission of a data string. However, the S&H capacitor voltage may be incorrect during power up or after long periods of inactivity (no data transmission); a learning sequence before each data transmission is recommended.

The comparator is a CMOS circuit that does not load the S&H capacitor. Leaving the transmission gate (LEARN/HOLD switch) open (in hold mode) during periods of inactivity, such as during standby, may be useful in maintaining the capacitor reference voltage. However, the reference voltage gradually discharges over time due to leakage current.

The time constant for charging the S&H capacitor is determined by its capacitance and an internal 51-kΩ resistor. A slow data rate requires a larger S&H capacitor (longer time constant). The value of the S&H capacitor, C_{sh}, can be calculated with the following equation:

$$S \ \& \ H \ Cap = \frac{\text{Number of training Bits}}{5 \times 51k \times \text{Data Rate (Hz)}} ; \text{Farad}$$

Where the data rate in Hz is the fundamental frequency (in Hz) of the base band waveform.



†External Sample-and-Hold Capacitor

Figure 7. Data Slicer and Bit Synchronizer

The received data and data clock output modes are determined by field RXM according to Table 3. When RXM, E<15:14> is set to 00, the raw data from the data slicer is output at terminal 33, RX_DATA. No synchronization or data recovery is performed and the receiver can be used in an asynchronous mode. When RXM, E<15:14>, is set to 01, received data is first passed through a deglitching filter. These modes are useful for the reception of data whose baud rate is nonstandard.

data slicer and bit synchronizer (continued)

When RXM is set to enable recovered data, RXM E<15:14> = 10 or 11, the integrated bit synchronizer determines the preprogrammed data rate as determined by the crystal frequency and the values of D1, D2, and D3, and performs data recovery. Glitch-free, recovered data is then output at terminal 33, RX_DATA, and the corresponding data clock is output at terminal 27, DCLK.

The preprogrammed bit rate can be calculated based on the following equation:

$$\text{Bit rate (kbps)} = \frac{\text{crystal frequency (kHz)}}{D1 \times D2 \times D3} = \frac{F_x}{D1 \times D2 \times D3} = f_c \text{ (kHz)}$$

where

- D1 = 1, 5, 6, or 8
- D2 = 1, 2, 4, 8, 16, 32, 64, or 128
- D3 = 15 or 16

data clock

When enabled, RXM = 10 or 11, the data clock circuitry provides as an output at terminal 27, DCLK, a data clock based on a programmable bit rate. The bit rate is programmable via variables D1, D2, and D3 and is always relative to the master clock (XTAL) frequency, F_x. Table 2 shows common bit rates (kbps) vs selected crystal frequencies (MHz) and the respective settings of D1, D2, and D3.

Table 2. Common Bit Rates, Corresponding Crystal Frequencies, and Values of D1, D2, and D3

| BIT RATE (kbps) | D1, D2, AND D3 MULTIPLIERS FOR COMMON CRYSTAL VALUES (CRYSTAL FREQUENCIES IN MHZ) | | | | | |
|--------------------|---|----------|----------|----------|----------|----------|
| | 9.8304 | 12.288 | 14.7456 | 15.72864 | 16.384 | 19.6608 |
| 0.6 | 8x128x16 | | | | | |
| 0.9 | | | 8x128x16 | | | |
| 1 | | 6x128x16 | | | 8x128x16 | |
| 1.024 | 5x128x15 | | | 8x128x15 | | |
| 1.2 | 8x64x16 | 5x128x16 | 6x128x16 | | | 8x128x16 |
| 1.8 | | | 8x64x16 | | | |
| 2 | | 6x64x16 | | | 8x64x16 | |
| 2.048 | 5x64x15 | | | 8x64x15 | | 5x128x15 |
| 2.4 | 8x32x16 | 5x64x16 | 6x64x16 | | | 8x64x16 |
| 3.6 | | | 8x32x16 | | | |
| 4 | | 6x32x16 | | | 8x32x16 | |
| 4.096 | 5x32x15 | | | 8x32x15 | | 5x64x15 |
| 4.8 | 8x16x16 | 5x32x16 | 6x32x16 | | | 8x32x16 |
| 7.2 | | | 8x16x16 | | | |
| 8 | | 6x16x16 | | | 8x16x16 | |
| 8.192 | 5x16x15 | | | 8x16x15 | | 5x32x15 |
| 9.6 | 8x8x16 | 5x16x16 | 6x16x16 | | | 8x16x16 |
| 14.4 | | | 8x8x16 | | | |
| 16 | | 6x8x16 | | | 8x8x16 | |
| 16.384 | 5x8x15 | | | 8x8x15 | | 5x16x15 |
| 19.2 | 8x4x16 | 5x8x16 | 6x8x16 | | | 8x8x16 |
| 28.8 | | | 8x4x16 | | | |
| 32 | | 6x4x16 | | | 8x4x16 | |
| 32.768 | 5x4x15 | | | 8x4x15 | | 5x8x15 |
| 38.4 | 8x2x16 | 5x4x16 | 6x4 x16 | | | 8x4x16 |
| 57.6 | | | 8x2x16 | | | |
| 64 | | 6x2x16 | | | 8x2x16 | |
| 65.536 | 5x2x15 | | | 8x2x15 | | 5x4x15 |



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data clock (continued)

Table 2. Common Bit Rates, Corresponding Crystal Frequencies, and Values of D1, D2, and D3 (continued)

| BIT RATE (kbps) | D1, D2, AND D3 MULTIPLIERS FOR COMMON CRYSTAL VALUES (CRYSTAL FREQUENCIES IN MHZ) | | | | | |
|--------------------|---|--------|---------|----------|--------|---------|
| | 9.8304 | 12.288 | 14.7456 | 15.72864 | 16.384 | 19.6608 |
| 76.8 | 8x1x16 | 5x2x16 | 6x2x16 | | | 8x2x16 |
| 115.2 | | | 8x1x16 | | | |
| 128 | | 6x1x16 | | | 8x1x16 | |

There are several receive modes, from raw slicer output to clock recovery and training sequence recognition. The receive logic is controlled by the RXM, TWO, and TCOUNT fields. The RXM, E<15:14>, field determines the receive mode as indicated in Table 3. These modes are described in more detail below.

Table 3. Clock Recovery and Receive Data Modes Selected by RXM

| RXM | RECEIVE MODE | RX_DATA | DCLK | RX_FLAG |
|-----|----------------|--|--|--|
| 00 | Raw data | Data direct from data slicer | Inactive; held low | Inactive; held low |
| 01 | Deglitch | Deglitched data | Active; clock synchronous to deglitched data | Inactive; held low |
| 10 | Clock recovery | Deglitched data; synchronous to bit-rate clock at DCLK | Active; synchronous bit-rate clock | Inactive; held low |
| 11 | Self train | Deglitched data; synchronous to bit-rate clock at DCLK | Active; synchronous bit-rate clock | Active; set high at first received bit that is not part of a predetermined training sequence |

In *Raw Data* mode, the data slicer output is fed directly to the RX_DATA terminal, and the DCLK and RX_FLAG terminals are held low.

In *Deglitch* mode, the data slicer output is passed through the internal deglitch filter. This filter samples the slicer output at a rate f_{DG} , where

$$f_{DG} = \frac{F_x}{D1 \times D2}$$

The filter output is high if five or more of the last seven samples were high, and low if two or less of the last seven samples were high. Otherwise, the filter holds its previous value. The deglitched data is applied to the RX_DATA terminal, and the over-sampled deglitch filter clock is passed on to the DCLK terminal. Data will appear on the RX_DATA terminal a few gate delays after the rising edge of DCLK. The RX_FLAG terminal is held low.

In *Clock Recovery* mode, the edges of the deglitched data are used to synchronize a bit-rate clock to the data. As long as the consecutive number of ones or zeros in the data stream, N_{CB} , meets the condition:

$$N_{CB} < \frac{250000}{\Delta_B} \quad \text{where } \Delta_B \text{ is the error between the transmit bit rate and the receiver bit-rate clock in ppm.}$$

The output data is synchronous with the bit-rate clock. The deglitched data is routed to the RX_DATA terminal and the synchronized bit-rate clock appears at DCLK. The RX_FLAG terminal is held low. The data transition is timed to coincide with the falling edge of DCLK, so that the external microcontroller using the TRF6903 can latch RX_DATA on the rising edge of DCLK with plenty of setup and hold margin. If no data edges have been observed since the last reset, then DCLK is held low until an edge is seen.

data clock (continued)

In *Self Train* mode, the TRF6903 receiver not only performs clock recovery, but also looks for the end of a training sequence. The TWO, E<12>, field determines the pattern of the training sequence. If TWO is low, the training sequence is assumed to be alternating ones and zeros; if TWO is high, the training sequence is assumed to be alternating pairs of ones and zeros. RX_DATA and DCLK output are the same as in *Clock Recovery* mode. However, if a minimum number of training bits have been observed, then the RX_FLAG terminal is asserted high for one clock period (after which it returns low) at the first bit that is not part of the training sequence. The timing of RX_FLAG is a few gate delays after the rising edge of DCLK. The minimum number of training bits is four times the unsigned binary value of TCOUNT, E<11:7>, plus two if TWO = 0 or plus three if TWO = 1, according to the equation:

$$TB_{\min} = (4 \times TCOUNT) + TWO + 2$$

The clock recovery and training sequence recognition circuits are all designed to reset/clear internally with no user action required.

When active, DCLK is synchronized to the received data. The rising edge of the data clock is intended to be located at the middle of the received recovered data bit, thus enhancing the synchronization ability of the microcontroller and reducing the need for extensive signal processing in the microcontroller.

main divider

The main divider is composed of a 5-bit A-counter and a 9-bit B-counter and a prescaler. The A-counter controls the divider ratio of the prescaler, which divides the VCO signal by either 33 or 32. The prescaler divides by 33 until the A-counter reaches its terminal count and then divides by 32 until the B-counter reaches terminal count, whereupon both counters reset and the cycle repeats. The total divide-by-N operation is related to the 32/33 prescaler by:

$$N_{\text{TOTAL}} = 33 \times A + 32 \times (B - A)$$

where $0 \leq A \leq 31$ and $31 \leq B \leq 511$ or, $N_{\text{TOTAL}} = A + 32B$

Thus, the N-divider has a range of $992 \leq N_{\text{TOTAL}} \leq 16383$

PLL

The phase-locked loop is the radio frequency synthesizer for the TRF6903. It is used to generate the transmit signal and as the local oscillator for the receive mixer. The signal (F_X) from a reference crystal oscillator (XO) is divided by an integer factor R down to F_R . The minimum frequency resolution, and thus, the minimum channel spacing, is F_R .

$$F_R = F_X \div R \text{ where } 1 \leq R \leq 256$$

The phase-locked loop is an integer-N design. The voltage-controlled oscillator (VCO) signal is divided by an integer factor N to get a frequency at the phase detector input.

$$F_{PD} = F_{VCO} \div N$$

The phase detector compares the divided VCO signal to the divided crystal frequency and implements an error signal from two charge pumps. The error signal corrects the VCO output to the desired frequency.

As is in any integer-N PLLs, the VCO output has spurs at integer multiples of the reference frequency (nF_R). In applications requiring contiguous frequency channels, the reference frequency is often chosen to be equal to the channel spacing, thus, channel spacing = $F_R = F_X \div R$. When the PLL is locked, the LOCK_DETECT terminal is high.

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PLL (continued)

With the addition of an output divider for multiband operation, the actual output frequency, F_{out} , is given by:

$$F_{out} = \frac{F_{VCO}}{P} = \frac{F_X}{R} \times \frac{N}{P} = F_R \times \frac{N}{P} = \frac{A + 32B}{P} \times F_R$$

where $F_R = F_{PD}$ under locked conditions. The actual minimum channel spacing is:

$$\frac{F_R}{P} = \frac{F_X \div R}{P}$$

where $P = 1, 2, 3$ and is set by $A<1:0>$.

oscillator circuit and reference divider

The reference divider reduces the frequency of the external crystal (F_X) by an 8-bit programmable integer divisor, R , to an internal reference frequency (F_R) used for the phase-locked loop. See Figure 8. The choice of internal reference frequency also has implications for lock time, maximum data rate, noise floor, and loop-filter design. The crystal frequency can be tuned using the F word to control internal trimming capacitors, which are placed in parallel with the crystal. These offset a small frequency error in the crystal. In an FSK application, an additional capacitor is placed in parallel (through terminal 31) with the external capacitor that is connected in series with the crystal, thus, changing the load capacitance as the transmit data switch (TX_DATA, terminal 32) is toggled. The change in load capacitance pulls the crystal off-frequency by the total frequency deviation.

Hence, the 2-FSK frequency, set by the level of TX_DATA and the external capacitor, can be represented as follows:

$$f_{out1} = \text{TX_DATA Low (XTAL switch closed)} \text{ and } f_{out2} = \text{TX_DATA High (XTAL switch open)}$$

Note that the frequencies f_{out1} and f_{out2} are centered about the frequency $f_{center} = (f_{out1} + f_{out2})/2$. When transmitting FSK, f_{center} is considered to be the effective carrier frequency and any receiver local oscillator (LO) should be set to the same f_{center} frequency \pm the receiver's IF frequency (f_{IF}) for proper reception and demodulation.

For the case of high-side injection, the receiver LO would be set to $f_{LO} = f_{center} + f_{IF}$. Using high-side injection, the received data at terminal 33, RX_DATA, would be inverted from the transmitted data applied at terminal 32, TX_DATA. Conversely, for low-side injection, the receiver LO would be set to $f_{LO} = f_{center} - f_{IF}$. Using low-side injection, the received data would be the same as the transmitted data. The data polarity invert bit PI, $A<4>$, can be used to invert the data at terminal 33, RX_DATA, when high-side injection is being used.

In addition, when the TRF6903 is placed in receive mode, it is recommended that the $D<19>$ bit be kept high to keep the XTAL switch closed. In this manner, the actual LO frequency injected into the mixer is $f_{out1} = f_{LO}$. If $D<19>$ is set low, the receiver LO would be offset, resulting in poor receiver sensitivity.

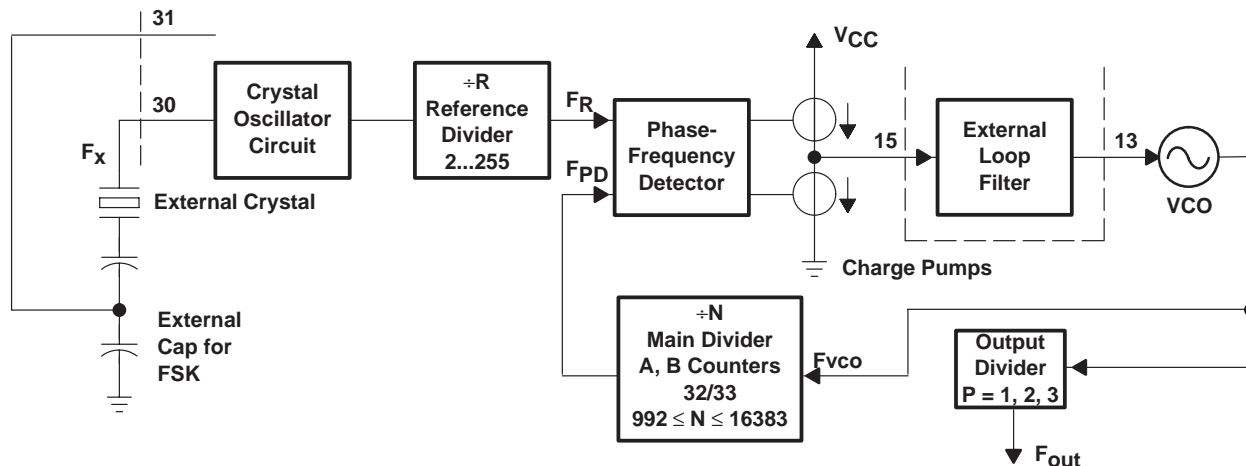


Figure 8. TRF6903 PLL and Output Divider

phase detector and charge pumps

The phase detector is a phase-frequency design. The phase-frequency detector gain is given by:

$$K_P = I_{CP}/2\pi$$

where, I_{CP} is the peak charge pump current. The peak charge pump current is programmable with A<3:2> in three steps: 250 μ A, 500 μ A, and 1000 μ A.

loop filter

The loop filter must be carefully chosen for proper operation of the TRF6903. The loop filter as shown in Figure 9 is typically a second- or third-order passive design and in FSK operation should have a bandwidth wide enough to allow the PLL to relock quickly as the external crystal frequency is pulled off-center during modulation. The loop filter should also be wider than the data modulation rate. These requirements should be balanced with making the loop narrow enough in consideration of the reference frequency. In OOK the VCO frequency is not changed during data modulation, so the filter bandwidth may be narrower than the modulation bandwidth. Filters can be calculated using standard formulas in reference literature. Some third-order filter examples are shown in Table 4.

$$F(s) = \frac{1 + sC2R2}{s(C1 + C2 + sC1C2R2)} \times \frac{1}{s + \frac{1}{C3R3}}$$

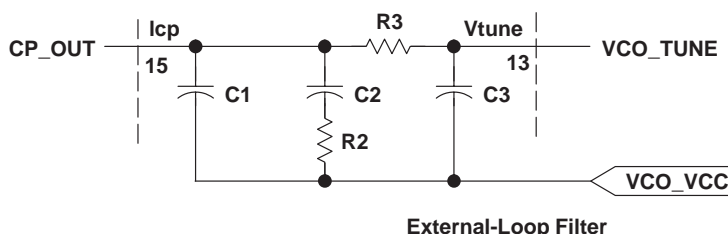


Figure 9. Third-Order Loop Filter and Transfer Function

Table 4. Loop Filter Component Values For Various Data Rates at a Reference Frequency of 409.6 kHz, 0.5-mA Charge Pump Current

| | | | | | | | | | |
|--|------------------------|-------|-------|-------|--------|--------|-------|--------|---------|
| Bit rate – kbps | Manchester coding | 1.024 | 2.048 | 4.096 | 8.192 | 16.384 | 19.2 | 32.768 | 65.536 |
| | NRZ coding | 2.048 | 4.096 | 8.192 | 16.384 | 32.768 | 38.4 | 65.536 | 131.072 |
| Data rate – kHz | Fundamental freq of BB | 1.024 | 2.048 | 4.096 | 8.192 | 16.384 | 19.2 | 32.768 | 65.536 |
| Loop filter component (selected to nearest standard value) | C1, nF | 47 | 12 | 2.7 | 0.68 | 0.18 | 0.12 | 0.043 | 0.01 |
| | C2, nF | 1800 | 430 | 100 | 27 | 6.8 | 5.1 | 1.8 | 0.47 |
| | C3, nF | 27 | 6.8 | 1.5 | 0.39 | 0.1 | 0.075 | 0.027 | 0.0068 |
| | R2, k Ω | 0.39 | 0.75 | 1.5 | 3 | 5.7 | 6.8 | 12 | 24 |
| | R3, k Ω | 0.75 | 1.5 | 3 | 5.7 | 12 | 15 | 22 | 47 |
| –3–dB bandwidth, kHz (approximate) | | 1.28 | 2.56 | 5.12 | 10.24 | 20.48 | 24 | 40.96 | 81.92 |

VCO

The voltage-controlled oscillator (VCO) produces an RF output signal with a frequency that is dependent upon the dc-tuning voltage at terminal 13. The tank circuit is passive and has integrated varactor diodes and inductors. The open-loop VCO gain is approximately 100 MHz/V.

A <1:0> is used to set the output divider ratio for operation within the 315-MHz, 433-MHz, 868-MHz, or 915-MHz bands.

When the \overline{STDBY} terminal is high, the reference, PLL, VCO, and dividers are powered up. When \overline{STDBY} is low, these blocks are powered down.

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power amplifier

The power amplifier has three programmable attenuation states as determined by A<7:6> and B<7:6>: full power (0-dB attenuation), 10-dB attenuation, and 20-dB attenuation. This adjustment feature allows the user to fine-tune the device for optimal output power. The power amplifier can be enabled/disabled during transmit by bit B<3>, PARXED. During receive, the transmit power amplifier is powered down but the VCO and PLL are still operating. During ASK or OOK operation, the TX_DATA signal turns the power amplifier on and off according to the transmit data incident at terminal 32.

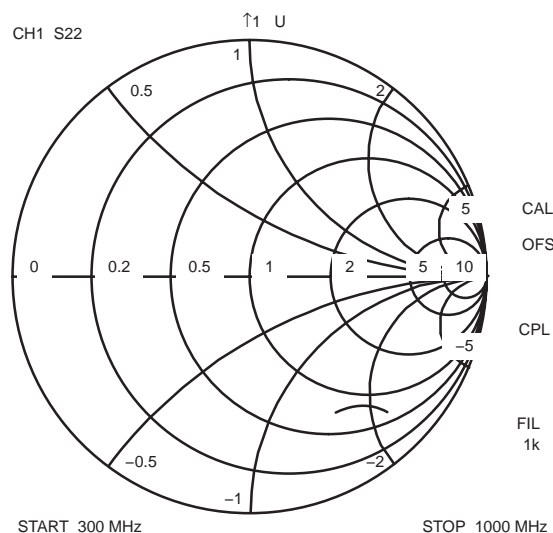


Figure 10. Typical PA Output Impedance (S22) at Device Terminal PA_OUT

brownout detector

The brownout detector provides an output voltage to indicate a low supply voltage. This may be used to signal the need to change transmit power to conserve battery life, or for system power down. The brownout detector threshold is set with the B word. Four different thresholds are available.

serial control interface

The TRF6903 is controlled through a serial interface; there are five 24-bit control words (A, B, C, D, E) which set the device state. The A and B words are almost identical, and provide configuration settings for two modes, designated 0 and 1, which are commonly used to configure the transmit and receive states. The transmit and receive states can then be rapidly selected using MODE (terminal 21). The C word sets the reference dividers, the power amplifier bias, and contains various reset bits. The E word contains the bit-rate select, data clock control bits, and the power amplifier bias control registers. The D word is used to trim the external crystal frequency and tune the demodulator.

The register address is the composite of bits 23, 22, 1, and 0 of the 24 bits written to the serial interface. For some words, certain bits of the address are don't cares and are noted as XX. This flexible addressing scheme allows backward compatibility with the TRF6901, and because of this flexibility, the data length of each register varies from 15 bits to 22 bits.

Normal (write) operation of the serial interface is to clock in 24 bits through the CLOCK and DATA terminals. DATA values are clocked into the 24-bit serial interface shift register on the rising edge of CLOCK. The 24-bit value is decoded and written into the appropriate data register on the rising edge of STROBE.

PRINCIPLES OF OPERATION

register description

| Word | Address | | | | | | | | | | | | | | | | | | | | Address | | |
|------|---------|----|-------------------------------------|-----|-----|-----------|-----------|-------------------------------------|--------|----------|----|----|----|----|-----|--------|---------|---------|--------------------|-------------|---------|---|---|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | | 3 | 2 |
| A | 0 | 0 | Main A-Divider Coefficient (Mode 0) | | | | | Main B-Divider Coefficient (Mode 0) | | | | | | | PA0 | TX/RX0 | PI | CP Acc. | | | BND | | |
| B | 0 | 1 | Main A-Divider Coefficient (Mode 1) | | | | | Main B-Divider Coefficient (Mode 1) | | | | | | | PA1 | TX/RX1 | FSK/OOK | PARXED | Detector Threshold | Det. Enable | | | |
| C | 1 | 0 | Reference Divider Coefficient | | | | | | | Reserved | | | | | | | r | r | r | r | r | 0 | 0 |
| E | 1 | 0 | BRA | BRB | BRC | RXM | TXM | TWO | TCOUNT | | | | | 0 | 0 | r | r | r | 0 | 1 | | | |
| D | 1 | 1 | r | r | RXS | XTAL_Tune | PFD reset | Dem_Tune | OOKXS | r | r | r | r | r | r | r | r | r | r | r | r | r | 0 |

NOTE: r = reserved. All reserved bits should be set low (0) during normal operation.

NOTE: All bits indicated as 1 should be set high (1) during normal operation.

NOTE: All bits indicated as 0 should be set low (0) during normal operation.

| ADDRESS | LOCATION | NO. OF BITS | DESCRIPTION | DEFAULT VALUE |
|---------|----------|-------------|---|---------------|
| 00xx | 21:17 | 5 | Main A divider coefficient (Mode 0) | 00000 |
| 00xx | 16:8 | 9 | Main B divider coefficient (Mode 0) | 001110000 |
| 00xx | 7:6 | 2 | Controls the PA attenuation (Mode 0) | 10 |
| 00xx | 5 | 1 | Enables transmit/receive path (Mode 0) | 0 |
| 00xx | 4 | 1 | Receive data polarity invert bit | 0 |
| 00xx | 3:2 | 2 | Controls charge pump peak current | 00 |
| 00xx | 1:0 | 2 | Output divider coefficient; band select | 10 |
| 01xx | 21:17 | 5 | Main A divider coefficient (Mode 1) | 00000 |
| 01xx | 16:8 | 9 | Main B divider coefficient (Mode 1) | 001110000 |
| 01xx | 7:6 | 2 | Controls the PA attenuation (Mode 1) | 10 |
| 01xx | 5 | 1 | Enables transmit/receive path (Mode 1) | 0 |
| 01xx | 4 | 1 | Controls modulation scheme (FSK or OOK) | 0 |
| 01xx | 3 | 1 | Enables or disables the power amplifier while in transmit mode or the receive chain while in receive mode | 0 |
| 01xx | 2:1 | 2 | Sets threshold for the brownout detector | 00 |
| 01xx | 0 | 1 | Enables brownout detector | 0 |
| 1000 | 21:14 | 8 | Reference divider coefficient | 01000000 |
| 1001 | 21:20 | 2 | Bit-rate divider D1 | 11 |
| 1001 | 19:17 | 3 | Bit-rate divider D2 | 010 |
| 1001 | 16 | 1 | Bit-rate divider D3 | 0 |
| 1001 | 15:14 | 2 | Receive mode select | 00 |
| 1001 | 13 | 1 | Transmit capture mode select | 0 |
| 1001 | 12 | 1 | RX training sequence pattern select | 0 |
| 1001 | 11:7 | 5 | Determines the minimum number of training bits | 00100 |
| 11x0 | 19 | 1 | Controls the position of the XTAL switch during FSK reception | 0 |
| 11x0 | 18:16 | 3 | Tunes the XTAL frequency by using an internal capacitor bank | 000 |
| 11x0 | 15 | 1 | PFD reset | 1 |
| 11x0 | 14:12 | 3 | Tunes the resonant frequency of the external demodulation tank circuit | 000 |
| 11x0 | 11 | 1 | Controls the position of the XTAL switch during OOK operation | 0 |

NOTE: x = don't care



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PRINCIPLES OF OPERATION

At power on/startup, all of the TRF6903 register contents are as per the default values.

Address 00XX (A-Word):

Word A is a 22-bit data register comprising seven fields. The main A-divider coefficient (mode 0), A<21:17>, is the 5-bit divider ratio of the A counter when the MODE terminal is low. The main B-divider coefficient (mode 0), A<16:8>, is the 9-bit value of the B counter when the MODE terminal is low. A <21:17> and A <16:8> are unsigned binary values. PA0, A<7:6>, is the 2-bit PA attenuation setting when the MODE terminal is low. TX/RX0, A<5>, is the TX/RX switch when the MODE terminal is low. PI, A<4>, is the data polarity invert bit. When high, this bit causes the data slicer output to be inverted. CP Acc., A<3:2>, sets the charge pump current. BND, A<1:0>, sets the output divider, which in turn determines the band of operation.

Terminal 21 (MODE) selects bits A<21:5> if low, or B<21:5> if high.

Main divider A<21:17>: 5-bit value for divider ratio of the A counter

Main divider A<16:8>: 9-bit value for divider ratio of the B counter

PA attenuation A<7:6>: 2 bits for setting the PA attenuation

| A<7:6> | PA ATTENUATION |
|--------|----------------|
| 00 | 0 dB |
| 01 | 10 dB |
| 10 | 20 dB |
| 11 | Not defined |

A<5>: 1-bit TX/RX mode select

| A<5> | TX/RX MODE |
|------|------------|
| 0 | RX mode |
| 1 | TX mode |

A<4>: 1-bit data polarity invert bit

| A<4> | RX DATA POLARITY |
|------|------------------|
| 0 | Noninverted |
| 1 | Inverted |

A<3:2>: 2 bits for setting the charge pump current

| A<3:2> | CP CURRENT |
|--------|-------------|
| 00 | 0.5 mA |
| 01 | 1 mA |
| 10 | 0.25 mA |
| 11 | Not defined |

PRINCIPLES OF OPERATION

A<1:0>: 2-bit value to set the output divider and thus select the band of operation.

| A<1:0> | OUTPUT DIVIDER RATIO, P | BAND OF OPERATION |
|--------|-------------------------|--------------------|
| 00 | 3 | 315 MHz |
| 01 | 2 | 433 MHz |
| 10 | 1 | 868 MHz or 915 MHz |
| 11 | 1 | 868 MHz or 915 MHz |

Address 01XX (B-Word):

Word B is a 22-bit data register comprising eight fields. The main A-divider coefficient (mode 1), B<21:17>, is the 5-bit divider ratio of the A counter when the MODE terminal is high. The main B-divider coefficient (mode 1), B<16:8>, is the 9-bit value of the B counter when the MODE terminal is high. B<21:17> and B<16:8> are unsigned binary values. PA1, B<7:6>, is the 2-bit PA attenuation setting when the MODE terminal is high. TX/RX1, B<5>, is the TX/RX switch when the MODE terminal is high. FSK/OOK, B<4>, sets the modulation scheme for both TX and RX. Bit B<3> enables/disables the power amplifier while in transmit mode and enables/disables the receive chain while in receive mode. The detector threshold, B<2:1>, is the 2-bit setting for the threshold voltage of the brownout detector. Det. Enable, B<0>, is the brownout detector enable flag.

Terminal 21 (MODE) selects bits A<21:5> if low, or B<21:5> if high.

Main divider B<21:17>: 5-bit value for divider ratio of the A-counter
Main divider B<16:8>: 9-bit value for divider ratio of the B-counter

PA attenuation B<7:6>: 2 bits for setting the PA attenuation

| B<7:6> | PA ATTENUATION |
|--------|----------------|
| 00 | 0 dB |
| 01 | 10 dB |
| 10 | 20 dB |
| 11 | Not defined |

B<5>: 1-bit TX/RX mode select

| B<5> | TX/RX MODE |
|------|------------|
| 0 | RX mode |
| 1 | TX mode |

B<4> 1-bit modulation select

| B<4> | TX/RX MODULATION |
|------|------------------|
| 0 | OOK |
| 1 | FSK |

NOTE: During OOK reception, the OOK switch is closed. During FSK reception, the OOK switch is open.

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PRINCIPLES OF OPERATION

B<3>: 1-bit PA or receive chain enable/disable

| B<3> | PA OR RECEIVE CHAIN ENABLE/DISABLE |
|------|---------------------------------------|
| 0 | Disabled |
| 1 | Enabled |

B<2:1>: 2-bit value to set the threshold voltage for the brownout detector

| B<2:1> | THRESHOLD VOLTAGE |
|--------|-------------------|
| 00 | 2.2 V |
| 01 | 2.4 V |
| 10 | 2.6 V |
| 11 | 2.8 V |

B<0>: 1 bit to enable brownout detector

| B<0> | BROWNOUT DETECTOR |
|------|-------------------|
| 0 | Off |
| 1 | On |

Address 1000 (C-Word):

Word C is a 20-bit data register comprising four fields. The reference divider coefficient, C<21:14>, is the 8-bit divider ratio of the reference divider. The allowable reference divider range is 2 (C <21:14> = 00000010) through 255 (C <21:14> = 11111111).

Bits C<13> through C<2> are reserved and should be set to 0.

Address 1001 (E-Word):

Word E is a 20-bit data register comprising eight fields. The bit rate or bit frequency, used by the clock recovery receive modes and the transmit synchronous mode is controlled by the BRA, E<21:20>, BRB, E<19:17>, and BRC, E<16>, fields. These three fields control a sequence of dividers, D1 through D3, that divide the reference (crystal) frequency, F_X .

PRINCIPLES OF OPERATION

E<21:20>: 2 bits to set D1 divider setting

| E<21:20> | D1 |
|----------|----|
| 00 | 1 |
| 01 | 5 |
| 10 | 6 |
| 11 | 8 |

E<19:17>: 3 bits to set D2 divider setting

| E<19:17> | D2 |
|----------|-----|
| 000 | 1 |
| 001 | 2 |
| 010 | 4 |
| 011 | 8 |
| 100 | 16 |
| 101 | 32 |
| 110 | 64 |
| 111 | 128 |

E<16>: 1 bit to set D3 divider setting

| E<16> | D3 |
|-------|----|
| 0 | 16 |
| 1 | 15 |

RXM, E<15:14> controls the signals that appear at the RX_DATA and DCLK terminals. The definition of RXM is contained in Table 3.

TXM, E<13>, sets the transmit capture mode. If TXM is low, the TX_DATA terminal controls the transmit function asynchronously. If TXM is high, the bit-rate clock is output at DCLK and the transmit data at the TX_DATA terminal is latched on the rising edge of DCLK, where DCLK is the bit-rate clock.

TWO, E<12>, sets the receive training sequence pattern. If TWO is high, the expected training sequence is assumed to be alternating pairs of ones and zeroes. If TWO is low, the expected training sequence is assumed to be alternating ones and zeroes.

TCOUNT, E<11:7>, determines the minimum number of training bits. The minimum number of training bits is four times the unsigned binary value of TCOUNT, plus two if TWO = 0 or plus three if TWO = 1.

Bits E<6> through E<2> are reserved and should be set to 0.

Address 11X0 (D-Word):

Word D is a 21-bit data register comprising three fields. XTAL_Tune, D<18:16>, is used to fine tune the crystal frequency by using an internal capacitor bank. PFD reset, D<15>, selects the source of the PFD reset signal. Dem_Tune, D<14:12>, is a 3-bit value used to tune the demodulator time constant. Bit D<11> controls the position of the XTAL switch during OOK operation.

D<19>: 1-bit value to control the position of the XTAL switch during FSK reception, when B<4>=1 and either A<5> or B<5> = 0. It is recommended to set this bit to 1 (XTAL switch closed). If D<19> is set to 0 (XTAL switch open), the LO frequency injected into the mixer is $f_{outs} = f_{LO} + \text{designed peak-peak deviation}$. This results in the down-converted IF signal shifting higher (high-side injection) or lower (low-side injection) from the IF center frequency (10.7 MHz) by an amount equal to the designed peak-peak frequency deviation.

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PRINCIPLES OF OPERATION

| D<19> | XTAL SWITCH DURING FSK RECEPTION | TERMINAL 31 |
|-------|----------------------------------|------------------------------|
| 0 | Unconnected (open) | High-Z |
| 1 | Connected (closed) | Shorted to ground internally |

D<18:16>: 3-bit value to fine-tune the XTAL frequency by using an internal capacitor bank.

| D<18:16> | TYPICAL LOAD CAPACITANCE |
|----------|--------------------------|
| 000 | 13.23 pF |
| 001 | 22.57 pF |
| 010 | 17.9 pF |
| 011 | 27.24 pF |
| 100 | 15.56 pF |
| 101 | 24.9 pF |
| 110 | 20.23 pF |
| 111 | 29.57 pF |

D<15>: 1-bit value to select the reset signal for the PFD

| D<15> | RESET SIGNAL |
|-------|------------------------|
| 0 | Derived from XTAL |
| 1 | Derived from prescaler |

NOTE: The default setting for D<15> is 1.

D<14:12>: 3-bit value to tune the resonant frequency of the external demodulator tank circuit. It can be used to optimize the receiver performance. The recommended default setting is 110.

D<11>: 1-bit value to control position of the XTAL switch during OOK operation, when B<4> = 0.

| D<11> | XTAL SWITCH DURING OOK OPERATION | TERMINAL 31 |
|-------|----------------------------------|------------------------------|
| 0 | Unconnected (open) | High-Z |
| 1 | Connected (closed) | Shorted to ground internally |

It is recommended that D<19> and D<11> be set to 0 during FSK reception and OOK operation.

Bits D<21>, D<20>, and D<10> through D<1> are reserved and should be set to 0.

operating modes

Controlled with terminal 26, $\overline{\text{STDBY}}$

| $\overline{\text{STDBY}}$ | OPERATING MODE |
|---------------------------|---|
| 0 | Power down of all blocks—programming mode |
| 1 | Operational mode and programming mode |

Controlled with terminal 21, MODE

| MODE | OPERATING MODE |
|------|----------------|
| 0 | Enable A-word |
| 1 | Enable B-word |



PRINCIPLES OF OPERATION

Controlled with terminal 39, $\overline{\text{LEARN/HOLD}}$

| $\overline{\text{LEARN/HOLD}}$ | OPERATING MODE |
|--------------------------------|---|
| 0 | Selects data slicer decision level to HOLD |
| 1 | Selects data slicer decision level to LEARN |

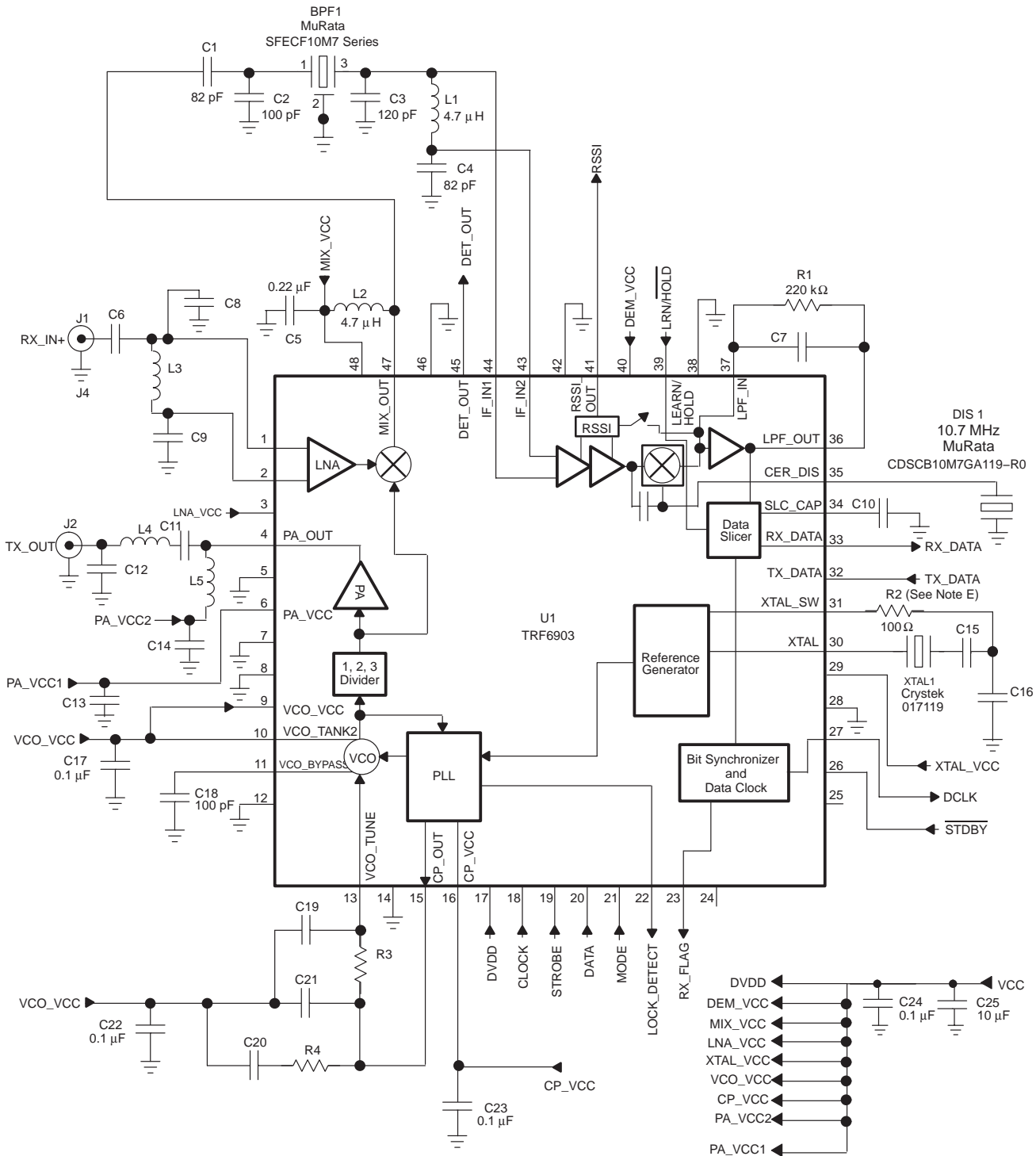
The transmit/receive mode is controlled by the TX/RX0, A<5>, TX/RX1, B<5>, and PARXED, B<3>, fields and the MODE and $\overline{\text{STDBY}}$ terminals.

| A<5> | B<5> | B<3> | MODE | $\overline{\text{STDBY}}$ | OPERATING MODE |
|------|------|------|------|---------------------------|---|
| X | X | X | X | 0 | Off, programming mode; SPI enabled |
| 0 | X | 0 | 0 | 1 | Receive mode 0, RX chain disabled. Reference, PLL, VCO and dividers enabled |
| 0 | X | 1 | 0 | 1 | Receive mode 0, RX chain enabled. Reference, PLL, VCO and dividers enabled |
| 1 | X | 0 | 0 | 1 | Transmit mode 0, PA disabled. Reference, PLL, VCO and dividers enabled |
| 1 | X | 1 | 0 | 1 | Transmit mode 0, PA enabled. Reference, PLL, VCO and dividers enabled |
| X | 0 | 0 | 1 | 1 | Receive mode 1, RX chain disabled. Reference, PLL, VCO and dividers enabled |
| X | 0 | 1 | 1 | 1 | Receive mode 1, RX chain enabled. Reference, PLL, VCO and dividers enabled |
| X | 1 | 0 | 1 | 1 | Transmit mode 1, PA disabled. Reference, PLL, VCO and dividers enabled |
| X | 1 | 1 | 1 | 1 | Transmit mode 1, PA enabled. Reference, PLL, VCO and dividers enabled |

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APPLICATION INFORMATION



NOTE: See Table 5 for component selection for band of operation.

Figure 11. Typical TRF6903 FSK Application Schematic



APPLICATION INFORMATION

Table 5. Component Selection for Band of Operation, FSK

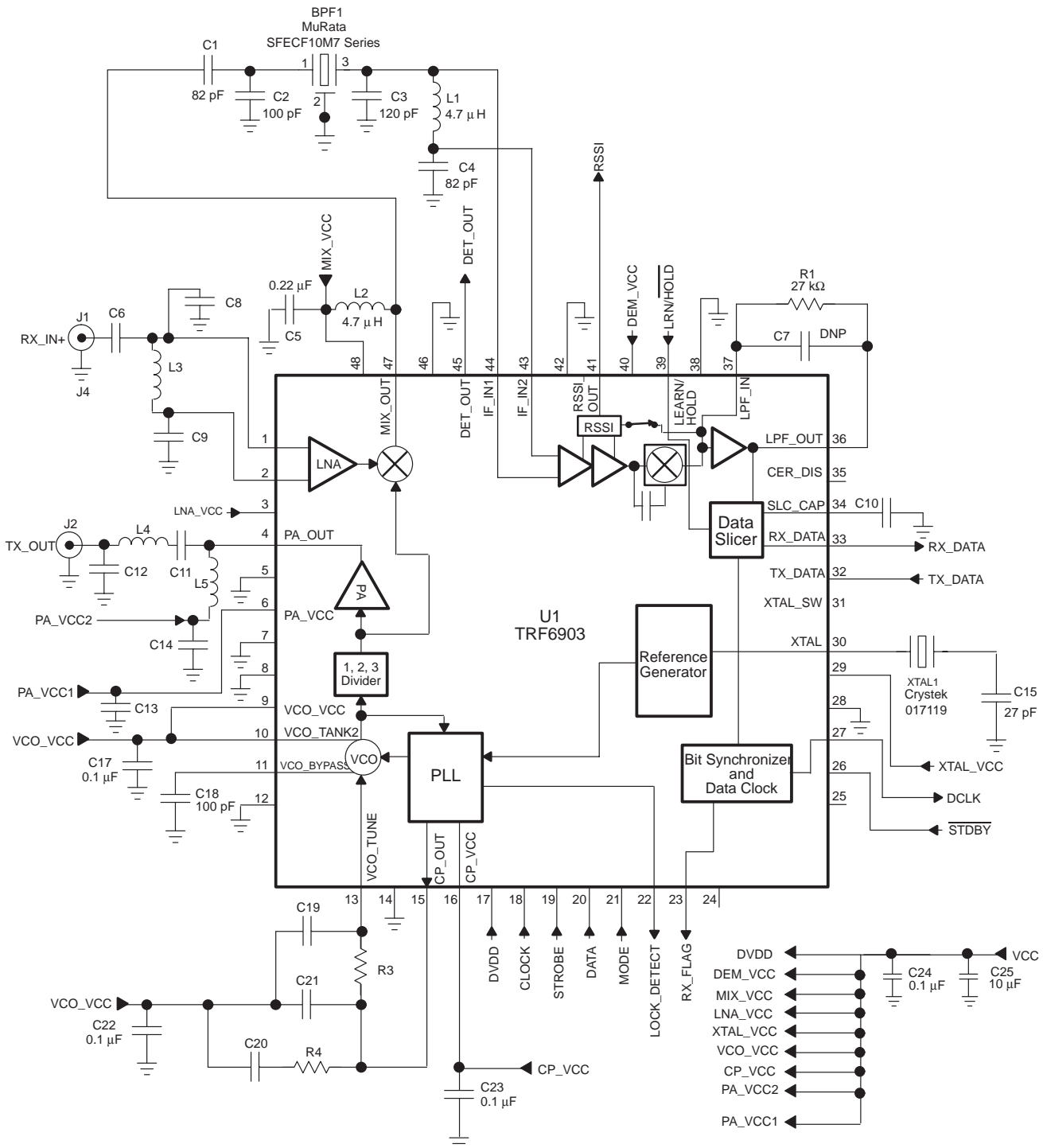
| | 315 MHz | | 433 MHz | | 868 MHz | | 915 MHz | |
|-----------------------------------|-----------|----------------|-----------|----------------|-----------|----------------|-----------|----------------|
| | Component | Value | Component | Value | Component | Value | Component | Value |
| Rx LNA Matching Network | C8 | 15 pF | C8 | 8.2 pF | C8 | 2.7 pF | C8 | 1.5 pF |
| | C6 | 330 pF | C6 | 180 pF | C6 | 39 pF | C6 | 33 pF |
| | C9 | 15 pF | C9 | 8.2 pF | C9 | 2.7 pF | C9 | 1.8 pF |
| | L3 | 27 nH | L3 | 22 nH | L3 | 15 nH | L3 | 12 nH |
| Tx PA Matching Network | C11 | 390 pF | C11 | 270 pF | C11 | 43 pF | C11 | 43 pF |
| | C14 | 390 pF | C14 | 270 pF | C14 | 39 pF | C14 | 33 pF |
| | L5 | 560 nH | L5 | 470 nH | L5 | 330 nH | L5 | 270 nH |
| | L4 | 75 nH | L4 | 39 nH | L4 | 15 nH | L4 | 15 nH |
| | C12 | 7.5 pF | C12 | 6.8 pF | C12 | 3.9 pF | C12 | 2.7 pF |
| | C13 | 390 pF | C13 | 270 pF | C13 | 39 pF | C13 | 33 pF |
| PLL Loop Filter | C19 | 75 pF | C19 | 75 pF | C19 | 75 pF | C19 | 75 pF |
| | C21 | 120 pF | C21 | 120 pF | C21 | 120 pF | C21 | 120 pF |
| | C20 | 5600 pF | C20 | 5600 pF | C20 | 5600 pF | C20 | 5600 pF |
| | R3 | 15 k Ω | R3 | 15 k Ω | R3 | 15 k Ω | R3 | 15 k Ω |
| | R4 | 7.5 k Ω | R4 | 7.5 k Ω | R4 | 7.5 k Ω | R4 | 7.5 k Ω |
| Post Detection Low-Pass Filter | C7 | 18 pF | C7 | 18 pF | C7 | 18 pF | C7 | 18 pF |
| Sample and Hold Capacitor | C10 | 3300 pF | C10 | 3300 pF | C10 | 3300 pF | C10 | 3300 pF |
| XTAL Switch Capacitor | C15 | 27 pF | C15 | 27 pF | C15 | 27 pF | C15 | 27 pF |
| | C16 | 5.6 pF | C16 | 9.1 pF | C16 | 20 pF | C16 | 22 pF |

- NOTES: A. Loop filter components selected for 19.2-kbps Manchester or 38.4-kbps NRZ for each band. $I_{CP} = 0.5$ mA, Reference Frequency = 409.6 kHz
- B. Post detection low-pass filter selected for 19.2-kbps Manchester or 38.4-kbps NRZ.
- C. Sample and hold capacitor selected for 7-bit training sequence and TWO = 0 (E<12>:0)
- D. XTAL switch capacitors selected for the frequency deviation of ± 50 kHz.
- E. R2 = 100 Ω is optional for operation in the 868-MHz and 915-MHz bands.

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NOTE: See Table 6 for component selection for band of operation.

Figure 12. Typical TRF6903 OOK Application Schematic With Ceramic IF Filter

APPLICATION INFORMATION

Table 6. Component Selection for Band of Operation, OOK

| | 315 MHz | | 433 MHz | | 868 MHz | | 915 MHz | |
|-------------------------------|-----------|----------------|-----------|----------------|-----------|----------------|-----------|----------------|
| | Component | Value | Component | Value | Component | Value | Component | Value |
| Rx LNA Matching Network | C8 | 15 pF | C8 | 8.2 pF | C8 | 2.7 pF | C8 | 1.5 pF |
| | C6 | 330 pF | C6 | 180 pF | C6 | 39 pF | C6 | 33 pF |
| | C9 | 15 pF | C9 | 8.2 pF | C9 | 2.7 pF | C9 | 1.8 pF |
| | L3 | 27 nH | L3 | 22 nH | L3 | 15 nH | L3 | 12 nH |
| Tx PA Matching Network | C11 | 390 pF | C11 | 270 pF | C11 | 43 pF | C11 | 43 pF |
| | C14 | 390 pF | C14 | 270 pF | C14 | 39 pF | C14 | 33 pF |
| | L5 | 560 nH | L5 | 470 nH | L5 | 330 nH | L5 | 270 nH |
| | L4 | 75 nH | L4 | 39 nH | L4 | 15 nH | L4 | 15 nH |
| | C12 | 7.5 pF | C12 | 6.8 pF | C12 | 3.9 pF | C12 | 2.7 pF |
| | C13 | 390 pF | C13 | 270 pF | C13 | 39 pF | C13 | 33 pF |
| PLL Loop Filter | C19 | 75 pF | C19 | 75 pF | C19 | 75 pF | C19 | 75 pF |
| | C21 | 120 pF | C21 | 120 pF | C21 | 120 pF | C21 | 120 pF |
| | C20 | 5600 pF | C20 | 5600 pF | C20 | 5600 pF | C20 | 5600 pF |
| | R3 | 15 k Ω | R3 | 15 k Ω | R3 | 15 k Ω | R3 | 15 k Ω |
| | R4 | 7.5 k Ω | R4 | 7.5 k Ω | R4 | 7.5 k Ω | R4 | 7.5 k Ω |
| Sample and Hold Capacitor | C10 | 3300 pF | C10 | 3300 pF | C10 | 3300 pF | C10 | 3300 pF |

- NOTES: A. Loop filter components selected for 19.2-kbps Manchester or 38.4-kbps NRZ for each band. $I_{CP} = 0.5$ mA, Reference Frequency = 409.6 kHz
 B. Sample and hold capacitor selected for 7-bit training sequence and TWO = 0 (E<12>:0)

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Revision History

| DATE | REV | PAGE | SECTION | DESCRIPTION |
|--------|-----|------|---------|--|
| 6/2/05 | D | 1 | — | Added application drawing to front page. |
| — | C | — | — | Information not available |
| — | B | — | — | Information not available |
| — | A | — | — | Information not available |
| — | * | — | — | Information not available |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TRF6903PT | NRND | LQFP | PT | 48 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TRF6903 | |
| TRF6903PTR | NRND | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | TRF6903 | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRF6903PTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRF6903PTR | LQFP | PT | 48 | 1000 | 350.0 | 350.0 | 43.0 |

TRAY

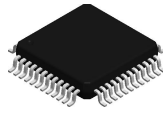


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|-----------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| TRF6903PT | PT | LQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |

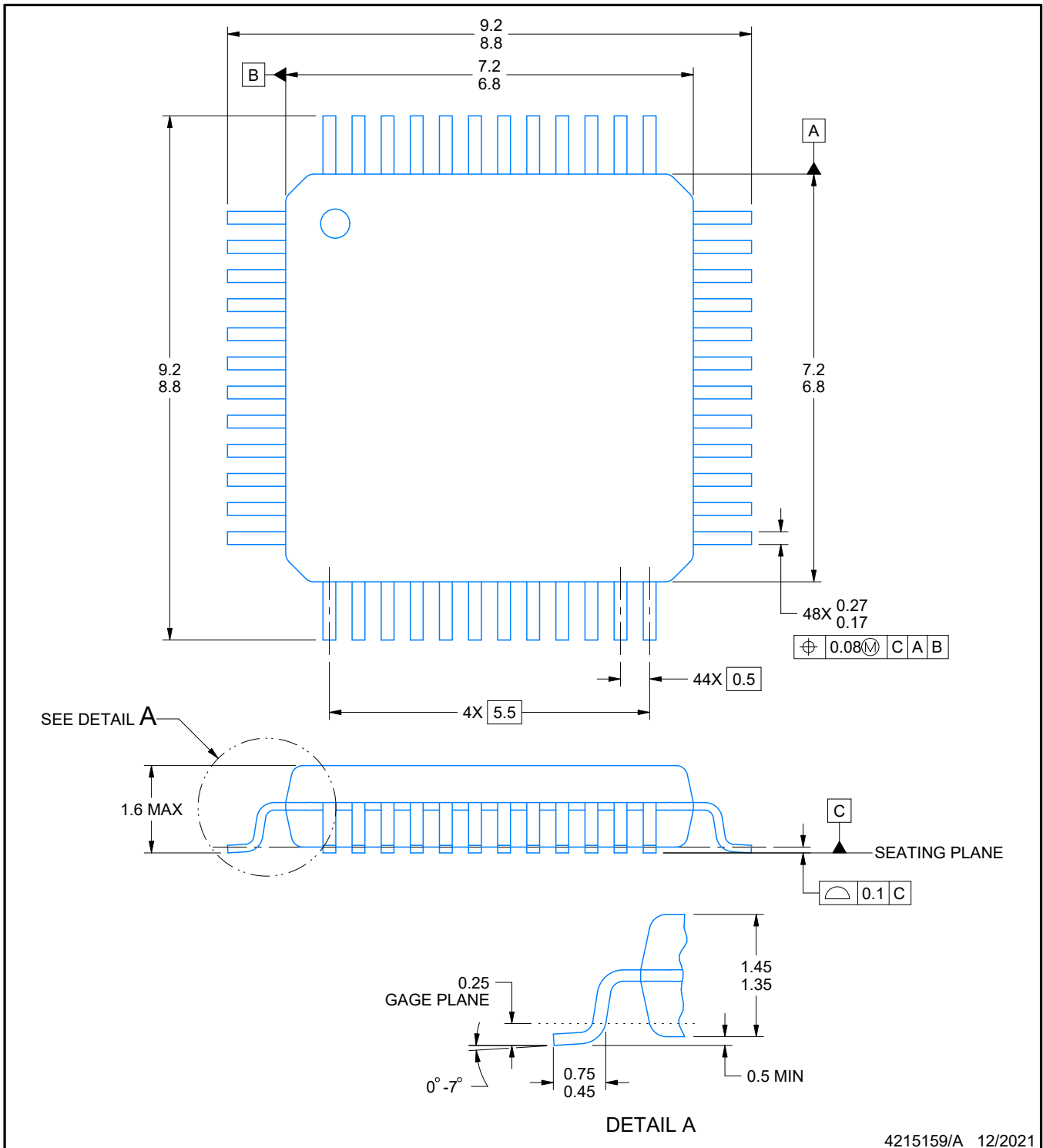
PT0048A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



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NOTES:

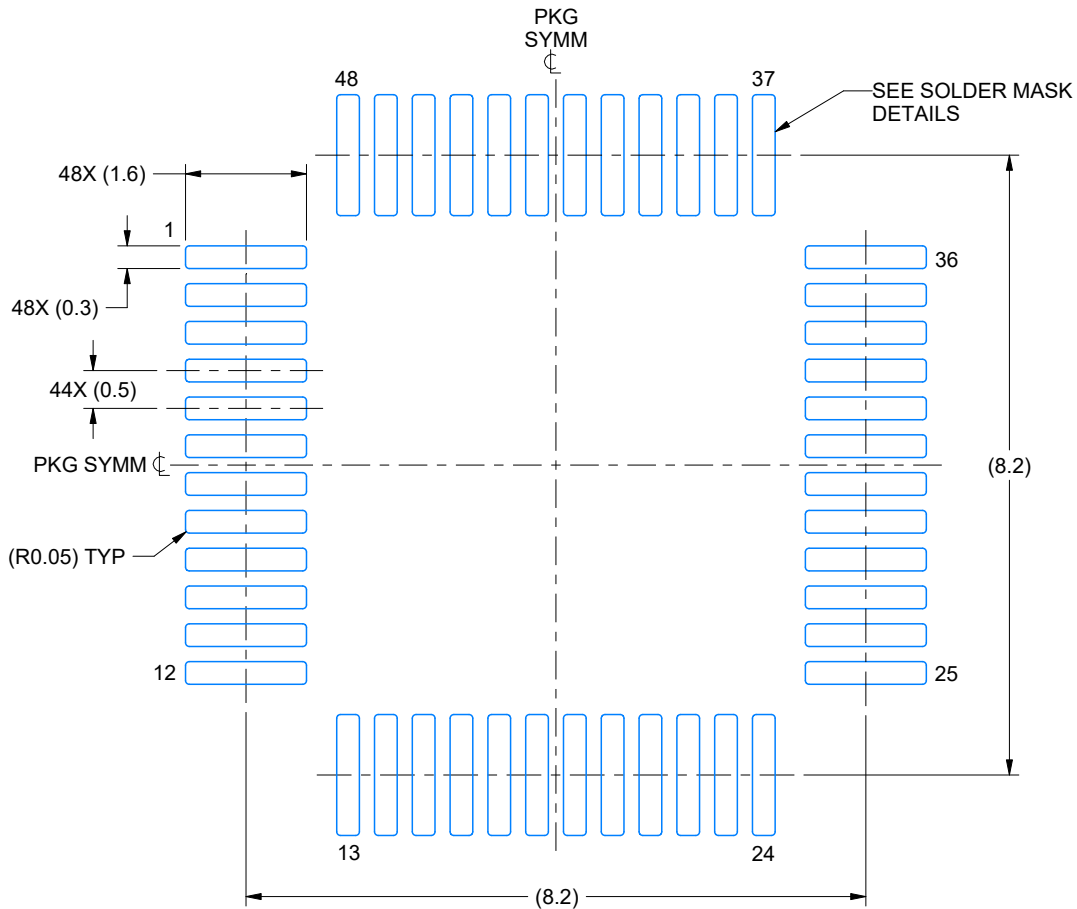
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

EXAMPLE BOARD LAYOUT

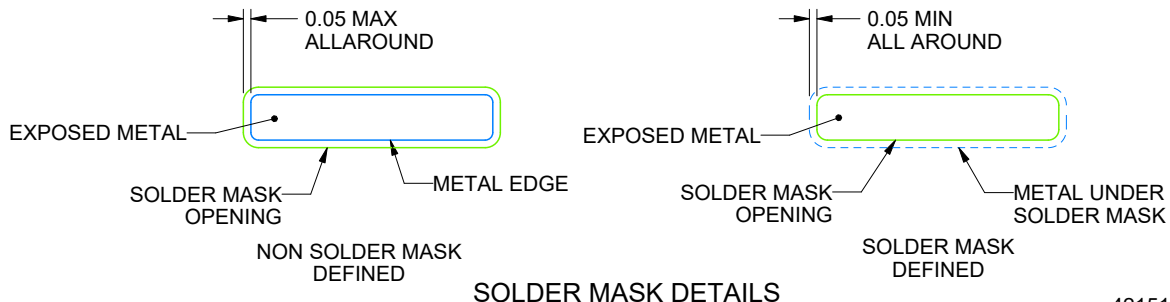
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

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NOTES: (continued)

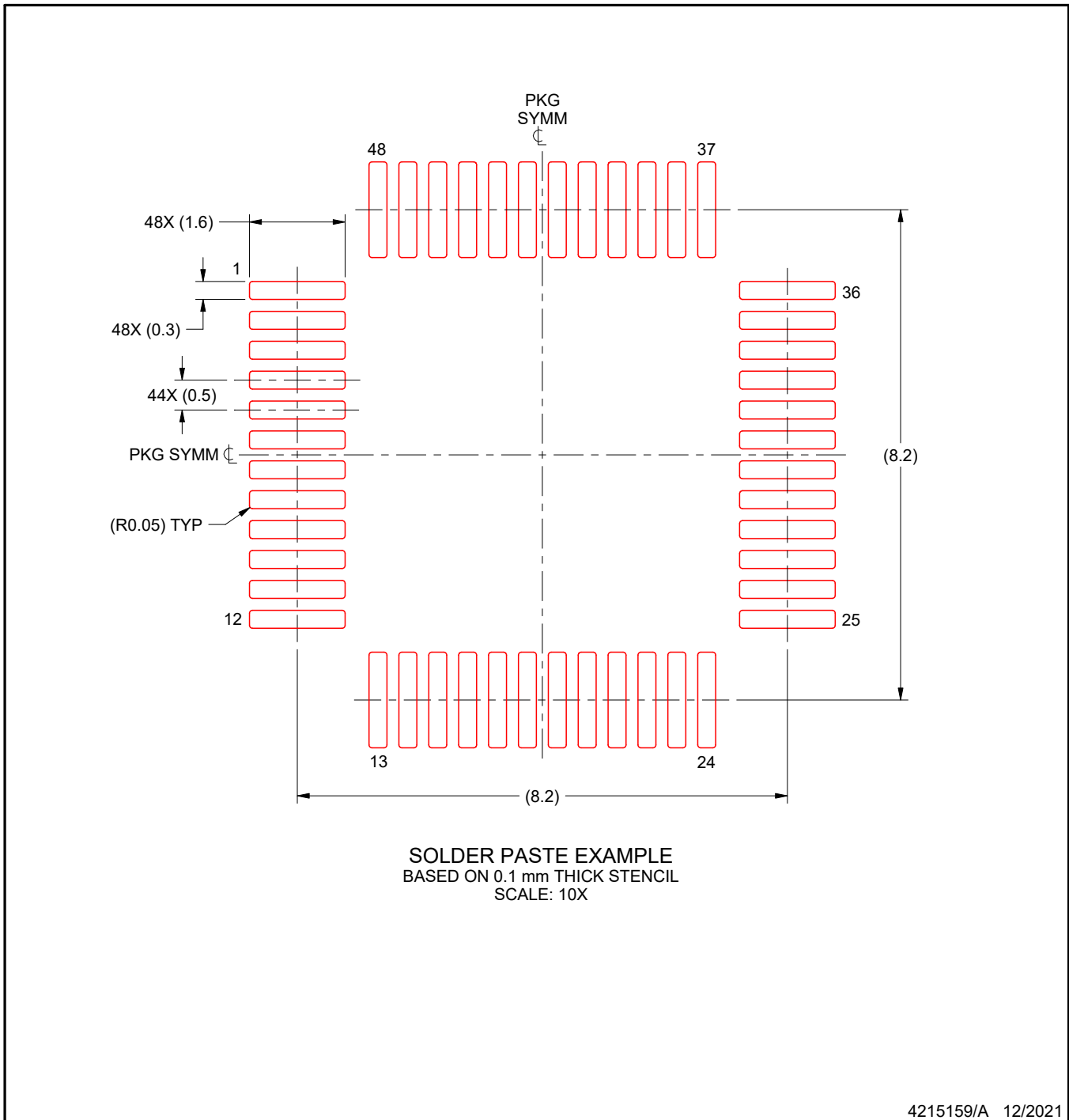
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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