CREE

C3M0120065D

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology

N-Channel Enhancement Mode

V_{DS}	650 V
$I_{D\ @\ 25^{\circ}C}$	22 A
$R_{DS(on)}$	120 mΩ

Features

- 3rd Generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Qrr)
- Halogen free, RoHS compliant

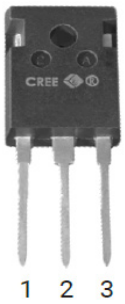
Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Applications

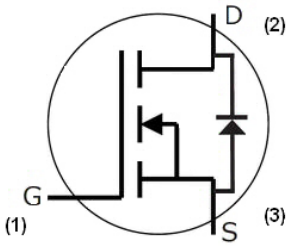
- Solar inverters
- DC/DC converters
- Switch Mode Power Supplies
- EV battery chargers
- UPS

Package



Halogen-Free

RoHS



Part Number	Package	Marking
C3M0120065D	TO-247-3	C3M0120065D

Maximum Ratings

Symbol	Parameter	Value	Unit	Note
V_{DSS}	Drain - Source Voltage, T_C = 25 ˚C	650	V	
V_{GS}	Gate - Source voltage (Under transient events < 100 ns)	-8/+19	V	Fig. 29
I_D	Continuous Drain Current, V_{GS} = 15 V, T_C = 25˚C	22	A	Fig. 19
	Continuous Drain Current, V_{GS} = 15 V, T_C = 100˚C	16		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_P limited by T_{jmax}	51	A	
P_D	Power Dissipation, T_C=25˚C, T_J = 175 ˚C	98	W	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-40 to +175	˚C	
T_L	Solder Temperature, 1.6mm (0.063”) from case for 10s	260	˚C	
M_d	Mounting Torque, (M3 or 6-32 screw)	1 8.8	Nm lbf-in	

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSon}	Gate-Source Recommended Turn-On Voltage		15		V	Static	Fig. 29
V_{GSoff}	Gate-Source Recommended Turn-Off Voltage		-4		V		
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3	3.6	V	V_{DS} = V_{GS}, I_D = 1.86 mA	Fig. 11
			1.9		V	V_{DS} = V_{GS}, I_D = 1.86 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		120	157	mΩ	V_{GS} = 15 V, I_D = 6.76 A	Fig. 4, 5,6
			168			V_{GS} = 15 V, I_D = 6.76 A, T_J = 175ºC	
g_{fs}	Transconductance		5.0		S	V_{DS}= 20 V, I_{DS}= 6.76 A	Fig. 7
			4.9			V_{DS}= 20 V, I_{DS}= 6.76 A, T_J = 175ºC	
C_{iss}	Input Capacitance		640		pF	V_{GS} = 0 V, V_{DS} = 0V to 400 V F = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		45				
C_{rss}	Reverse Transfer Capacitance		2.3				
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		57			V_{GS} = 0 V, V_{DS} = 0V to 400 V	Note: 1
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		79				Note: 1
E_{oss}	C_{oss} Stored Energy		4.3		µJ	V_{DS} = 400 V, F = 1 Mhz	Fig. 16
E_{ON}	Turn-On Switching Energy (Body Diode)		71		µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 6.76 A, $R_{G(ext)}$ = 10 Ω, L= 237 µH, T_J = 175ºC FWD = Internal Body Diode of MOSFET	Fig. 25
E_{OFF}	Turn Off Switching Energy (Body Diode)		8				
E_{ON}	Turn-On Switching Energy (External Diode)		57		µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 6.76 A, $R_{G(ext)}$ = 10 Ω, L= 237 µH, T_J = 175ºC FWD = External SiC DIODE	Fig. 25
E_{OFF}	Turn Off Switching Energy (External Diode)		7				
$t_{d(on)}$	Turn-On Delay Time		7		ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 6.76 A, $R_{G(ext)}$ = 10 Ω Timing relative to V_{DS} Inductive load	Fig. 26
t_r	Rise Time		17				
$t_{d(off)}$	Turn-Off Delay Time		13				
t_f	Fall Time		8				
$R_{G(int)}$	Internal Gate Resistance		6		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		7		nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 6.76 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		11				
Q_g	Total Gate Charge		28				

Note (1): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 400V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.5		V	V_{GS} = -4 V, I_{SD} = 3.4 A, T_J = 25 °C	Fig. 8, 9, 10
		4.0		V	V_{GS} = -4 V, I_{SD} = 3.4 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		16	A	V_{GS} = -4 V, T_C = 25˚C	
$I_{S, pulse}$	Diode pulse Current		51	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	18		ns	V_{GS} = -4 V, I_{SD} = 6.76 A, V_R = 400 V dif/dt = 2160 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	81		nC		
I_{rrm}	Peak Reverse Recovery Current	7		A		
t_{rr}	Reverse Recover time	25		ns	V_{GS} = -4 V, I_{SD} = 6.76 A, V_R = 400 V dif/dt = 900 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	76		nC		
I_{rrm}	Peak Reverse Recovery Current	4		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.53	°C/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

Typical Performance

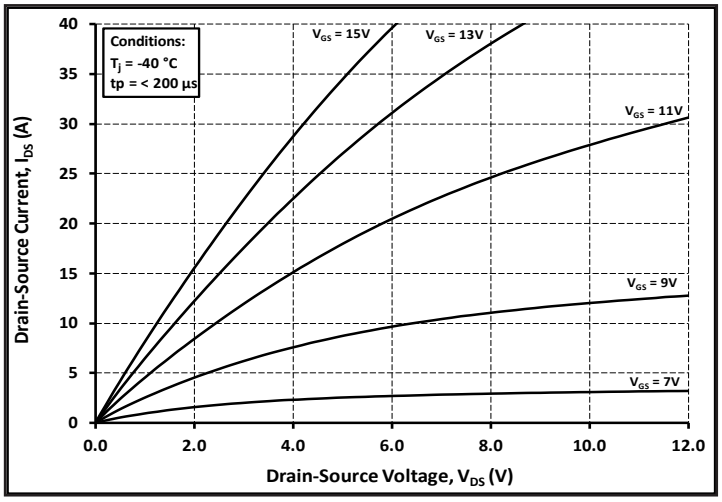


Figure 1. Output Characteristics T_J = -40 ºC

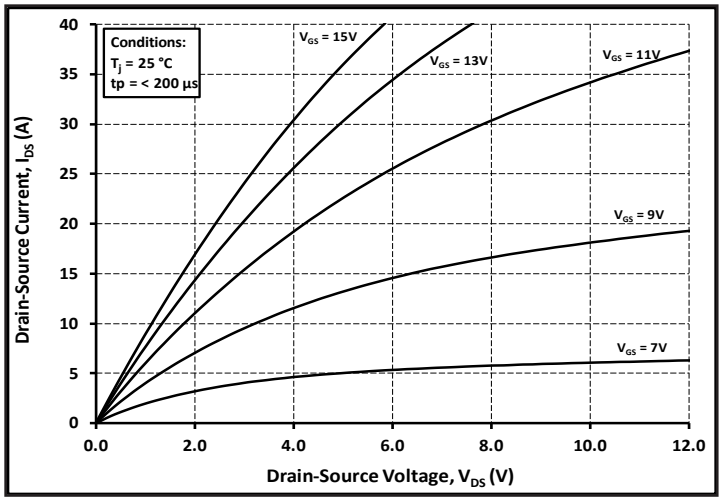


Figure 2. Output Characteristics T_J = 25 ºC

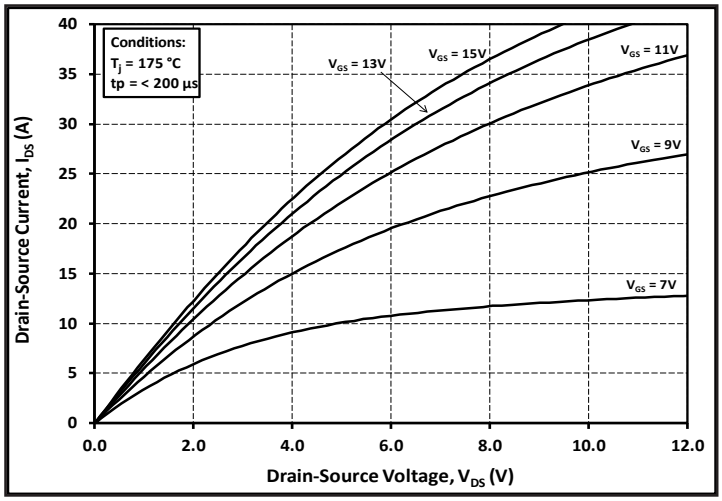


Figure 3. Output Characteristics T_J = 175 ºC

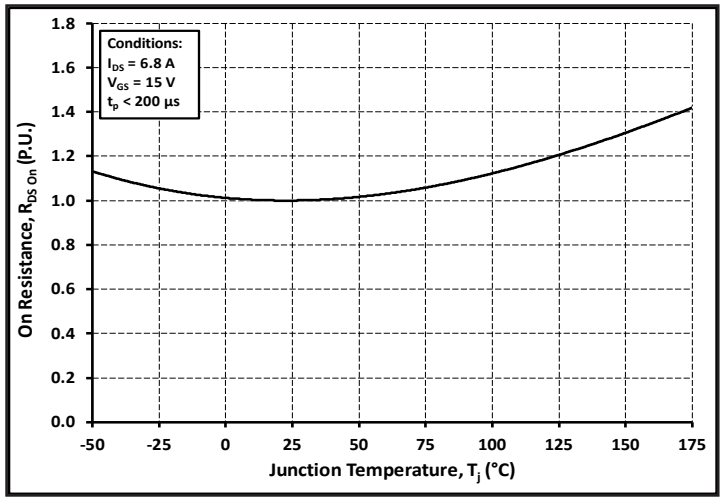


Figure 4. Normalized On-Resistance vs. Temperature

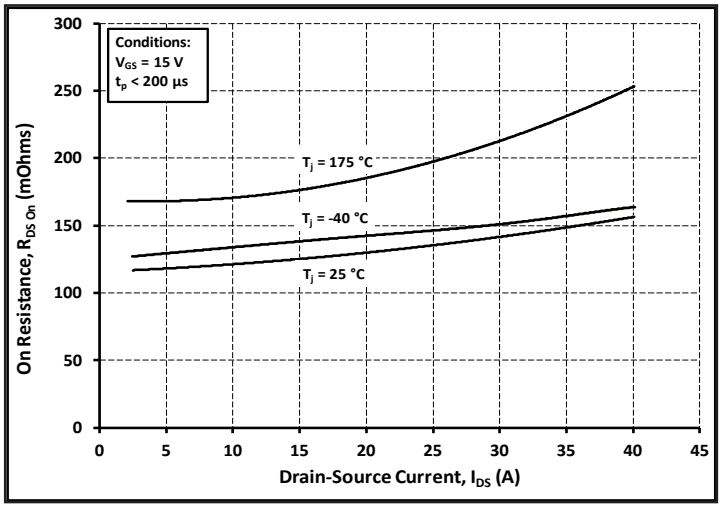


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

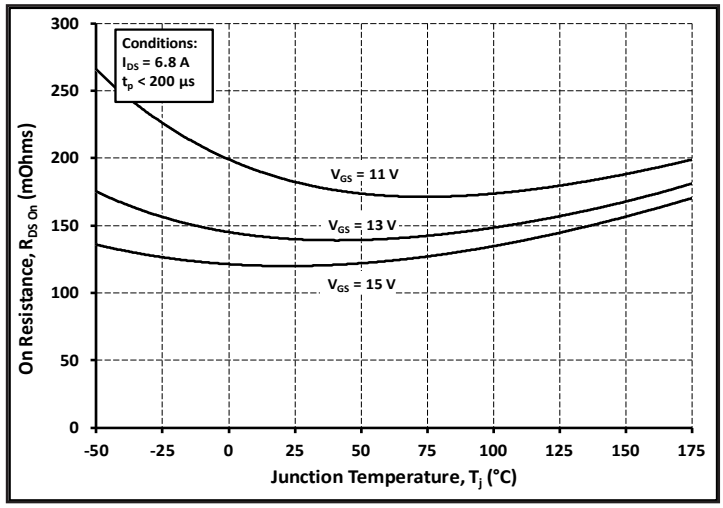


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

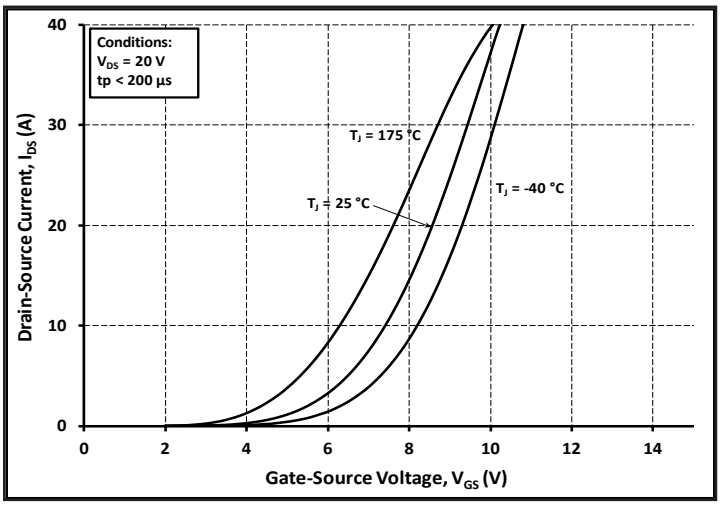


Figure 7. Transfer Characteristic for Various Junction Temperatures

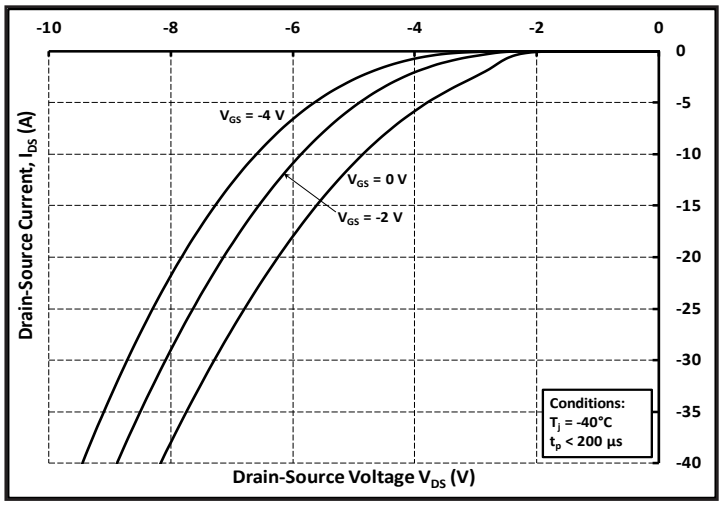


Figure 8. Body Diode Characteristic at -40 °C

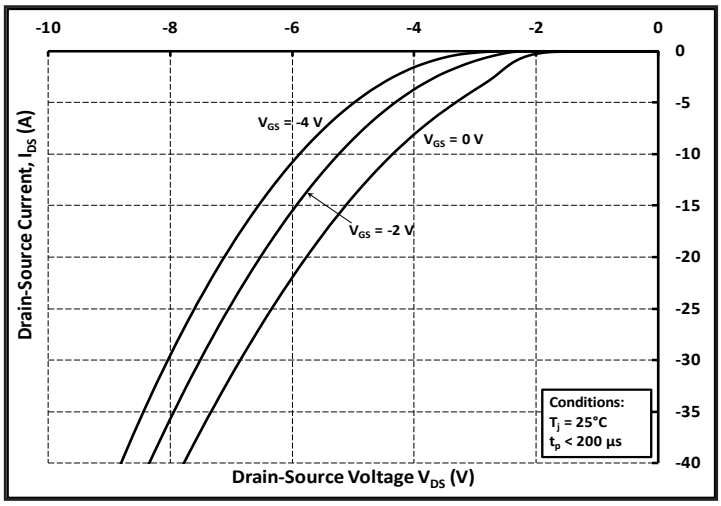


Figure 9. Body Diode Characteristic at 25 °C

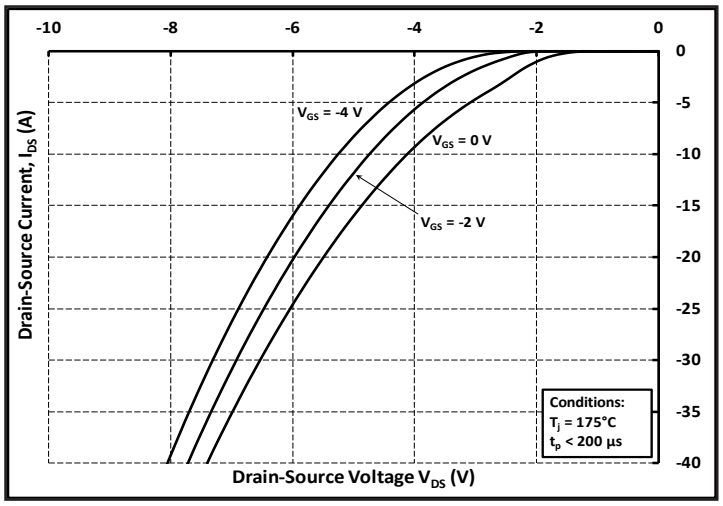


Figure 10. Body Diode Characteristic at 175 °C

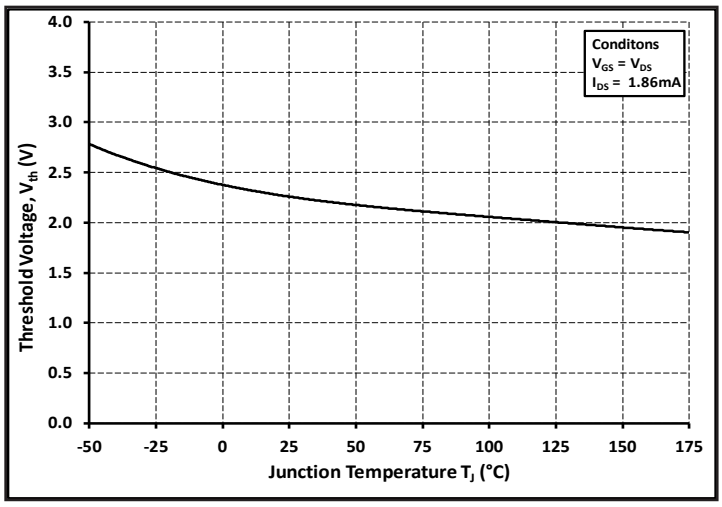


Figure 11. Threshold Voltage vs. Temperature

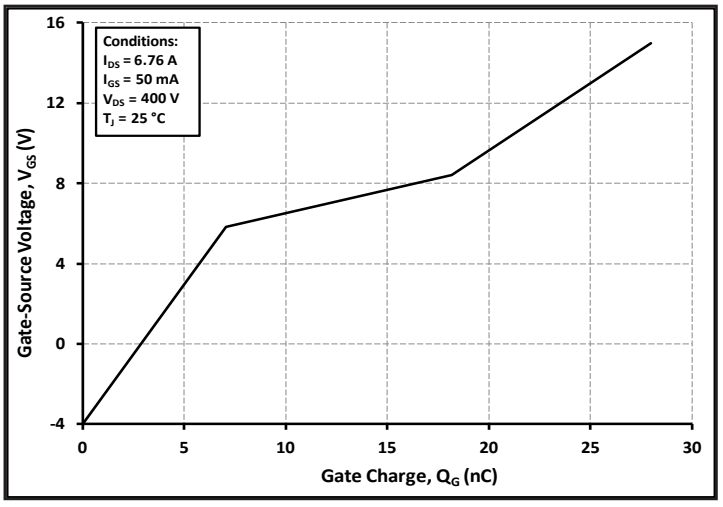


Figure 12. Gate Charge Characteristics

Typical Performance

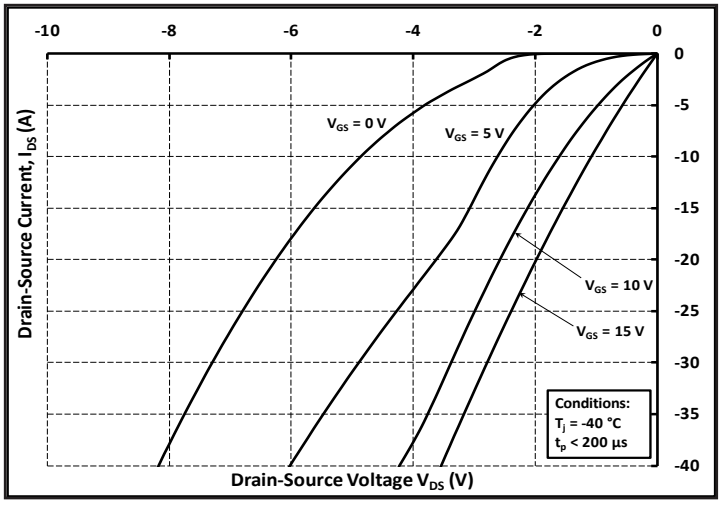


Figure 13. 3rd Quadrant Characteristic at -40 °C

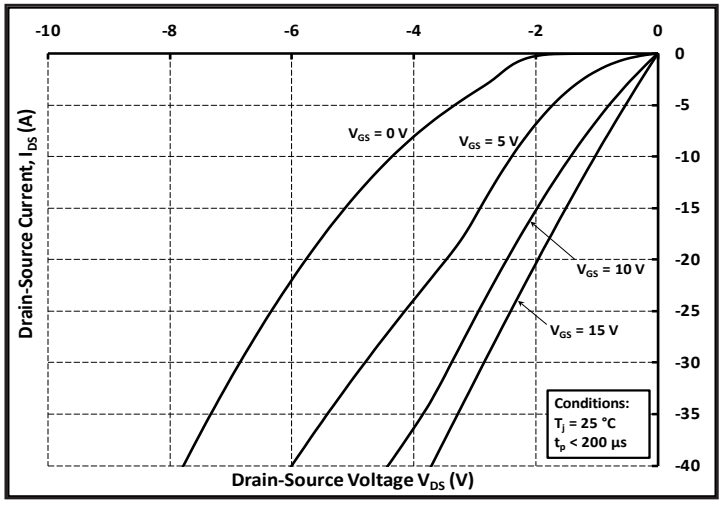


Figure 14. 3rd Quadrant Characteristic at 25 °C

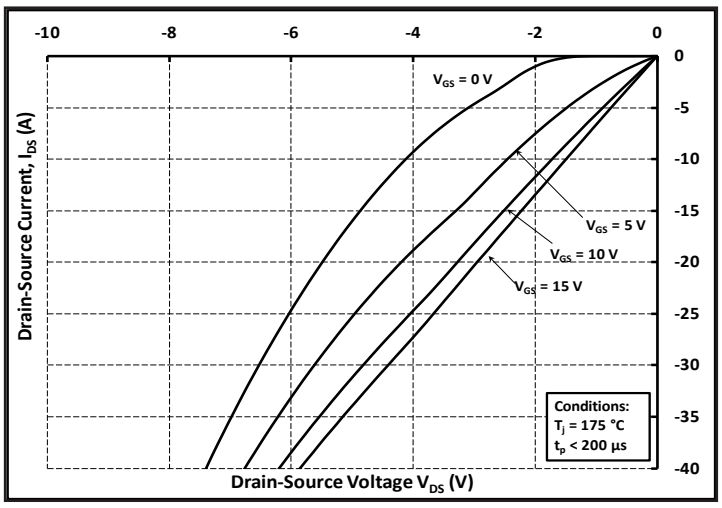


Figure 15. 3rd Quadrant Characteristic at 175 °C

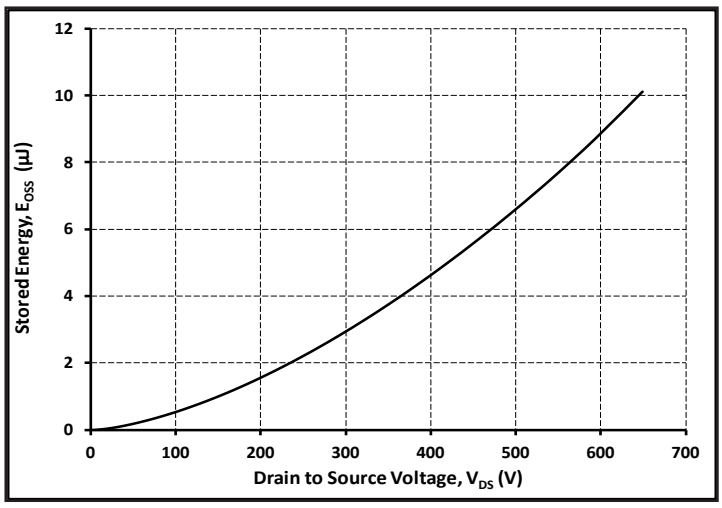


Figure 16. Output Capacitor Stored Energy

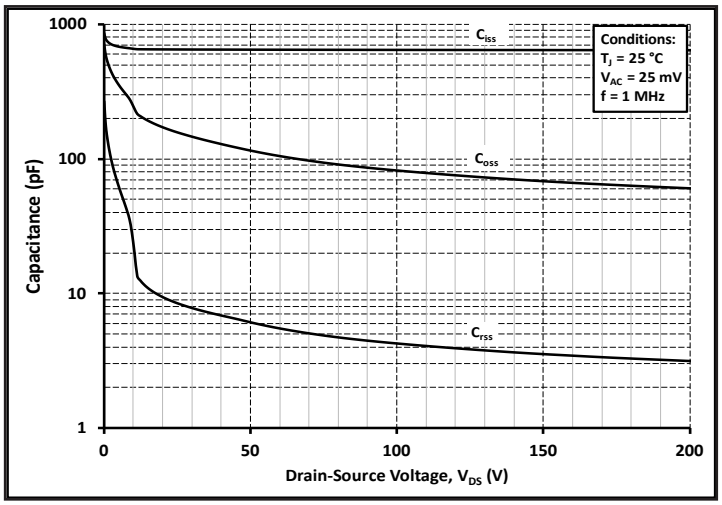


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

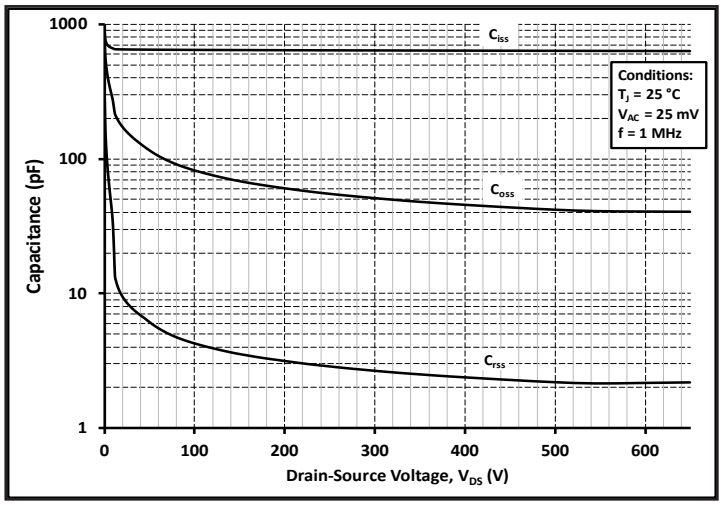


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

Typical Performance

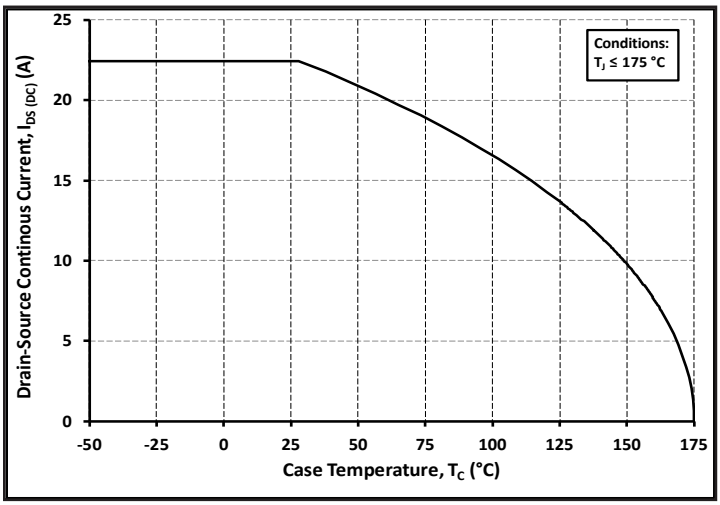


Figure 19. Continuous Drain Current Derating vs. Case Temperature

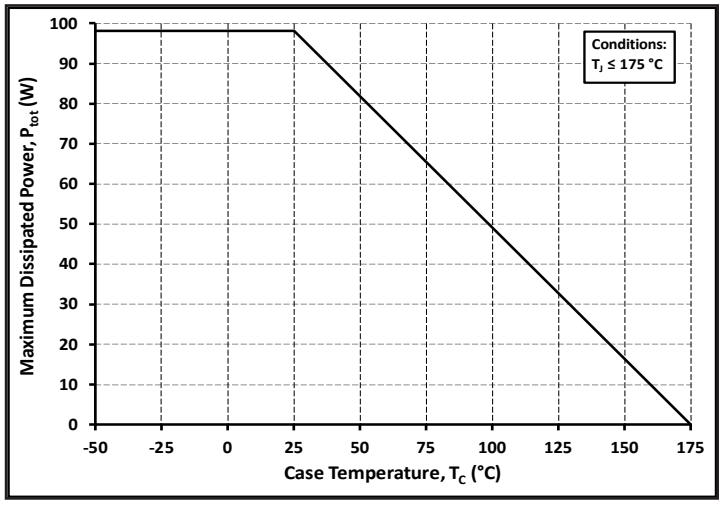


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

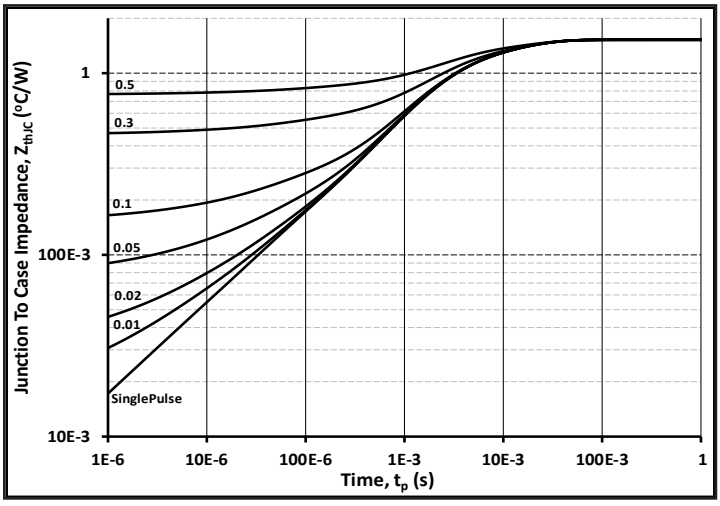


Figure 21. Transient Thermal Impedance (Junction - Case)

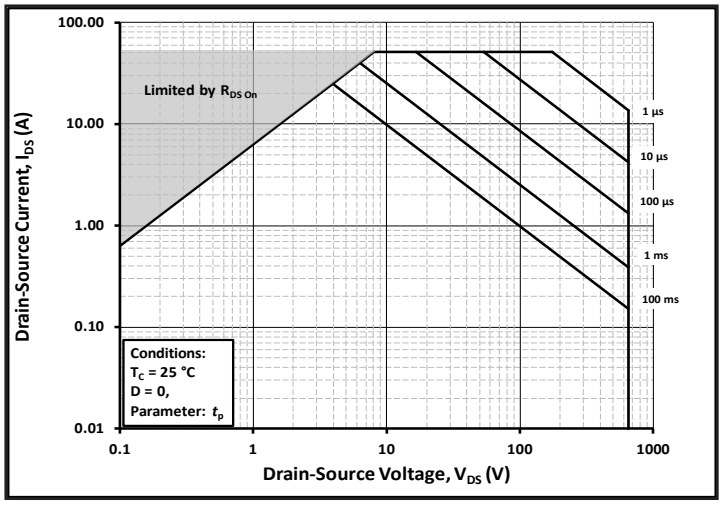


Figure 22. Safe Operating Area

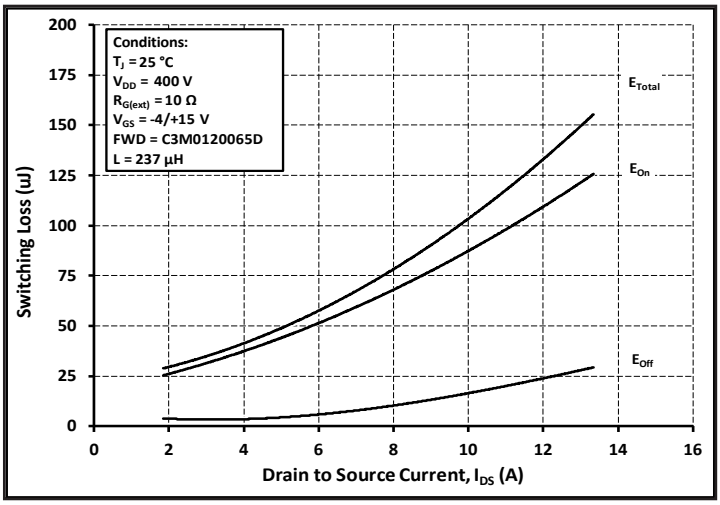


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400V)

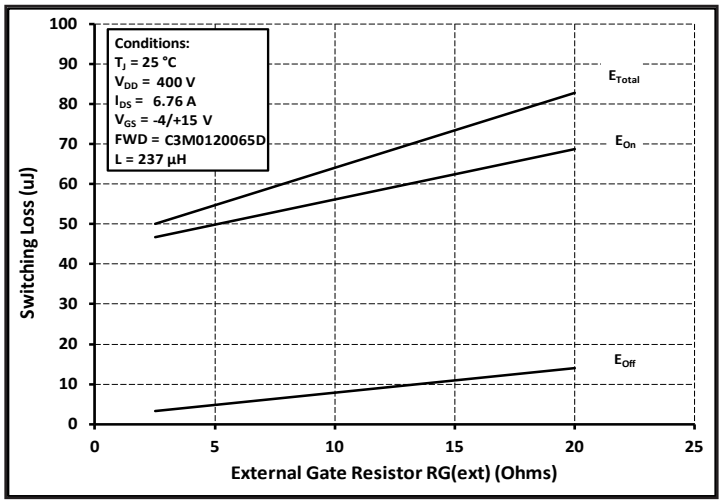


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

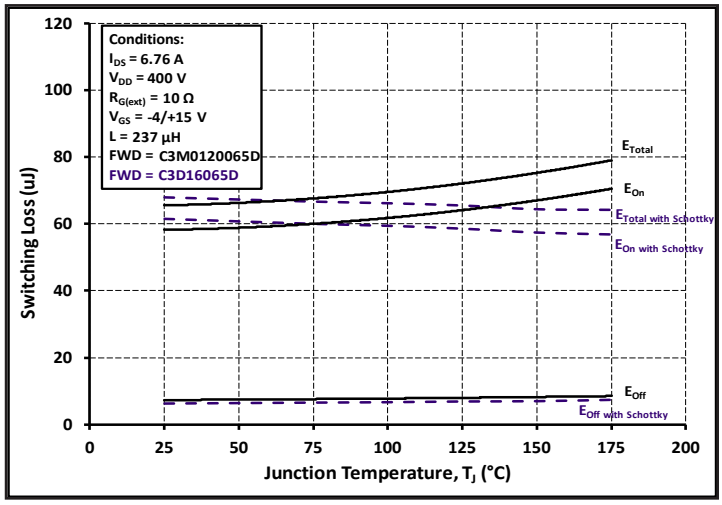


Figure 25. Clamped Inductive Switching Energy vs. Temperature

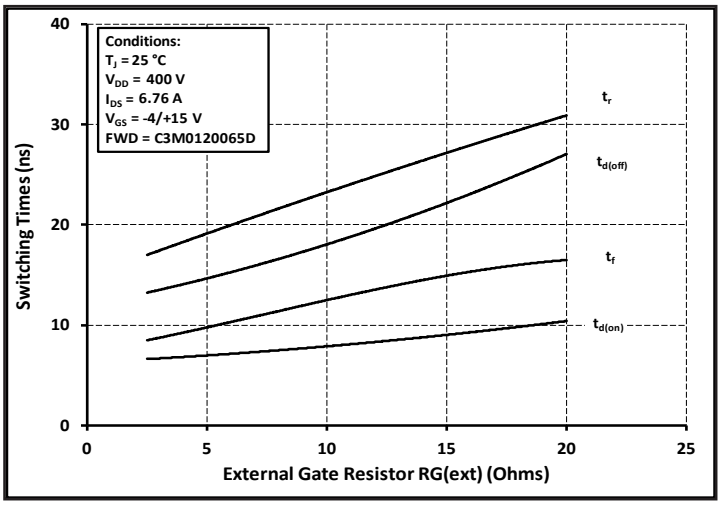


Figure 26. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

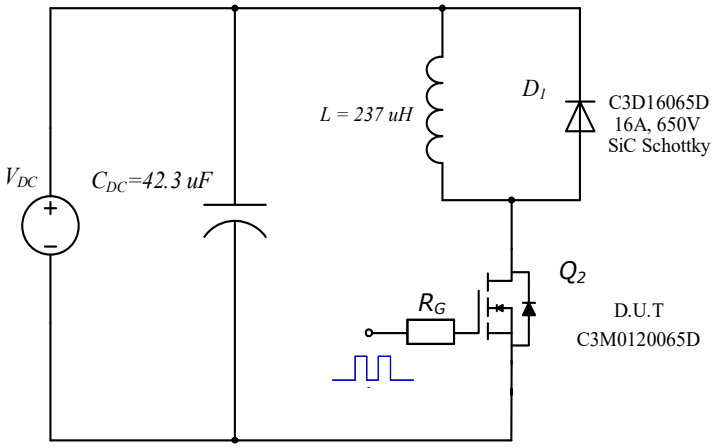


Figure 27. Clamped Inductive Switching Waveform Test Circuit

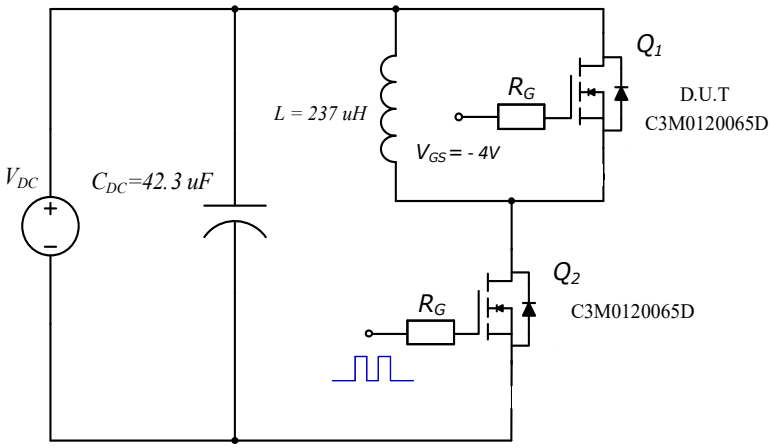


Figure 28. Body Diode Recovery Test Circuit

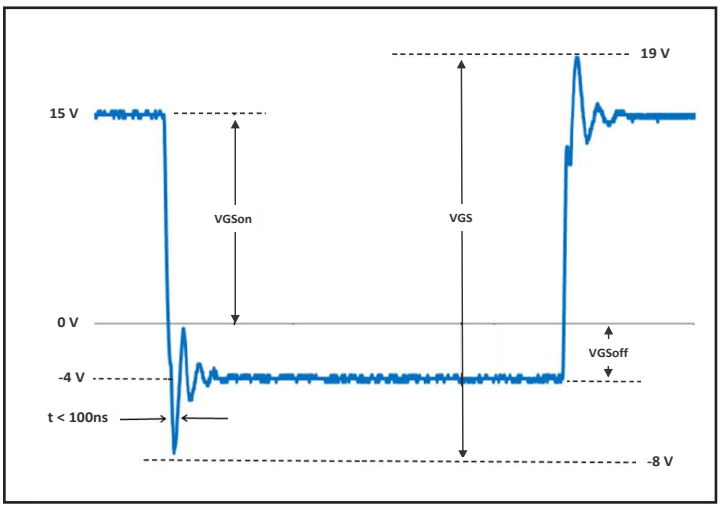
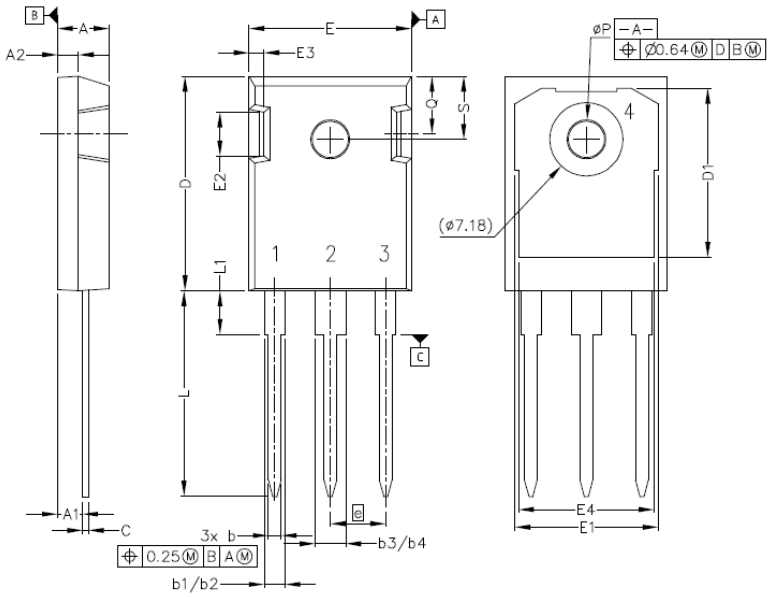
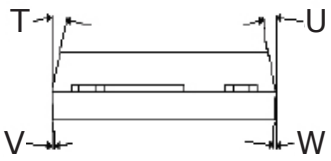


Figure 29. V_{GS} Waveform Example

Package Dimensions

Package TO-247-3



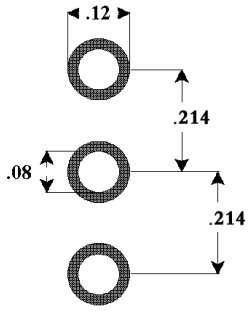


Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	9°	11°	9°	11°
U	9°	11°	9°	11°
V	2°	8°	2°	8°
W	2°	8°	2°	8°

Recommended Solder Pad Layout



TO-247-3

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **SPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

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