

December 1994

# 54F/74F74 Dual D-Type Positive Edge-Triggered Flip-Flop

## General Description

The '74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

### Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  sets Q to HIGH level
- LOW input to  $\bar{C}_D$  sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

## Features

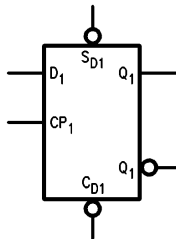
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F74PC		N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
	54F74DM (Note 2)	J14A	14-Lead Ceramic Dual-In-Line
74F74SC (Note 1)		M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F74SJ (Note 1)		M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F74FM (Note 2)	W14B	14-Lead Cerpack
	54F74LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

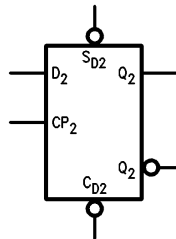
**Note 1:** Devices also available in 13" reel. Use Suffix = SCX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

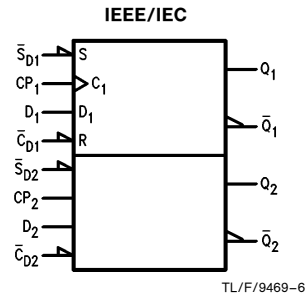
## Logic Symbols



TL/F/9469-3



TL/F/9469-4

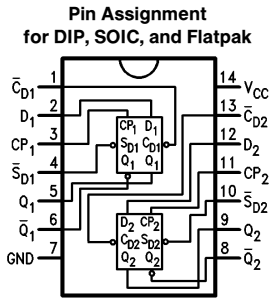


TL/F/9469-6

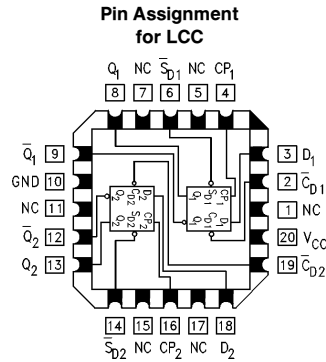
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54F/74F74 Dual D-Type Positive Edge-Triggered Flip-Flop

### Connection Diagrams



TL/F/9469-1



TL/F/9469-2

### Unit Loading/Fan Out

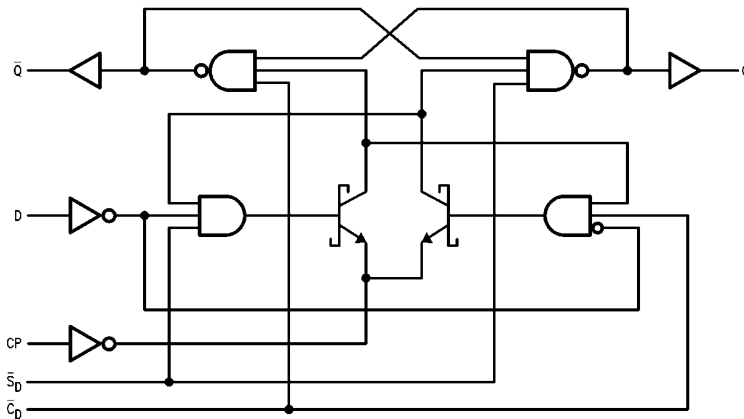
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
D <sub>1</sub> , D <sub>2</sub>	Data Inputs	1.0/1.0	20 μA/ -0.6 mA
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
C̄ <sub>D1</sub> , C̄ <sub>D2</sub>	Direct Clear Inputs (Active LOW)	1.0/3.0	20 μA/ -1.8 mA
S̄ <sub>D1</sub> , S̄ <sub>D2</sub>	Direct Set Inputs (Active LOW)	1.0/3.0	20 μA/ -1.8 mA
Q <sub>1</sub> , Q̄ <sub>1</sub> , Q <sub>2</sub> , Q̄ <sub>2</sub>	Outputs	50/33.3	-1 mA/20 mA

### Truth Table

Inputs				Outputs	
S̄ <sub>D</sub>	C̄ <sub>D</sub>	CP	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	h	H	L
H	H	↘	l	L	H
H	H	L	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

H (h) = HIGH Voltage Level  
 L (l) = LOW Voltage Level  
 X = Immaterial  
 Q<sub>0</sub> = Previous Q (Q̄) before LOW-to-HIGH Clock Transition  
 Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

### Logic Diagram



TL/F/9469-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

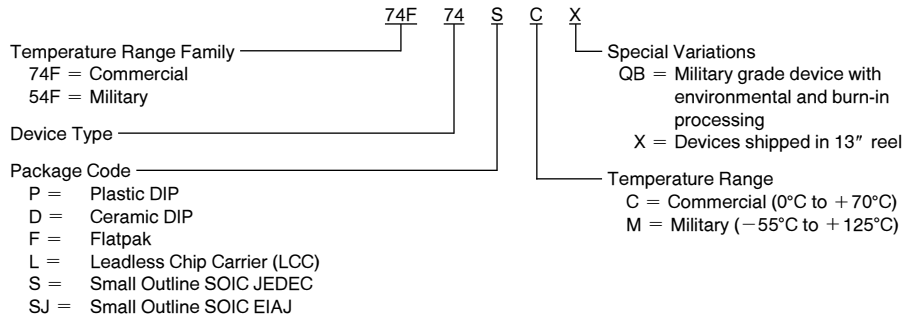
**DC Electrical Characteristics**

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				
		74F 5% V <sub>CC</sub>	2.7				
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.8	mA	Max	V <sub>IN</sub> = 0.5V (D, CP) V <sub>IN</sub> = 0.5V ( $\overline{C}_D$ , $\overline{S}_D$ )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		10.5	16.0	mA	Max	

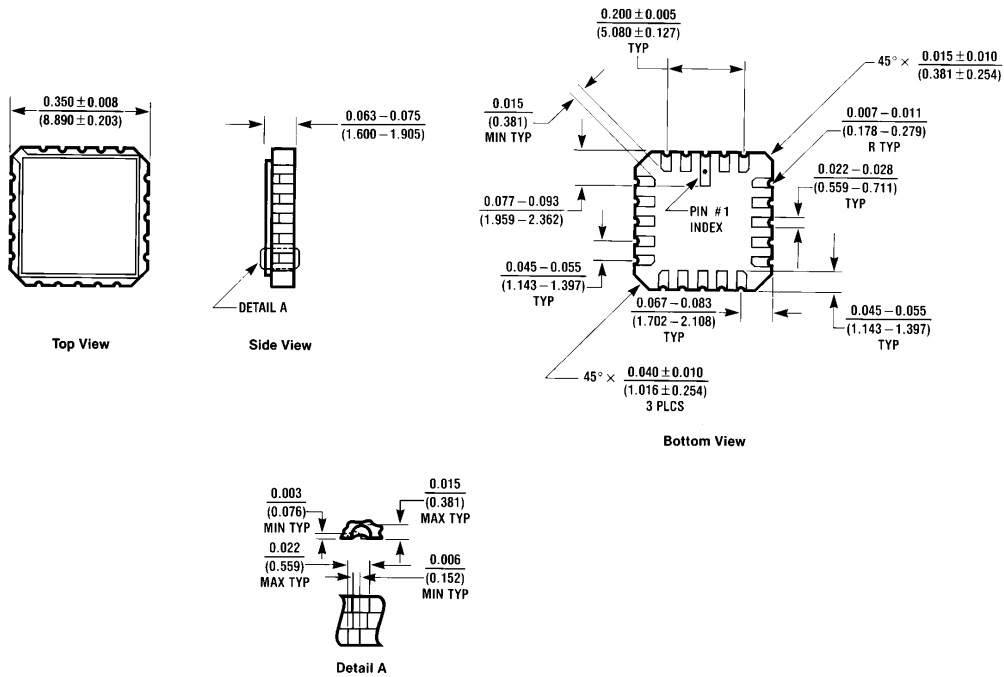
AC Electrical Characteristics									
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
$f_{\text{max}}$	Maximum Clock Frequency	100	125		80		100		MHz
$t_{\text{PLH}}$	Propagation Delay	3.8	5.3	6.8	3.8	8.5	3.8	7.8	ns
$t_{\text{PHL}}$	$CP_n$ to $Q_n$ or $\bar{Q}_n$	4.4	6.2	8.0	4.4	10.5	4.4	9.2	
$t_{\text{PLH}}$	Propagation Delay	3.2	4.6	6.1	3.2	8.0	3.2	7.1	ns
$t_{\text{PHL}}$	$\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to $Q_n$ or $\bar{Q}_n$	3.5	7.0	9.0	3.5	11.5	3.5	10.5	
AC Operating Requirements									
Symbol	Parameter	74F		54F		74F		Units	
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.0		3.0		2.0		ns	
$t_s(\text{L})$	$D_n$ to $CP_n$	3.0		4.0		3.0			
$t_h(\text{H})$	Hold Time, HIGH or LOW	1.0		2.0		1.0		ns	
$t_h(\text{L})$	$D_n$ to $CP_n$	1.0		2.0		1.0			
$t_w(\text{H})$	$CP_n$ Pulse Width	4.0		4.0		4.0		ns	
$t_w(\text{L})$	HIGH or LOW	5.0		6.0		5.0			
$t_w(\text{L})$	$\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ Pulse Width	4.0		4.0		4.0		ns	
$t_{\text{rec}}$	Recovery Time	2.0		3.0		2.0		ns	
	$\bar{C}_{Dn}$ or $\bar{S}_{Dn}$ to CP								

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



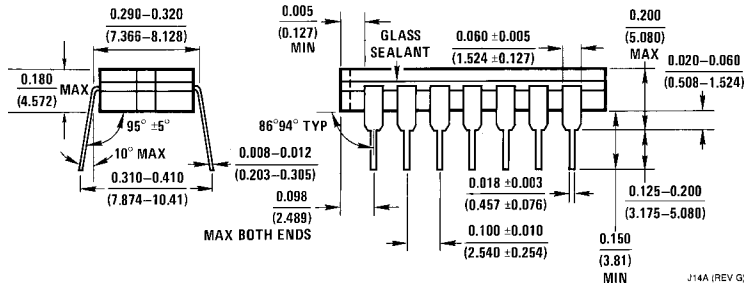
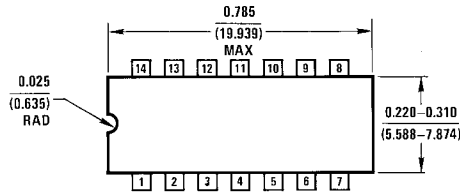
## Physical Dimensions inches (millimeters)



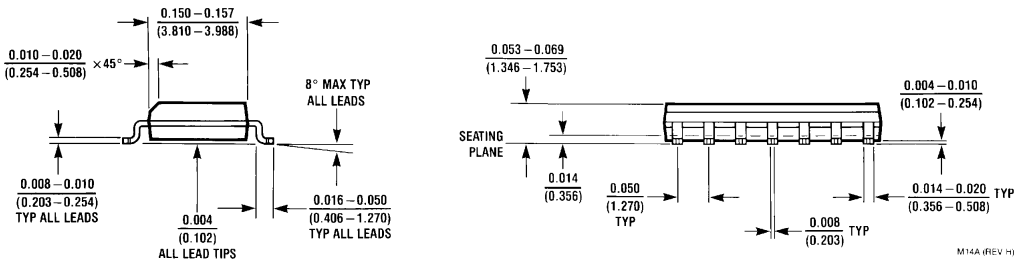
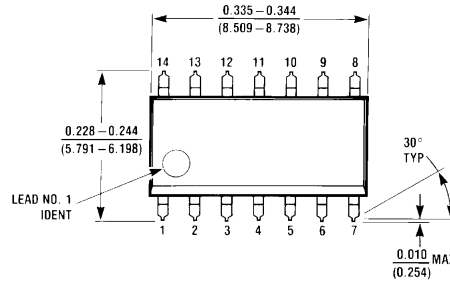
E20A (REV D)

**20-Lead Ceramic Leadless Chip Carrier (L)  
 NS Package Number E20A**

**Physical Dimensions** inches (millimeters) (Continued)

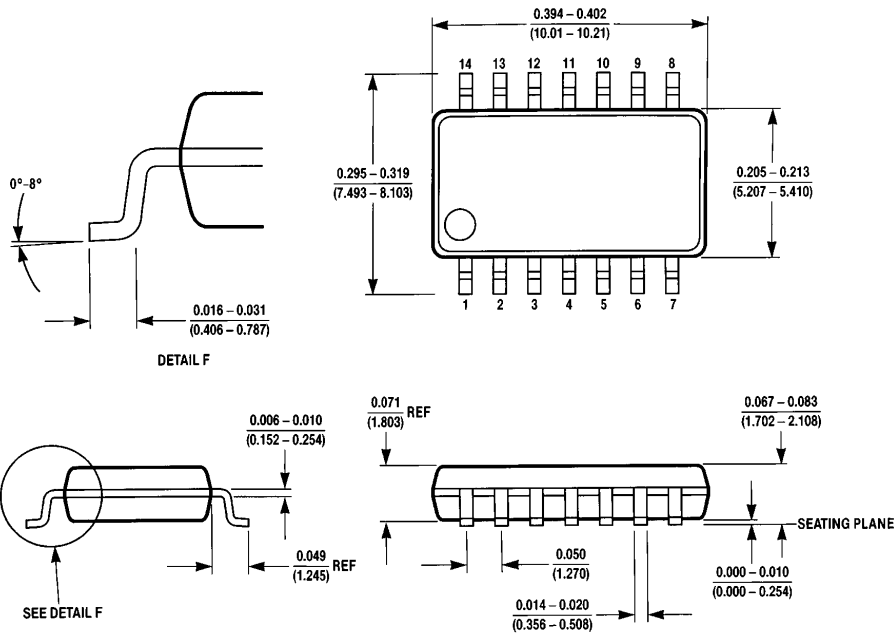


**14-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J14A



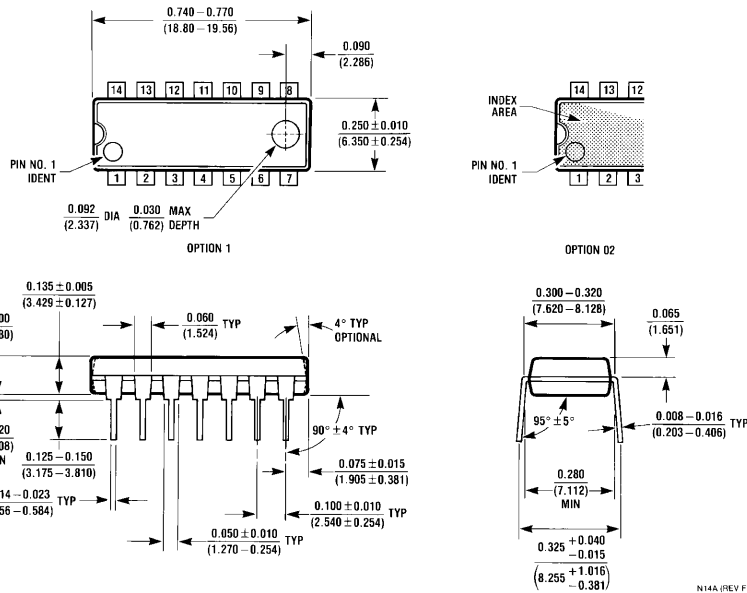
**14-Lead (0.150" Wide) Molded Small Outline, JEDEC (S)**  
NS Package Number M14A

**Physical Dimensions** inches (millimeters) (Continued)



M14D (REV A)

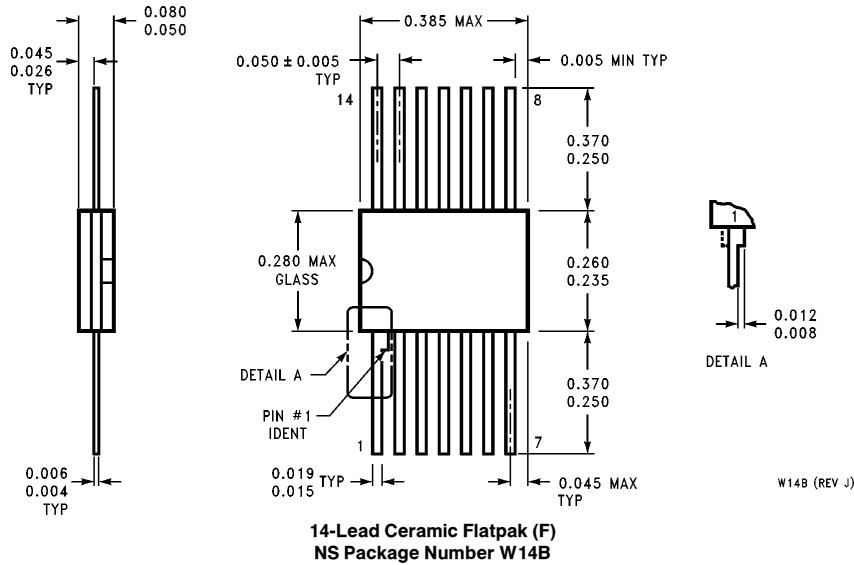
**14-Lead (0.300" Wide) Molded Small Outline, EIAJ (SJ)  
NS Package Number M14D**



N14A (REV F)

**14-Lead (0.300" Wide) Molded Dual-In-Line Package (P)  
NS Package Number N14A**

**Physical Dimensions** inches (millimeters) (Continued)



W14B (REV J)

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