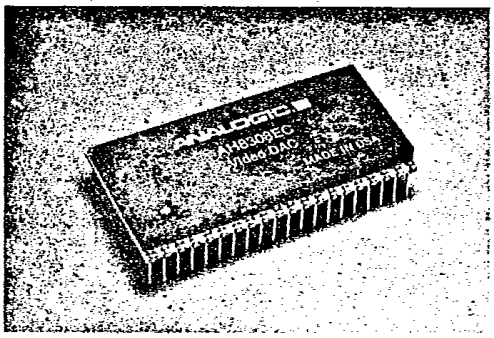


ANALOGIC®

AH8308EC

8-Bit RGB Video D/A Converter

Introduction

The **AH8308EC** is a third generation hybrid triple (RGB) 8-bit video DAC that provides designers of color display systems with a complete, self-contained, ECL-compatible RGB composite video subsystem in a 40-pin DIP. The **AH8308EC** features an advanced design that provides a low power (2.5W maximum), highly reliable and low cost video DAC. The small size of the **AH8308EC** reduces the PC board area by 30% or more for the equivalent function implemented with single channel DACs.

Each of three video DACs within the **AH8308EC** accepts 8-bit ECL data at an update rate of up to 150 MHz. Common Blanking and Strobe, and Sync (GREEN channel only) controls are provided. Blanking is synchronous with Strobe when activated, and asynchronous when deactivated. The video output for each channel is RS330/343 compatible, providing a 75Ω source impedance and a 1V p-p output signal.

The **AH8308EC** is a cost-effective solution to the requirement for a triple 8-bit composite video DAC in applications ranging from engineering workstations, to CAD/CAM systems, to medical imaging and other high-end graphics systems.

Features

- **Three 8-bit Video DACs in One 40-Pin DIP**
- **150 MHz Update Rate**
- **ECL Compatible**
- **Synchronous Blanking**
- **RS343/330 Composite Video Output Compatible**
- **Low Power Dissipation — 2.0W**

Applications

- **Color Graphic Workstations**
- **CAD/CAM Systems**
- **Medical Imaging Systems**
- **"Quick Look" Display Systems**
- **Image Processing Systems**

Operation

Each of the three DAC inputs is presented with an 8-bit data word corresponding to the intensity required for each CRT electron gun. After allowing for the data setup time, a high-to-low transition on the STROBE input causes the three 8-bit data words to be latched into the DACs. After the DAC propagation delay, each video output will produce a voltage corresponding to the data loaded into its DAC.

During the blanking interval, the BLANKING control line is activated by a logic 1. At the next STROBE pulse, the three DAC input registers are reset to 0000 0000 and the DAC outputs are driven to the blanking level. When the SYNC line is then activated (logic 1), the output of the GREEN channel is driven further negative to the sync level. When BLANKING (and SYNC) are deactivated at the end of the retrace interval, all three DAC outputs will remain at the Blanking level until the next STROBE pulse, when data present at the DAC inputs will be latched into their respective input registers, and will subsequently appear at the DAC outputs after the DAC propagation delay.

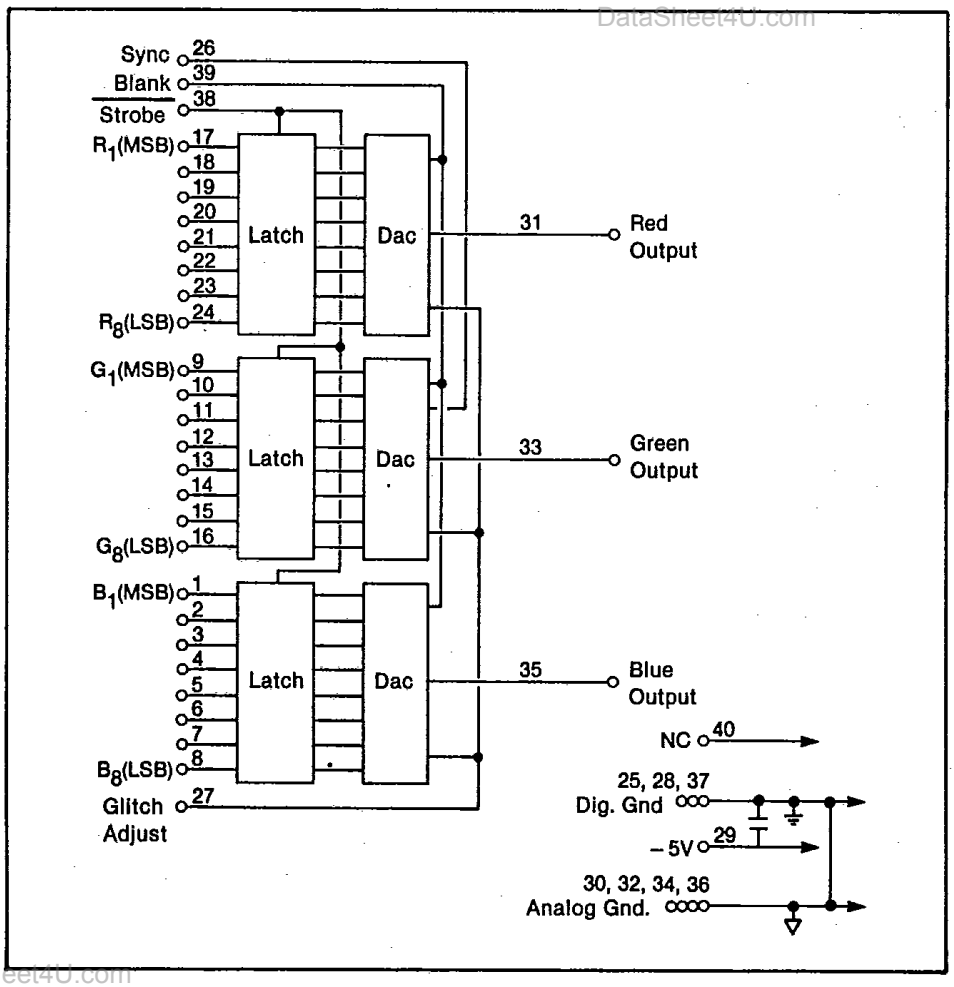


Figure 1. AH8308EC Block Diagram.

Specifications

(All specifications guaranteed at 25°C unless otherwise noted)

Output Characteristics (Each Channel)

Composite Output (GREEN Channel only)
0V to −1.00V, ±3% of full scale into 75Ω termination

Gray Scale Output (all Channels)
0V to −0.643V, ±3% of Gray Scale into 75Ω termination

Recommended Load Impedance
75Ω, ±5%, dc to 50 MHz

Source (Thevenin) Impedance
75Ω, ±5%, dc to 50 MHz

LSB Size
2.5 mV, nominal

Rise and Fall Time
3 ns typical, 4 ns maximum; 10% to 90%

Full-Step Settling Time
7.5 ns typical to 1 LSB (0.4%)

Glitch Settling Time
5 ns to <1 LSB for worst case transition

Glitch Area
80 pV-s typical

Cable Drive Capacity
75Ω characteristic impedance; to avoid appreciable signal loss, total length should have no more than 7.5Ω dc resistance

Composite Sync Level (GREEN Channel Only)
−1.00V absolute, −0.286V (−40 IRE Units) relative to Blanking level

Composite Blanking Level
−0.714V

Transfer Characteristics (Each Channel)

Resolution
8 bits, 256 Gray Scale levels; 2.5 mV per step, nominal

Coding
Binary

Reference White Level
1111 1111 produces 0V absolute; +0.714V (100 IRE Units) relative to Blanking level

Reference Black Level
0000 0000 produces −0.643V absolute; +0.071V (10 IRE Units) relative to Blanking level

Differential Linearity
±1/2 LSB maximum

Monotonicity
Guaranteed

Offset (Output with 1111 1111 Input)
±1/2 LSB maximum, 0°C to +55°C

Propagation Delay
7 ns typical, strobe to output; 50% points

Control Input Speed (SYNC, and BLANKING)
7 ns typical, 10 ns maximum to settle to 10% of final value

Channel-to-Channel Crosstalk
1/2 LSB maximum, dc component 100 pV-s maximum, ac component

Input Characteristics (Each Channel)

Logic Levels (all inputs)
10K Series ECL levels
Logic 0 = −1.75V
Logic 1 = −0.9V

Loading (All inputs)
5 pF; open transistor base; open input is logic "0"

Data Validity
Data must be valid 2.0 ns prior to Strobe and remain valid for 1.5 ns after data Strobe

Update Rate
150 MHz maximum

Common Control Inputs

Strobe Input
Data entered on negative-going edge (Timing Reference) on all three channels simultaneously

Skew
5 ns maximum variation between channels for data latched into input registers

Pulse Width
5.0 ns minimum

Rise and Fall Time
<10 ns (10% to 90%)

Composite Blanking
Logic 1 on Blanking input simultaneously resets all input registers to 0000 0000, and drives all channel outputs to −0.714V; Blanking is synchronous with falling edge of next STROBE pulse; after logic 1 to 0 transition, all channel outputs will remain at the Blanking level until next STROBE pulse, at which time data present at DAC inputs is loaded into the DAC

Composite Sync
Logic 1 on SYNC input (after Blanking is activated) drives the GREEN channel output further negative to −1.00V; if activated without BLANKING, at next STROBE pulse, control resets all registers to 0000 0000, drives the RED and BLUE channels to Blanking level (−0.714V) and GREEN channel output to −1.00V; when SYNC is released (returned to logic 0), all channel outputs will remain at the Blanking level until the next STROBE pulse which will load the data present at the inputs into the DACs (assuming BLANKING control is inactive)

Glitch Adjust Input Impedance
7.5 kΩ

Control Characteristics
75 pV-s/V applied to Glitch Adjust pin

Power Supply Requirements

−5.0V
500 mA maximum; 5 mV p-p ripple maximum (−4.75V to −5.5V operating range)

Power Dissipation
2.0 watts typical, 2.5 watts maximum

Environmental and Mechanical

Operating Temperature Range
0°C to +70°C

Storage Temperature
−25°C to +100°C

Relative Humidity
0 to 85%, non-condensing up to +40°C

Mechanical Dimensions
2.0" x 1.0" x 0.3"; 40-pin triple width DIP

Using the AH8308EC

Power Supply Requirements

The **AH8308EC** requires a −5V power supply. The output amplitudes specified are nominal values based on a −5.0V supply and will change in direct proportion to the −5.0V supply voltage.

The glitch area will also vary as a function of the −5V supply voltage. The factory trim is normally carried out at −5.0V and may be done at another voltage if specified when ordering.

If other than −5.0V (measured directly at pin 29) is used with a unit trimmed for −5.0V operation, provisions should be made on the PC board for a 10 kΩ potentiometer connected to the GLITCH ADJUST pin (pin 27) as shown in Figure 2. The pot should be adjusted to reduce the glitch area to a minimum.

Grounding

There are seven (7) ground pins all tied together internally via ground plane. To reduce ground loops, each ground pin should be used for the function for which it is labelled.

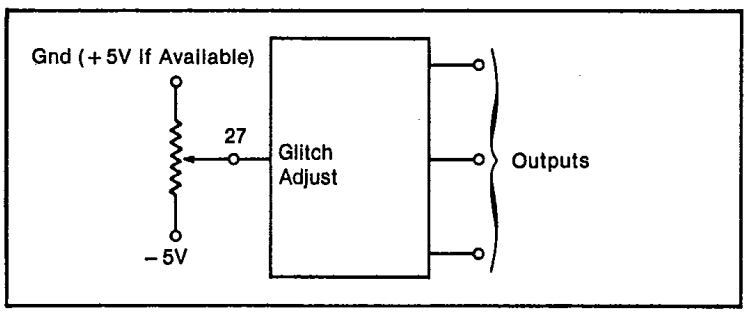
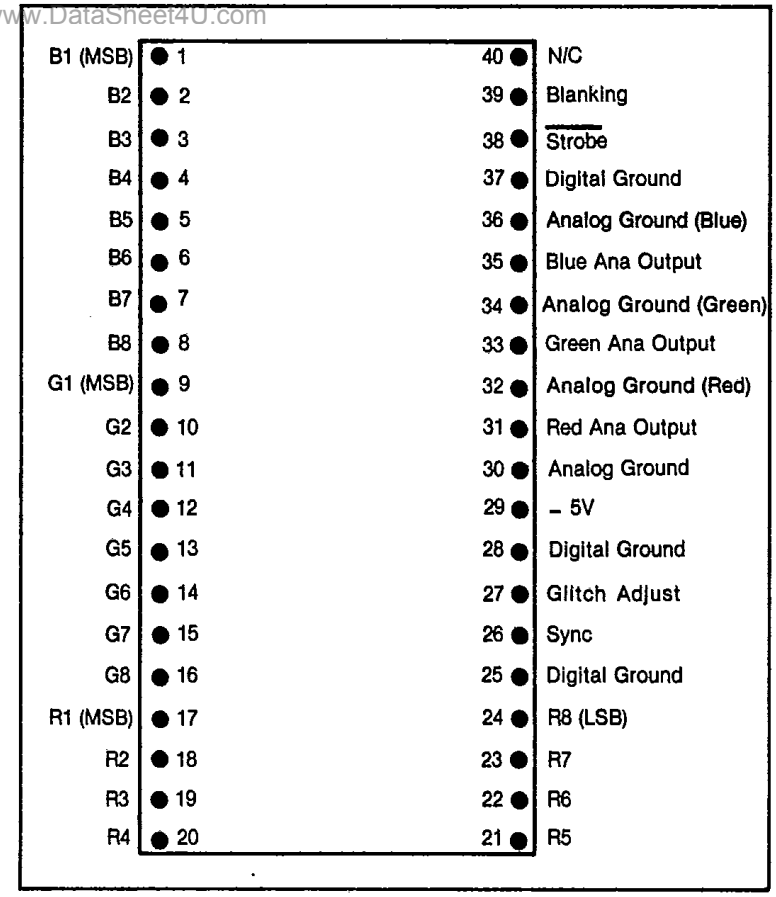
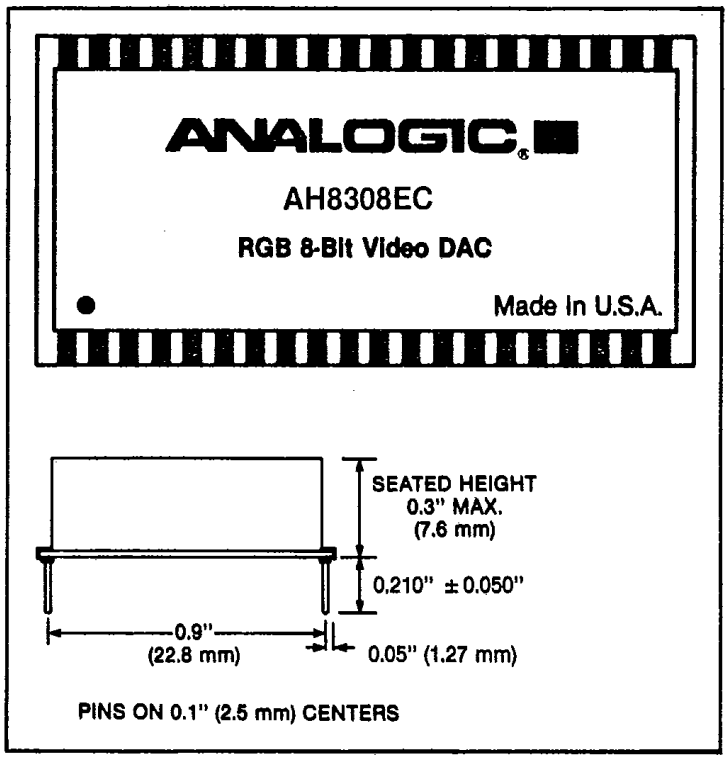


Figure 2. Glitch Adjust.

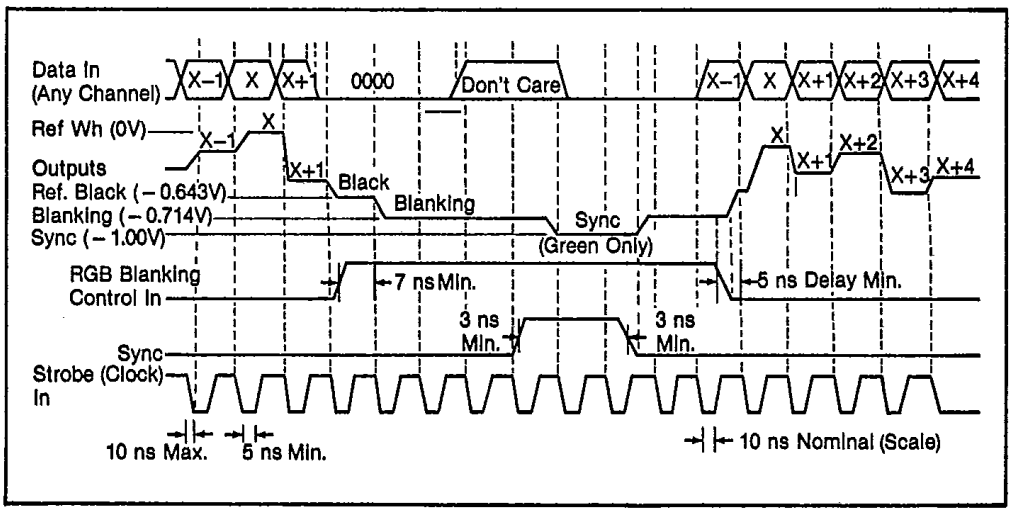


All ground pins (25, 28, 30, 32, 34, 36, and 37) are connected via ground plane. However, to reduce loops each ground should be used as it is functionally labelled.

Pinout



Mechanical



AH8308EC Typical Timing

Ordering Guide

150 MHz, RGB 8-bit
video DAC.....specify AH8308EC