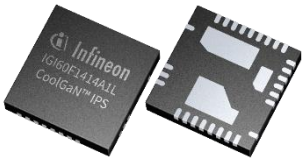
CoolGaN™ Integrated Power Stage (IPS) IGI60F2020A1L

200 mΩ / 600 V GaN half-bridge with fast accurate isolated gate drivers

Features



- Two 200 mΩ GaN switches in half-bridge configuration with dedicated high- and low-side isolated gate drivers
  - Source / sink driving current up to 1 / 2 A
  - Application-configurable turn-on and turn-off speed
- Fast input-to-output propagation (typ. 47 ns) with extremely small channel-to-channel mismatch
- PWM input signal (switching frequency up to 3 MHz)
- Standard logic input levels compatible with digital controllers
- Wide supply range
- Single gate driver supply voltage possible (typ. 8 V) with fast UVLO recovery
- Low-side open source for current sensing with external shunt resistor
- Galvanic input-to-output isolation based on robust coreless transformer technology
- Gate driver with very high common mode transient immunity (CMTI) > 300 V/ns
- Thermally enhanced 8 x 8 mm QFN-28 package
- Product is fully qualified acc. to JEDEC for Industrial Applications

Description

IGI60F2020A1L combines a half-bridge power stage consisting of two 200 mΩ (typ. R_{dson}) / 600 V enhancement-mode CoolGaN™ HEMTs with dedicated gate drivers in a small 8 x 8 mm QFN-28 package. In the low-to-medium power area (example application in **Figure 1**) it is thus ideally suited to support the design of high-density AC/DC chargers and adapters utilizing the superior switching behavior of CoolGaN™ HEMTs.
Infineon's CoolGaN™ and related power switches provide a very robust gate structure. When driven by a continuous gate current of a few mA in the "on" state, a minimum on-resistance R_{dson} is always guaranteed.

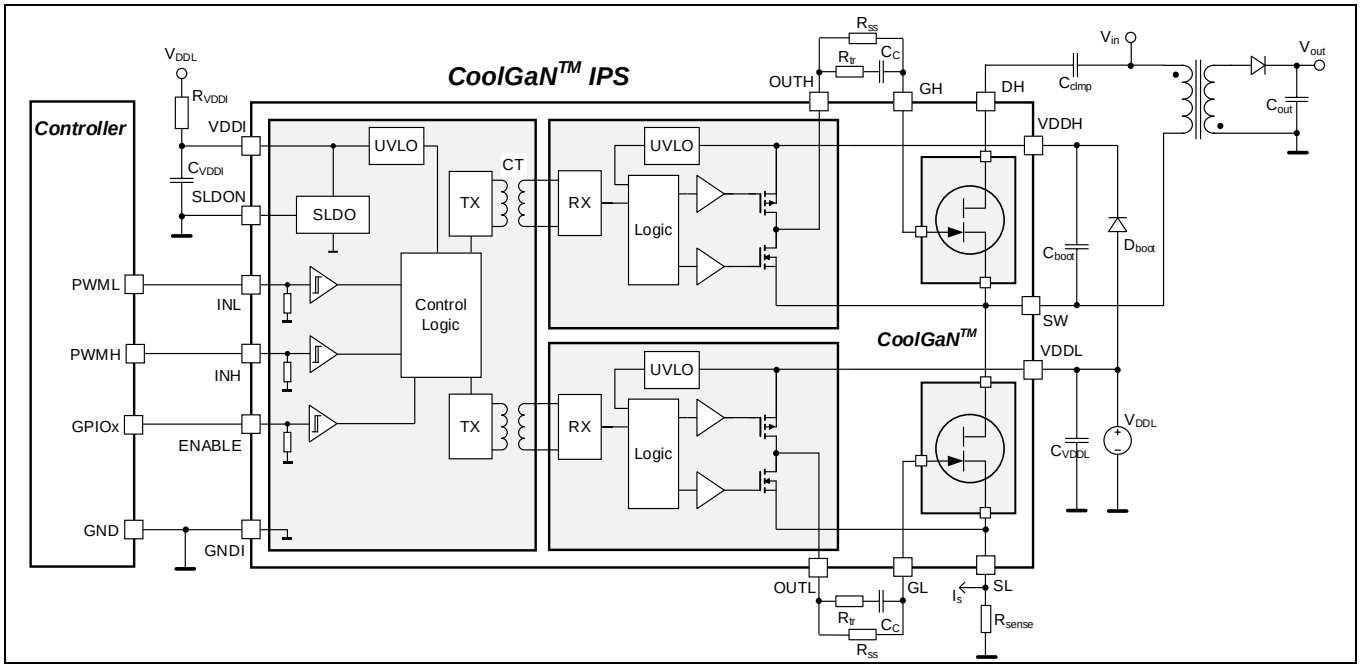


Figure 1 Typical application circuit (active clamp flyback converter)

Due to the GaN-specific low threshold voltage and the fast switching transients, a negative gate drive voltage is required in certain applications to both enable fast turn-off and avoid cross-conduction effects. This can be achieved by the well-known RC interface between driver and switch. A few external SMD resistors and caps enable easy adaptation to different power topologies.
The driver utilizes on-chip coreless transformer technology (CT) to achieve signal level-shifting to the high-side. Further, CT guarantees robustness even for extremely fast switching transients above 300 V/ns.

Applications

- Charger and adaptors
- Server, telecom & networking SMPS
- Low power motor drive
- LED lighting

Power Topologies

- Active clamp flyback or hybrid flyback converters
- LLC or LCC resonant converters
- Single or interleaved synchronous buck or boost converter
- Single phase or multiphase two-level inverters

Product Versions

Table 1 CoolGaN™ integrated power stage half bridge products overview

Part Number / Ordering code	OPN	Package	Typ. R_{dson} high- / low-side	Marking
IGI60F1414A1L	IGI60F1414A1L AUMA1	PG-TIQFN-28-1 8 x 8 mm	140 mΩ / 140 mΩ	60F1414A
IGI60F2020A1L	IGI60F2020A1L AUMA1	PG-TIQFN-28-1 8 x 8 mm	200 mΩ / 200 mΩ	60F2020A
IGI60F2727A1L	IGI60F2727A1L AUMA1	PG-TIQFN-28-1 8 x 8 mm	270 mΩ / 270 mΩ	60F2727A
IGI60F5050A1L	IGI60F5050A1L AUMA1	PG-TIQFN-28-1 8 x 8 mm	500 mΩ / 500 mΩ	60F5050A

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1 Pin configuration and description

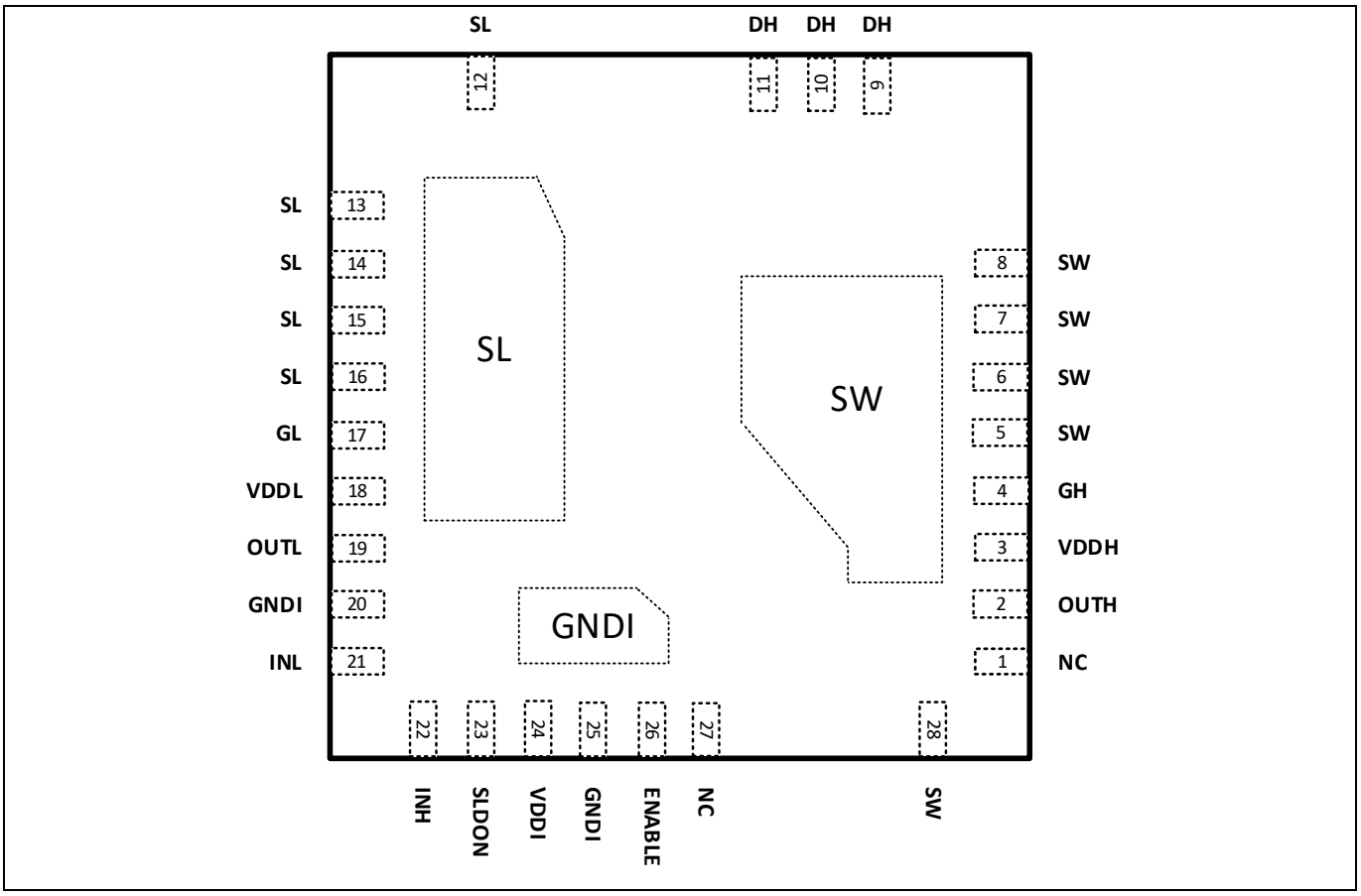


Figure 2 Pin configuration and exposed pads for QFN-28 8 x 8 mm package, top view (not to scale)

Table 2 Pin description

Pin No.	Symbol	Description
1	NC	Not connected
2	OUTH	Driver output high-side
3	VDDH	Supply voltage for high-side driver (typ. 8 V referred to SW)
4	GH	Gate connection high-side switch
5 – 8, 28	SW	Half-bridge output (switching node)
9 - 11	DH	Drain connection high-side switch
12 - 16	SL	Source connection low-side switch
17	GL	Gate connection low-side switch
18	VDDL	Supply voltage for low-side driver (typ. 8 V referred to SL)
19	OUTL	Driver output low-side
20, 25	GNDI	Ground connection of driver input stage

21	INL	Input signal (default state “Low”); controls low-side switch
22	INH	Input signal (default state “Low”); controls high-side switch
23	SLDON	Connected to VDDI (or not connected): VDDI directly supplies driver input circuitry Connected to GNDI: Internal shunt regulator activated to generate VDDI (3.3 V)
24	VDDI	Supply voltage driver input stage (+3.3 V); can be either applied directly or generated by internal SLDO (e.g by connecting VDDI via resistor R_{VDDI} to VDDL)
26	ENABLE	Input signal (default state “Low” - both outputs set to low state); logic “High” required to activate outputs
27	NC	Not connected

2 Functional description

2.1 Block Diagram

A simplified functional block diagram of the CoolGaN™ Power Stage is given in **Figure 3**. For the level-shifting function of the input signal to the high-side switch an on-chip coreless transformer (CT) is utilized. For symmetry reasons a CT is also included in the low-side path, resulting in both a galvanic input-to-output and high-to-low-side isolation. In addition, this CT separates the low-side gate driver reference (SL) from GNDI allowing to use a shunt resistor for current sensing as shown in **Figure 1**.

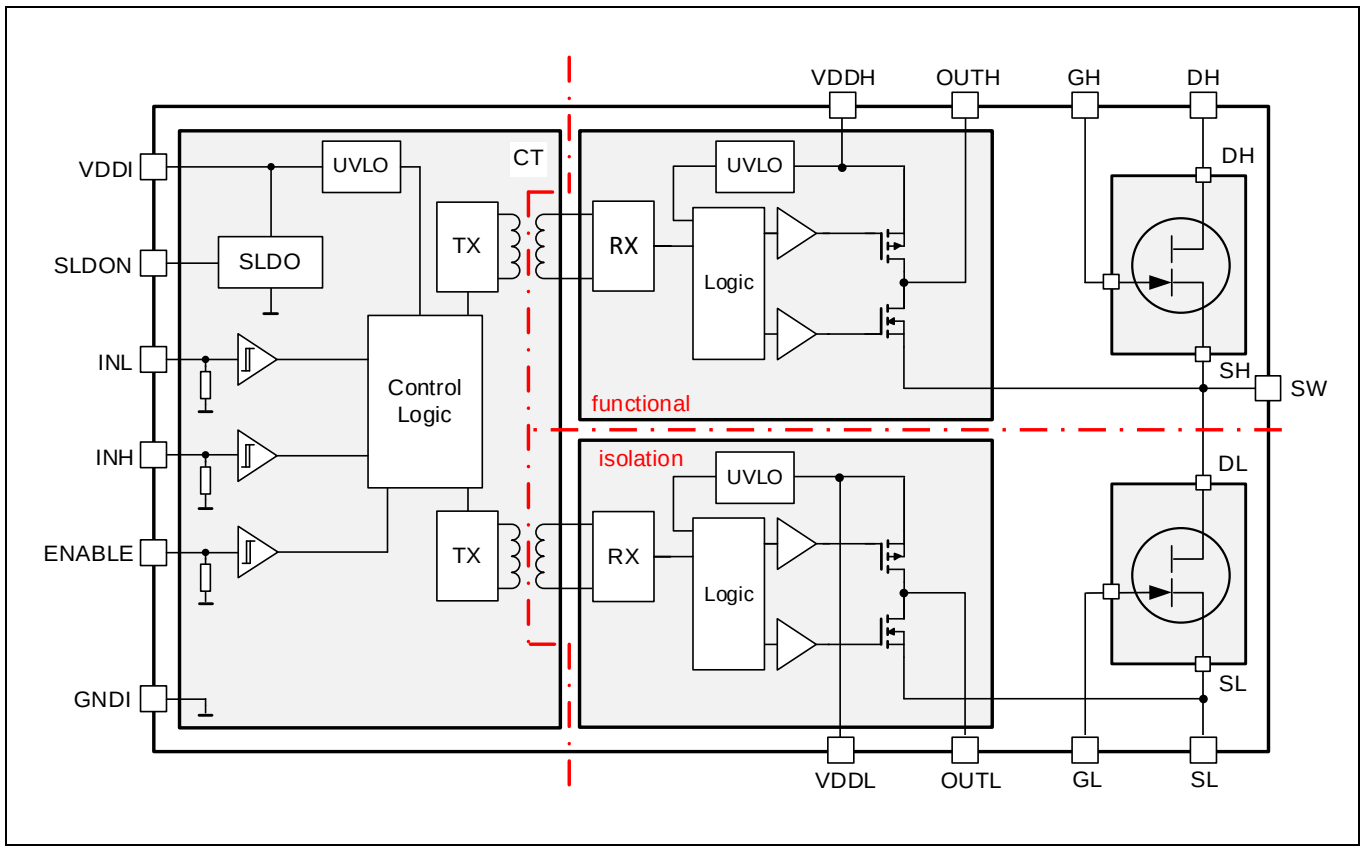


Figure 3 Block Diagram IGI60F2020A1L

2.2 Power supply

Basically, the Power Stage requires 3 supply voltages: a ground-related 3.3 V (V_{DDI}) for the driver input circuitry, another ground-related 8 V (V_{DDL}) for the low-side driver and a floating 8 V (V_{DDH}) for the high-side driver. However, in most applications a single 8 V supply is sufficient, as V_{DDI} and V_{DDH} can be simply generated from V_{DDL}. Independent Undervoltage Lockout (UVLO) functions for all supply voltages ensure a defined start-up and robust functionality under all operating conditions.

All driver supply currents stay in the few mA range, as described in **Table 9**, resp. However, in particular applications a further power reduction in stand-by mode might be beneficial. Then a complete elimination of the supply currents can be achieved by implementing a simple circuit with a bipolar transistor as a supply switch controlled by the Enable signal.

2.2.1 Driver input supply voltage

The driver input die is supplied via V_{DDI} with a nominal voltage of 3.3 V. The Undervoltage Lockout threshold, defining the minimum V_{DDI}, is set to typically 2.85 V. Power consumption to some extent depends on switching frequency, as the input signal is converted into a train of repetitive current pulses to drive the CT. Due to the chosen robust encoding scheme the average repetition rate of these pulses and thus the average supply current depends on the switching frequency f_{sw}. However, for f_{sw} < 500 kHz this effect is very small.

If no separate 3.3 V supply is available, the input side can also be operated with V_{DDL} (typically 8 V). Then the shunt LDO voltage regulator (SLDO) has to be enabled by connecting pin SLDON (pin#23) to GNDI. The SLDO regulates the current through an external resistor R_{VDDI} connected between V_{DDL} and pin VDDI as depicted in **Figure 1** to generate the required voltage drop. For proper operation it has to be ensured that the current through R_{VDDI} always exceeds the maximum supply current I_{VDDI} of the input chip; but not too small to casue a high power dissipation and significant impact on the total system efficiency. R_{VDDI} thus has to fulfil:

$$R_{VDDI} < \frac{V_{DDL,min} - 3.3\ V}{I_{VDDI,max}} \quad (1)$$

A typical choice for V_{DDL} = 8 V would be R_{VDDI} = 1 kΩ, resulting in sufficient margin between resistor current and maximum operating current. Dynamic current peaks are provided by a blocking cap (10 to 22 nF) between V_{DDI} and GNDI. **Table 3** shows proper R_{VDDI} values for different supply voltages V_{DDL}.

Table 3 Proper R_{VDDI} values for different V_{DDL}

V_{DDL}	R_{VDDI}	SLDO
3.3 V	no resistor (connect VDDL to VDDI pin)	Disabled
5.0 V	360 Ω	Enabled
8.0 V	1.0 kΩ	Enabled
12.0 V	1.8 kΩ	Enabled

2.2.2 Driver output supply voltages

Both output dice have to be supplied by a voltage of typically 8 V related to the source of the respective GaN switch. In many applications the floating high-side supply V_{DDH} can be generated from the ground-related V_{DDL} by means of bootstrapping (components D_{boot}, C_{boot} and R_{boot} in **Figure 1**). A ceramic bypass capacitance C_{VDDL} of typically 100 nF has to be placed close to pin VDDL.

For both driver output stages the minimum operating supply voltage is set by independent undervoltage lockout functions ($UVLO_{out}$).

2.3 Input configurations

The inputs INL and INH are two independent logic (PWM) channels. The input signal is transferred non-inverted to the corresponding gate driver outputs OUTL and OUTH. All inputs are compatible with LV-TTL threshold levels with a hysteresis of typ. 0.8 V. The hysteresis is independent of the supply voltage VDDI.

The PWM inputs are internally pulled down to a logic low voltage level (GNDI). In case the PWM-controller signals have an undefined state during the power-up sequence, the gate driver outputs are forced to the "off"-state (low). If the Enable input is low, both channel outputs are driven to “low”, regardless of the state of INL or INH. **Table 4** shows the logic table in normal operation.

Table 4 Logic table (UVLO input inactive, both output side UVLO inactive; normal operation)

Inputs			Gate Drive Ouput	
Enable	**INL**	**INH**	**OUTL**	**OUTH**
L	x	x	L	L
H	L	L	L	L
H	L	H	L	H
H	H	L	H	L
H	H	H	H	H

2.4 Driver outputs

The rail-to-rail gate driver output stage realized with complementary MOS transistors is able to provide a typical 1 A sourcing and 2 A sinking current. This is by far sufficient when driving the GaN HEMTs due to their low gate charge. In addition, the relatively low driver output resistance is beneficial, too. With an R_{on} of 3.1 Ω for the sourcing pMOS and 1.2 Ω for the sinking nMOS transistor the driver can be considered as nearly ideal. The gate drive parameters can thus be determined easily and accurately by the external components as described in chapter 4. The p-channel sourcing transistor allows real rail-to-rail behavior without suffering from a source follower's voltage drop.

2.5 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the gate drive outputs can be switched to their high level only, if both input and output supply voltages exceed the corresponding UVLO threshold voltages. Thus it can be guaranteed, that the GaN switches are in “off” state, if the driving voltage is too low for complete and fast switching on, thereby avoiding excessive power dissipation and keeping the switch transistors within their safe operating area (SOA).

The UVLO levels for the output supplies V_{DDL} and V_{DDH} are set to a typical “on”-value of 4.2 V (with 0.3 V hysteresis), whereas $UVLO_{in}$ for V_{DDI} is set to 2.85 V with 0.15 V hysteresis. **Table 5** shows the logic table in the condition that input or outputs are in UVLO active or inactive condition.

Table 5 Logic table (dependence on UVLO status)

Inputs						Gate Drive Ouput	
Enable	**INL**	**INH**	**UVLO input**	**UVLO output L**	**UVLO output H**	**OUTL**	**OUTH**
x	x	x	Active	x	x	L	L
H	x	L	Inactive	Active	Inactive	L	L
H	x	H	Inactive	Active	Inactive	L	H
H	L	x	Inactive	Inactive	Active	L	L
H	H	x	Inactive	Inactive	Active	H	L

2.6 Start-up and active clamping

Special attention has been paid to cover all possible operating conditions, like start-up or arbitrary supply voltage situations:

- if V_{DDI} drops below $UVLO_{in}$, a “switch-to-low” command is sent to both outputs OUTL and OUTH
- for V_{DDL} and/or V_{DDH} lower than the respective UVLO levels, a new fast active clamping circuit provides a low-impedance path from the gate driver outputs OUTL and OUTH to their respective grounds SL and SW. As soon as the output voltage exceeds a low threshold level (typically below 1 V), the clamp is activated within approximately 20 ns.

As the result, safe operation of the GaN Power Stage can be guaranteed under any circumstances.

2.7 CT Communication and Data Transmission

A Coreless Transformer (CT) based communication module is used for PWM signal transfer between input and outputs. A proven high-resolution pulse repetition scheme in the transmitter combined with a watchdog time-out at the receiver side enables recovery from communication fails and ensures safe system shut-down in failure cases.

2.8 CoolGaN™ output stage

The output stage consists of two CoolGaN™ 600V switches in half-bridge configuration. The switches are characterized by a typical R_{dson} of 200 mΩ @ 25 °C. And thanks to the current driving concept, this value increases by a comparably moderate 85 % @ 150 °C. As typical for GaN, gate and output charges are very small (3 and 16 nC, resp.) and there is no reverse recovery charge due to the lack of a physical body diode (for more information please refer to [1]).

3 Characteristics

3.1 Absolute maximum ratings

The absolute maximum ratings are listed in **Table 6**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note or Test Conditions
		Min.	Max.		
Voltage between output pins DH, SW and SL	V_{DHSW}	-	600	V	
	V_{SWSL}	-	600	V	V_{GHSH} = 0 V, V_{GLSL} = 0 V
Drain-to-source voltage pulsed	$V_{DS,pulse}$	-	750[1]	V	T_J = 25°C, V_{GS} ≤ 0 V, cumulated stress time ≤ 1h
		-	650	V	T_J = 125°C, V_{GS} ≤ 0 V, cumulated stress time ≤ 1h
Continuous drain current	I_D	-	5.0	A	T_{Case} = 25°C
		-	3.7	A	T_{Case} = 125°C
Pulsed drain current[2]	$I_{D,pulse}$	-	14.1	A	T_{Case} = 25°C (see **Figure 13**)
		-	7.7[3]	A	T_{Case} = 125°C (see **Figure 13**)
Supply voltage input chip	V_{DDI}	-0.3	3.7	V	Note[4]
Supply voltage output chips	$V_{DDL/H}$	-0.3	22	V	with respect to SW/SL
Voltage at pins INL, INH and ENABLE	V_{IN}	-0.3	17	V	
Voltage at pin SLDO	V_{SLDO}	-0.3	V_{DDI} + 0.3	V	
Voltage at pins OUTL, OUTH	$V_{OUTL/H}$	-0.3	$V_{DDL/H}$ + 0.3	V	
Junction temperature	T_J	- 40	150	°C	
Storage temperature	T_S	- 55	150	°C	
Soldering temperature	T_{sold}	-	260	°C	reflow/wave soldering[5]

[1] Acc to JEDEC-JEP180

[2] Limits derived from product characterization, parameter not measured during production

[3] Parameter is influenced by reliability requirements. Please contact the local Infineon Sales Office to get an assessment of your application

[4] If the SLDO is activated (SLDON pin tied to GNDI), the input-side supply voltage (VDDL) does not correspond to VDDI and can be higher

[5] Acc. to JESD22A111

Parameter	Symbol	Values		Unit	Note or Test Conditions
		Min.	Max.		
ESD capability	V_{ESD_HBM}	-	2	kV	Human Body Model[1]
	V_{ESD_CDM}	-	1.0	kV	Charged Device Model[2]

3.2 Thermal characteristics

Table 7 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Thermal resistance junction-case	R_{thJC}	-	-	3.0	°C/W	
Thermal resistance junction-ambient	R_{thJA}	-	35	-	°C/W	Device mounted on four-layer PCB with 600 mm² total cooling area

3.3 Recommended operating range

Table 8 Recommended operating range

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	3	3.3	3.5	V	if operated directly without SLDO
Driver output supply voltages	$V_{DDL/H}$	5.5	8	12	V	min. defined by $UVLO_{out}$
VDDI blocking capacitance	C_{VDDI}	10	-	22	nF	SLDO active
Logic input voltage at pins INL, INH and ENABLE	V_{IN}	0	-	6.5	V	
Voltage at pin SLDO	V_{SLDO}	0	-	3.5	V	
Gate current, continuous[3] [4]	$I_{G, avg}$	-	-	6.9	mA	
Junction temperature	T_J	-40	-	125 [5]	°C	

[1] Acc. to EIA/JESD22-A114-B (discharging 100 pF capacitor through 1.5 kΩ resistor)

[2] Acc. to JESD22-002

[3] Parameter is influenced by rel-requirements. Contact the local Infineon Sales Office to get an assessment of your application.

[4] We recommend to use RC interface gate drive to optimize the device performance. Please see gate drive application note for details.

[5] Continuous operation above 125°C may reduce lifetime

3.4 Electrical characteristics

Unless otherwise noted, min/max values of characteristics are the lower and upper limits, resp. They are valid within the full operating range. All values are given at T_J = 25 °C with V_{DDI} = 3.3 V and $V_{DDL/H}$ = 8 V.

Table 9 Power supply

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
V_{DDI} quiescent current[1]	I_{VDDIqu}	-	1.4	-	mA	no switching
V_{DDL} quiescent current[1]	I_{VDDLqu}	-	0.7	-	mA	no switching
V_{DDH} quiescent current[1]	I_{VDDHqu}	-	0.7	-	mA	no switching
Undervoltage Lockout input ($UVLO_{VDDI}$) turn-on threshold	$UVLO_{VDDI}$	2.75	2.85	2.95	V	
$UVLO_{VDDI}$ turn-off threshold	$UVLO_{VDDI-}$	-	2.7	-	V	
$UVLO_{VDDI}$ threshold hysteresis	$\Delta UVLO_{VDDI}$	0.1	0.15	0.2	V	
Undervoltage Lockout outputs ($UVLO_{VDDL/H}$) turn-on threshold	$UVLO_{outLH}$	4.0	4.2	4.4	V	
$UVLO_{VDDL/H}$ turn-off threshold	$UVLO_{VDDL/H\ -}$	-	3.9	-	V	
$UVLO_{VDDL/H}$ threshold hysteresis	$\Delta UVLO_{VDDL/H}$	0.2	0.3	0.4	V	

Table 10 Logic inputs INL, INH and ENABLE

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{IN+}	1.7	2.0	2.3	V	independent of V_{DDI}
Input voltage threshold for transition HL	V_{IN-}	-	1.2	-	V	independent of V_{DDI}
Input voltage threshold hysteresis	V_{IN_hys}	0.4	0.8	1.2	V	
Input pull down resistor	R_{IN}	-	150	-	kΩ	

[1] Can be completely eliminated in stand-by mode by utilizing external supply switch (see chapter 2.2)

Table 11 Static gate driver output characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
High-level (sourcing) output resistance	R_{on}	1.4	3.1	5.8	Ω	
Peak sourcing output current[1]	$I_{src,pk}$	-	1	-	A	actively limited to 1.3 A
Low-level (sinking) output resistance	R_{off}	0.6	1.2	2.5	Ω	
Peak sinking output current[1]	$I_{snk,pk}$	-	-2	-	A	actively limited to -2.6 A
Active clamp threshold voltage	V_{clmp}	-	1	-	V	

Table 12 Output characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
R_{dson} high-side	R_{dshs}	-	200	260	mΩ	I_G = 6.9 mA, I_D = 2.1 A, T_J = 25°C
		-	360	-	mΩ	I_G = 6.9 mA, I_D = 2.1 A, T_J = 150°C
R_{dson} low-side	R_{dsls}	-	200	260	mΩ	I_G = 6.9 mA, I_D = 2.1 A, T_J = 25°C
		-	360	-	mΩ	I_G = 6.9 mA, I_D = 2.1 A, T_J = 150°C
Drain-source leakage current	I_{DSShs}, I_{DSSls}	-	0.26	-	µA	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 25°C
		-	5.3	-	µA	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 25°C
Total gate charge (per switch) [1]	Q_G	-	1.5	-	nC	I_G = 0 to 2.6 mA, V_{DH} = 400 V, I_D = 2.1 A

[1]Verified by design / characterization, not tested in production

Table 13 Static characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 0.7	1.2 1.0	1.6 1.4	V V	I_{DS} = 0.69 mA, V_{DS} = 10 V, T_j =25 °C I_{DS} = 0.69 mA, V_{DS} = 10 V, T_j=125°C
Gate-source reverse clamping voltage	$V_{GS,\ clamp}$	-	-	-8	V	I_{GSS}[1] = -1 mA, T_j =25 °C
Gate resistance	$R_{G,int}$	-	0.80	-	Ω	LCR impedance measurement

Table 14 Dynamic characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	100	-	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1MHz
Output capacitance	C_{oss}	-	19.0	-	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1MHz
Reverse transfer capacitance	C_{rss}	-	0.1	-	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1MHz
Effective output capacitance, energy related[2]	$C_{o(er)}$	-	21.1	-	pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Effective output capacitance, time related[3]	$C_{o(tr)}$	-	27.1	-	pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Output charge	Q_{oss}	-	10.8	-	nC	V_{DS} = 0 to 400 V

1 Gate-Source leakage current

2 $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

3 $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 15 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	VSD	-	2.2	2.5	V	V_{GS} = 0V, I_{SD} = 2.1 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	15.8	A	I_G = 6.9 mA
Reverse recovery charge	Q_{rr}[1]	-	0	-	nC	I_{SD} = 2.1 A, V_{DS} = 400V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

Table 16 Dynamic Characteristics[2] (see Figure 4, Figure 5)

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
INL to SW propagation delay “on”	t_{PDonL}	-	47	-	ns	R_{tr} = 50 Ω
INL to SW propagation delay “off”	t_{PDoffL}	-	47	-	ns	I_{load} = 2 A
Propagation delay matching high/low-side	Δt_{PDonLH} $\Delta t_{PDoffLH}$	-5 -5	- -	5 5	ns ns	
ENABLE to SW propagation delay	$t_{PD\_DIS\_ON}$, $t_{PD\_DIS\_OFF}$	-	70 70	-	ns ns	
Rise time SW	t_{rise}	-	6	-	ns	10 % to 90 %
Fall time SW	t_{fall}	-	5	-	ns	90 % to 10 %
Minimum input pulse width that changes output state	t_{PW}	-	18	-	ns	-
Input-side start-up time[2]	$t_{START,VDDI}$	-	7	-	µs	see **Figure 6**
Input-side deactivation time[2]	$t_{STOP,VDDI}$	-	255	-	ns	see **Figure 6**
Input-side deactivation time[2]	$t_{START,VDDL/H}$	-	5	-	ns	see **Figure 6**
Output-side deactivation time[2]	$t_{STOP,VDDL/H}$	-	110	-	ns	see **Figure 6**

[1] Excluding Q_{oss}

[2] Verified by design / characterization, not tested in production

Table 17 Isolation specifications

Parameter		Symbol	Value	Unit	Note or Test Conditions
Functional isolation	Max. Input-to-DH voltage	V_{InDH}	>1200	V_{DC}	production test > 10 ms
	Max. Input-to-SW voltage	V_{InSW}	>600	V_{DC}	
	Max. Input-to-SL voltage	V_{InSL}	>100	V_{DC}	
Package characteristics	Nominal package clearance	CLR	1.9	mm	shortest distance over air, from any input pin to any high-side output pin
	Nominal package creepage	CRP	1.9	mm	shortest distance over surface, from any input pin to any high-side output pin
	Comparative Tracking Index of package mold	CTI	>400	V	according to DIN EN 60112 (VDE 0303-11)
	Material group	-	II	-	according to IEC 60112
Common Mode Transient Immunity (CMTI)	Static Common Mode Transient Immunity[1,2]	$\lvert CM_{Static,H} \rvert$	300	V/ns	V_{CM} = 1500 V; INL, INH tied to V_{DDI} (logic high inputs)
		$\lvert CM_{Static,L} \rvert$	300	V/ns	V_{CM} = 1500 V; INL, INH tied to GNDI (logic high inputs)
	Dynamic Common Mode Transient Immunity[1,3]	$\lvert CM_{Dynamic} \rvert$	300	V/ns	V_{CM} = 1500 V; dynamic INL, INH (10 MHz square wave)

[1] minimum slew rate of a common mode voltage at which the output signal is disturbed

[2] parameters verified by characterization according to VDE0884-11 standard definitions and test-methods

[3] verified by characterization with ground reference for the common mode pulse generator connected to the coupler intput-side ground to reflect real applications requirements

3.5 Timing diagrams and test circuit

Figure 4 depicts rise, fall and delay times measured at the GaN half-bridge output SW. **Figure 5** shows the associated test circuit. The power stage is operated in a boost configuration at a constant current I_{load}. In this so-called double-pulse arrangement I_{load} is determined by the high-voltage supply (400 V), the output inductance and the length of the first “on”-phase of the INL-signal. The specified delay and transient times are related to an I_{load} value of 2 A (particularly the “off” transient strongly depends on this current). INH need not be switched for this measurement.

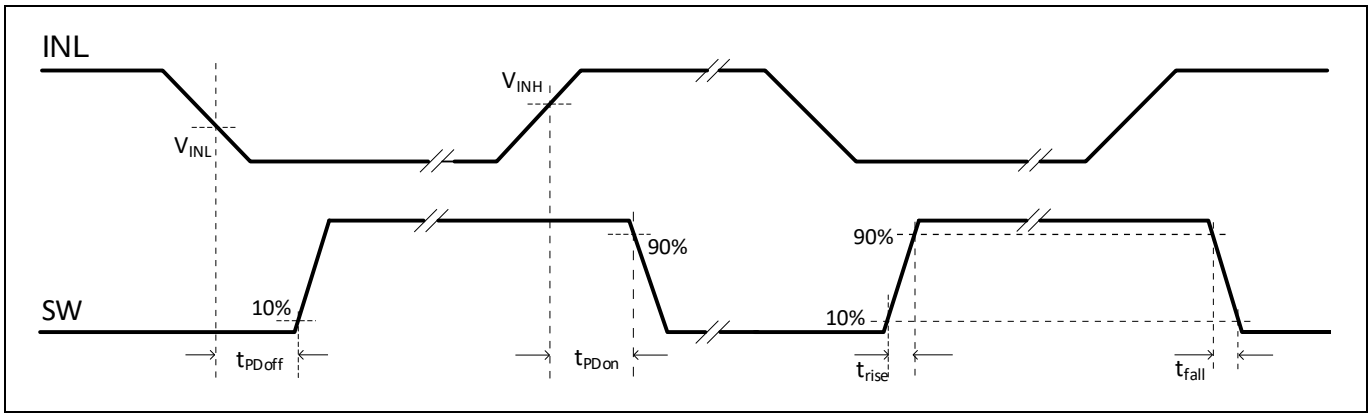


Figure 4 Propagation delay, rise and fall time

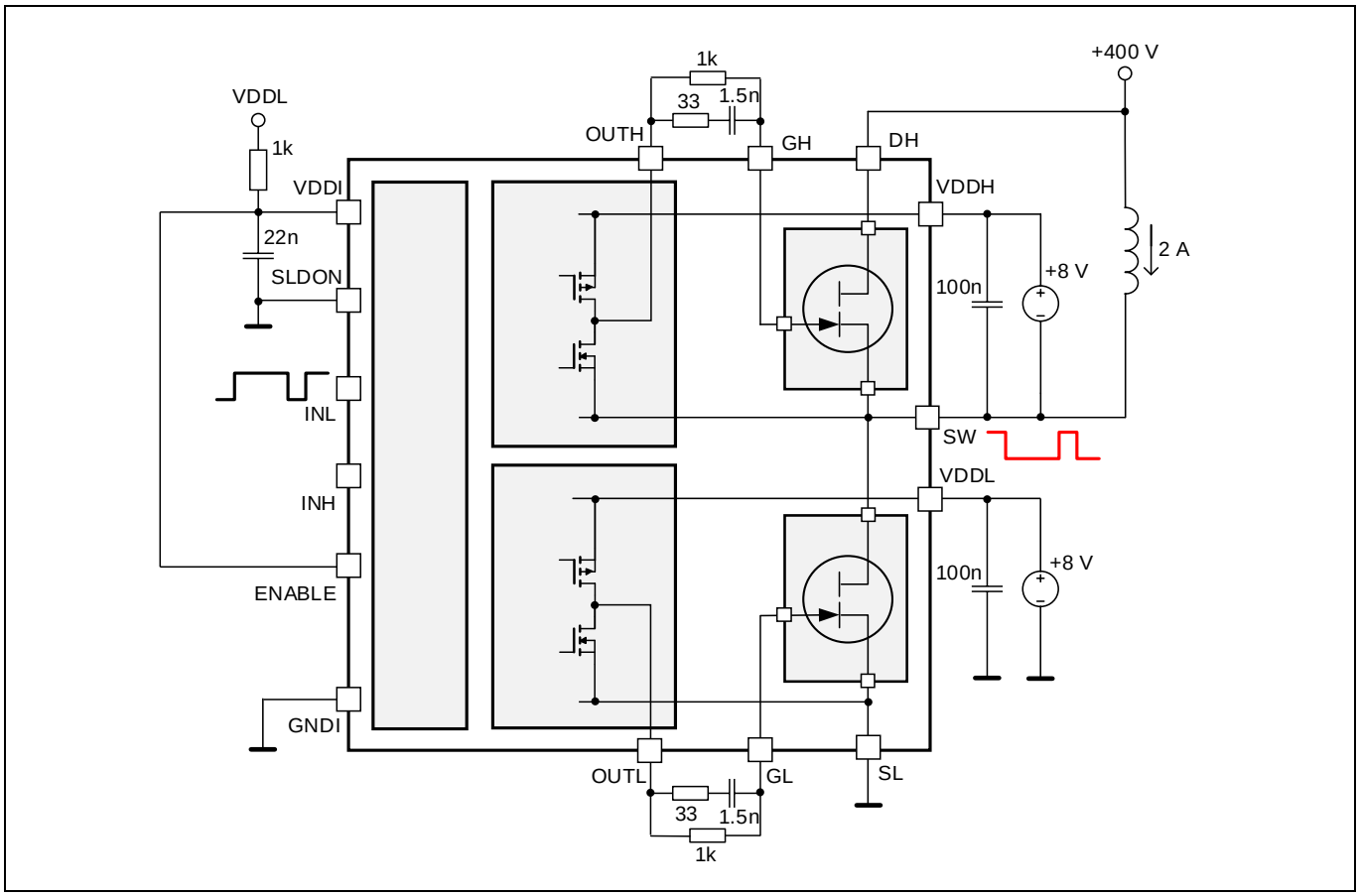


Figure 5 Test circuit

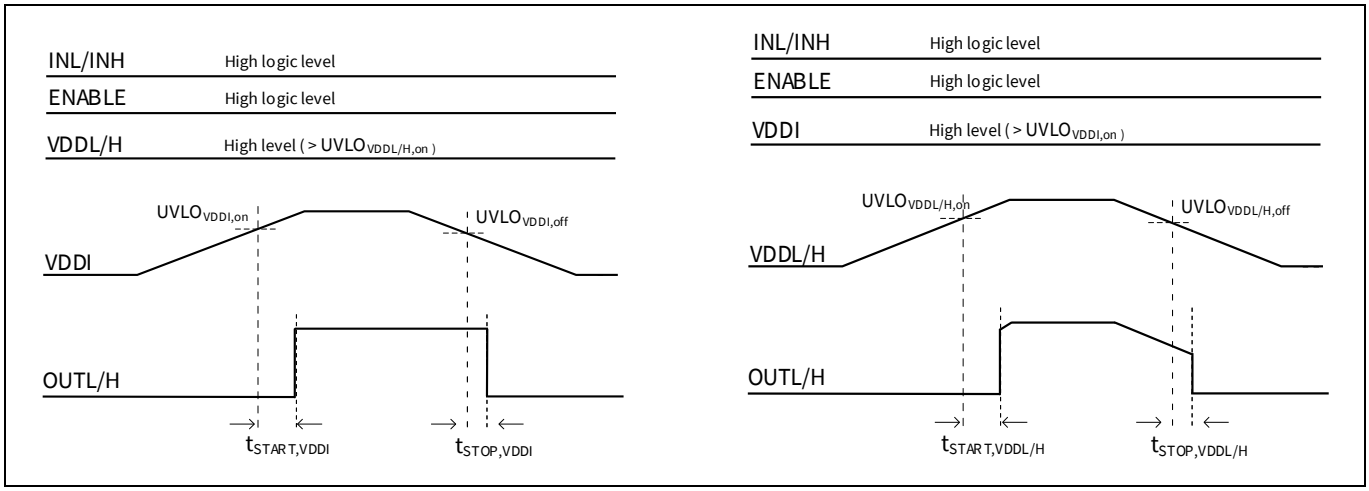


Figure 6 UVLO behavior, start-up and deactivation time (unloaded output)

4 Driving CoolGaN™ HEMTs

Although Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) with ohmic connection to a pGaN gate are robust enhancement-mode (“normally-off”) devices, they differ significantly from MOSFETs. The gate module is not isolated from the channel, but behaves like a diode with a forward voltage V_F of 3 to 4 V. Equivalent circuit and typical gate input characteristic are given in **Figure 7**. In the steady “on” state a continuous gate current is required to achieve stable operating conditions. The switch is “normally-off”, but the threshold voltage V_{th} is rather low (~ +1 V). This is why in many applications a negative gate voltage -V_N, typically in the range of several Volts, is required to safely keep the switch “off” (**Figure 7b**).

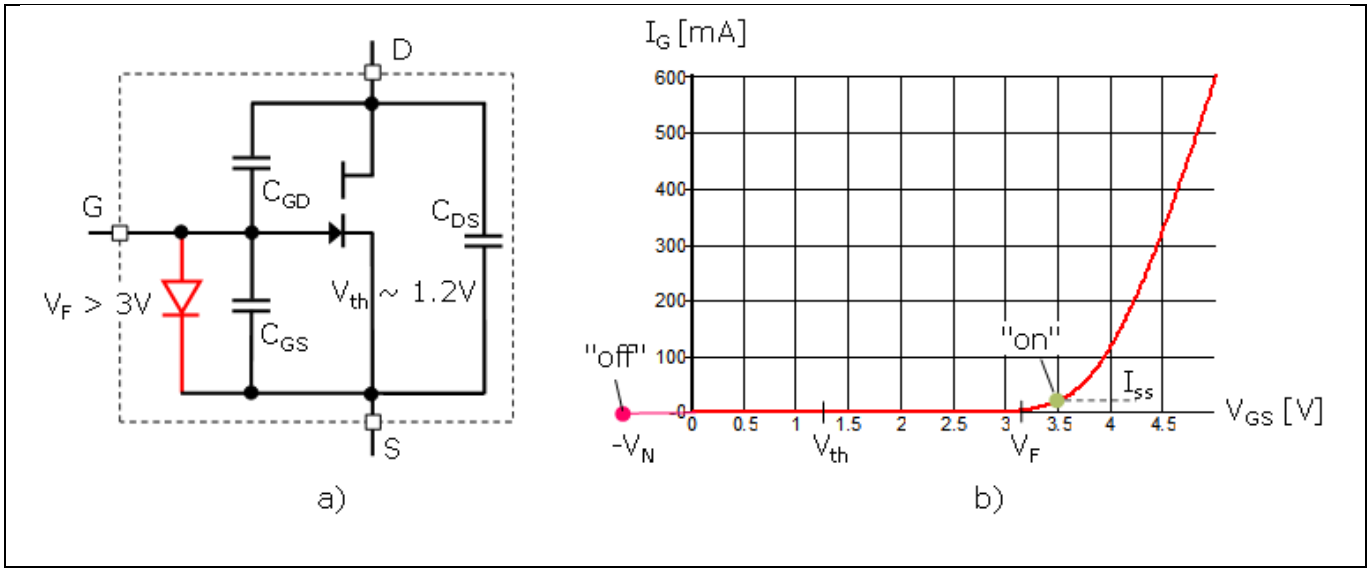


Figure 7 Equivalent circuit (a) and gate input characteristics (b) of typical normally-off GaN HEMT

Obviously the transistor in **Figure 7** cannot be driven like a conventional MOSFET due to the need for a steady-state “on” current I_{ss} and a negative “off” voltage –V_N. While an I_{ss} of a few mA is sufficient, fast switching transients require gate charging currents I_{on} and I_{off} in the 1 A range. To avoid a dedicated driver with 2 separate “on” paths and bipolar supply voltage, the solution depicted in **Figure 8** is usually chosen, combining a standard gate driver with a passive RC circuit to achieve the intended behavior. The high-current paths containing the small gate resistors R_{on} and R_{off}, respectively, are connected to the gate via a coupling capacitance C_C. C_C is chosen to have no significant effect on the dynamic gate currents I_{on} and I_{off}. In parallel to the high-current charging path the much larger resistor R_{ss} forms a direct gate connection to continuously deliver the small steady-state gate current I_{ss}. In addition, C_C can be used to generate a negative gate voltage. Obviously, in the “on”-state C_C is charged to the difference of driver supply V_{DD} and diode voltage V_F. When switching off, this charge is redistributed between C_C and C_{GS} and causes an initial negative V_{GS} of value:

$$V_N = \frac{C_C \cdot (V_{DD} - V_F) - Q_G}{C_C + C_{GS}} \quad (2)$$

with Q_G denoting the total gate charge. V_N can thus be controlled by proper choice of V_{DD} and C_C. During the „off“ state the negative V_{GS} decreases, as C_C is discharged via R_{SS}. The associated time constant cannot be chosen independently, but is related to the steady-state current and is typically in the 1 µs range. The negative gate voltage at the end of the “off” phase (V_{Nf} in **Figure 8b**) thus depends on the “off” duration. It lowers the effective driver voltage for the following switching-on event, resulting in a slight dependence of switching dynamics on frequency and duty cycle. However, in most applications the impact of this effect is negligible.

Another situation requires attention, too. If there is by any reason a longer period with both switches of a half-bridge in “off”-state (e.g. during system start-up, burst mode operation etc.), both capacitors C_C will be discharged. That

means, for the first switching pulse after such an extended non-switching period no negative voltage is available. To avoid instabilities due to spurious turn-on effects in such a situation, C_C should not be chosen lower than 1 nF.

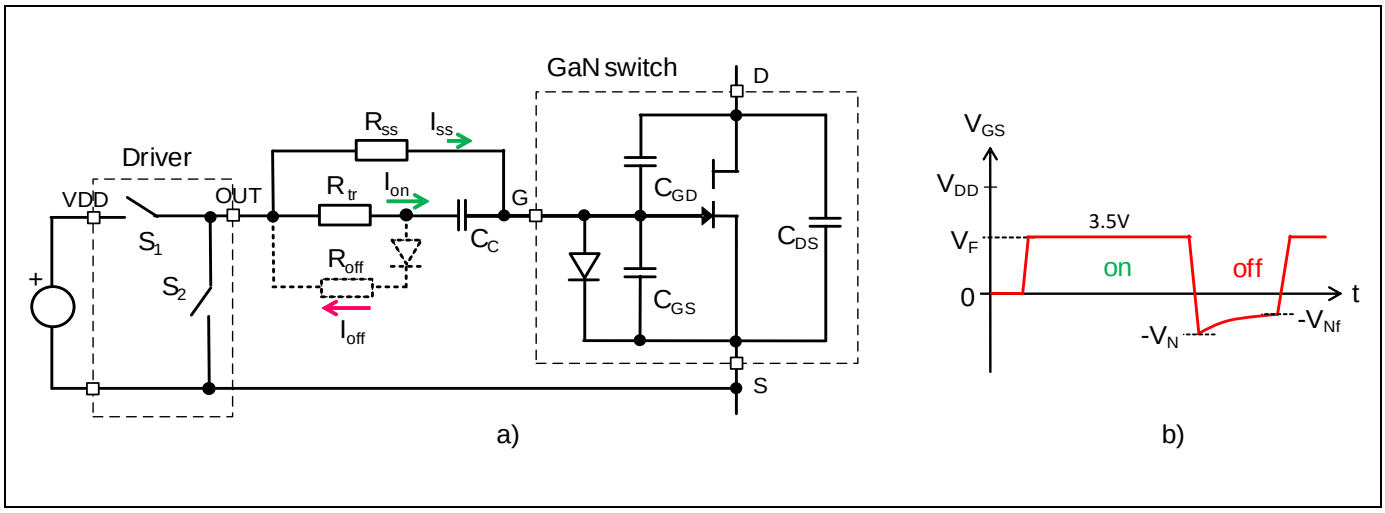


Figure 8 Equivalent circuit of GaN switch with RC gate drive (a) and gate-to-source voltage V_{GS} (b)

In the topology of **Figure 8** often a single resistor R_{tr} can be used for setting the maximum transient charging and discharging current. If this is not acceptable by any reason, an additional resistor R_{off} with series diode in parallel with R_{tr} can be used to realize independent gate impedances for the “on” and “off” transient, respectively.
All relevant driving parameters are easily programmable by choosing V_{DD}, R_{ss}, R_{tr}, R_{off} and C_C according to the relations

$$V_N = \frac{C_C \cdot (V_{DD} - V_F) - Q_G}{C_C + C_{GS}}$$

$$I_{ss} = \frac{V_{DD} - V_F}{R_{ss}}, \qquad I_{on,max} \sim \frac{V_{DD} - V_{Nf}}{R_{tr}}, \qquad I_{off,max} \sim \frac{(V_{th} + V_N) \cdot (R_{off} + R_{tr})}{R_{off} \cdot R_{tr}} \tag{3}$$

The main guidelines for dimensioning gate drive parameters are as follows:

- V_N must always be positive; a target value of 2 V in soft-switching and 4 V to 5 V in hard-switching systems is recommended
- The target value of I_{ss} is around 3 mA, R_{ss} has to be chosen accordingly
- R_{tr} sets the transient speed for a hard switching “on” event. Due to the low gate charge, values above 50 Ω typically do not result in significant benefits. For soft switching systems R_{tr} is anyway uncritical.
- If a separate R_{off} is used, it should guarantee sufficient damping of oscillations in the gate loop.

For a given driving voltage the values for the gate drive components can now be derived from equations (3).
V_{DD} = 8 V, for example, yields

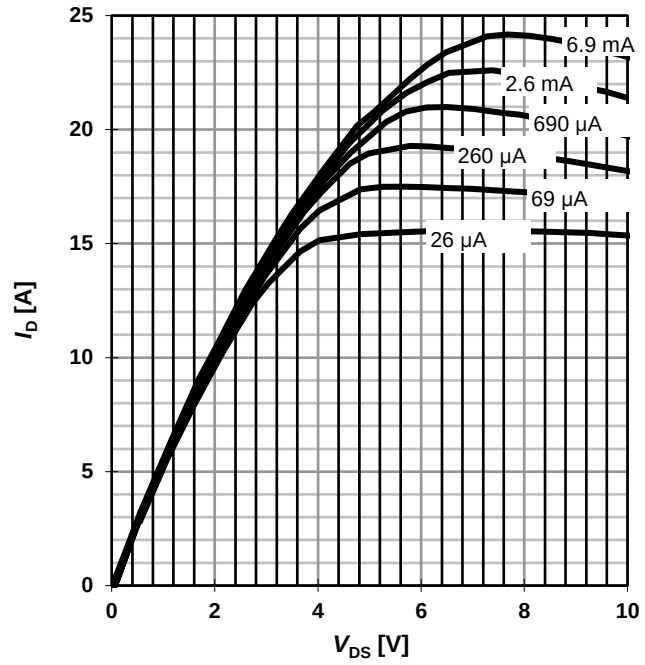
- C_C = 1.2 nF
- R_{ss} = 2 kΩ
- R_{tr} = 27 … 68 Ω
- R_{off} = 10 Ω (if used)

For more information regarding how to drive GaN HEMT refer to [2] [3].

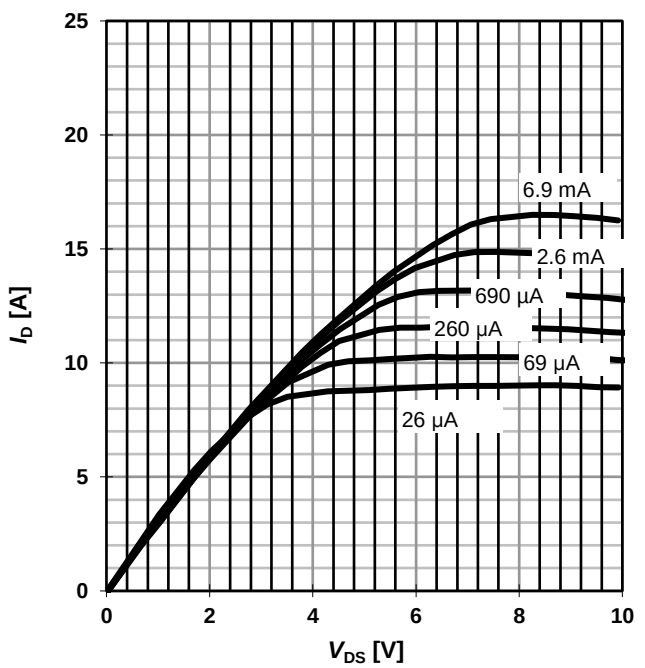
5 Typical characteristics

5.1 GaN switch characteristics

The following graphs refer to a single GaN switch.

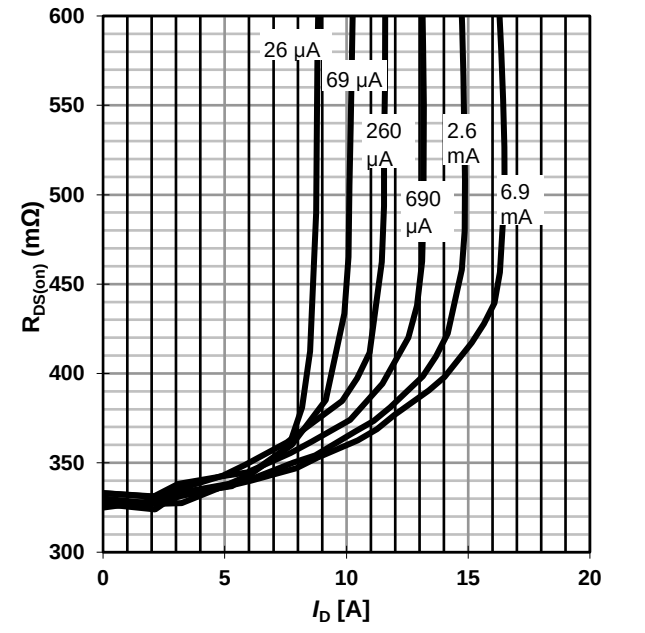


$I_D=f(V_{DS},I_{GS})$; $T_j=25°C$

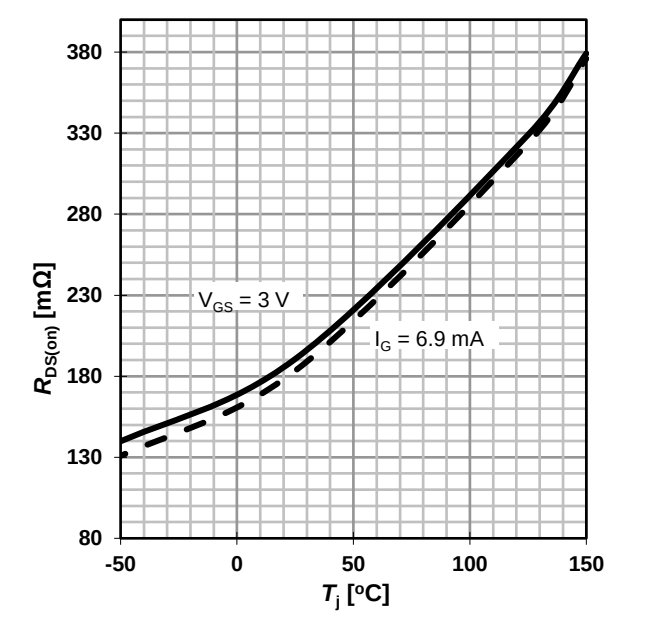


$I_D=f(V_{DS},I_{GS})$; $T_j=125°C$

Figure 9 Typical output characteristics

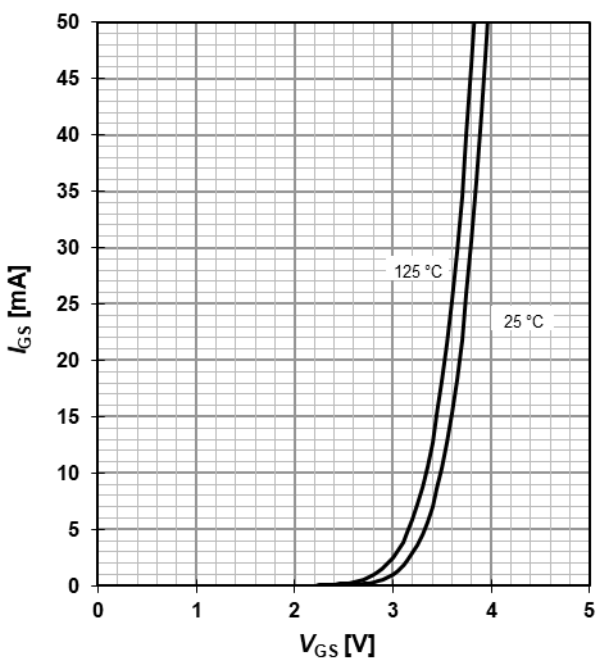


$R_{DS(on)}=f(I_D,I_G)$; $T_j=125°C$

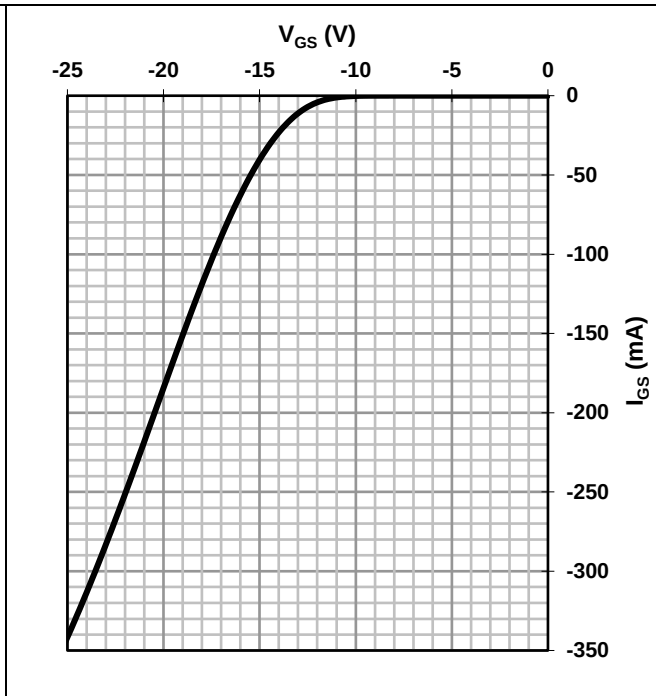


$R_{DS(on)}=f(T_j)$; $I_D=2.11$ A

Figure 10 Typical drain-source on-resistance

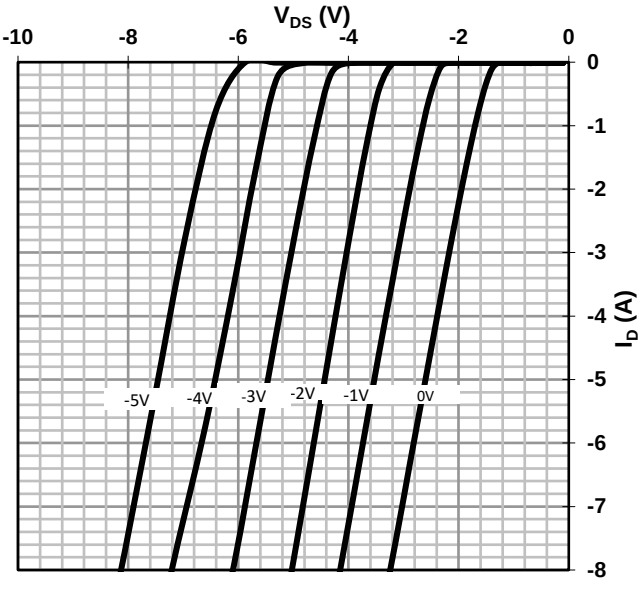


$I_{GS}=f(V_{GS},T_j)$; Open Drain

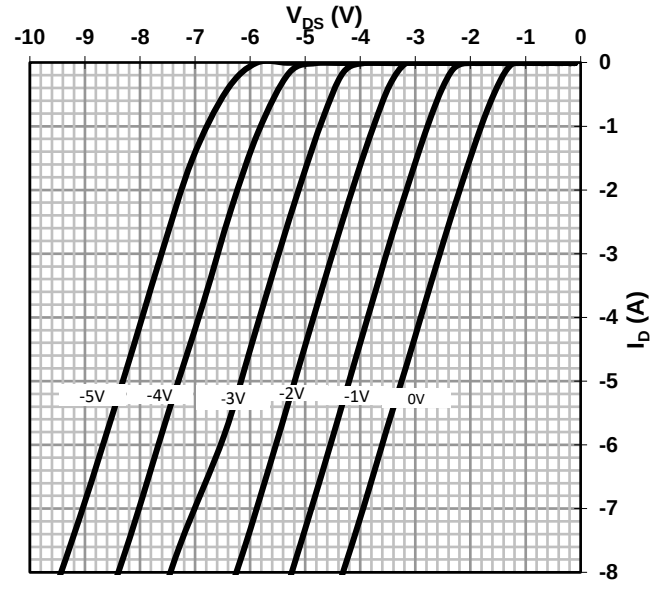


$I_{GS}=f(V_{GS},T_j)$; T_j=25°C

Figure 11 Typical gate characteristics forward and reverse

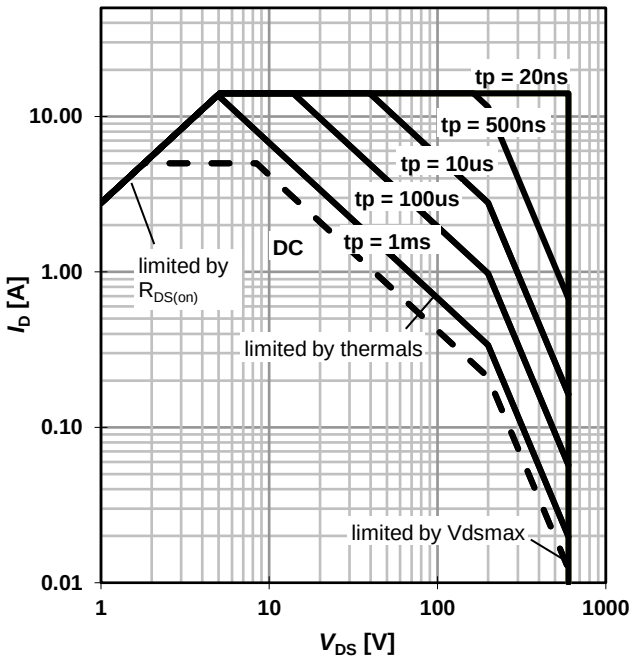


$V_{DS}=f(I_D, V_{GS})$; T_j = 25 °C

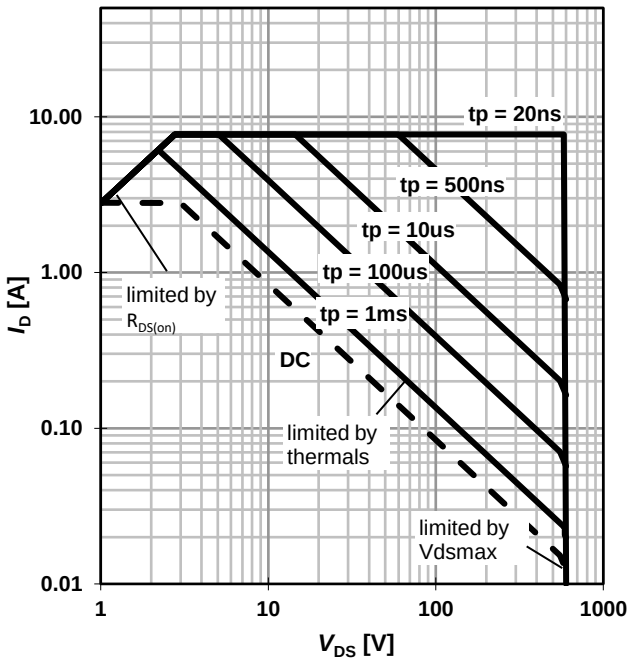


$V_{DS}=f(I_D, V_{GS})$; T_j = 125 °C

Figure 12 Output characteristic I_{ds} (V_{ds}) in reverse operation (parameter V_{gs})

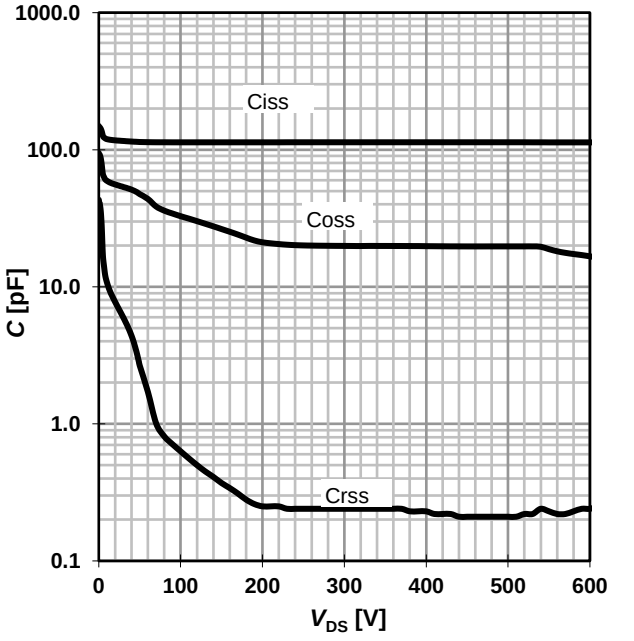


$I_D=f(V_{DS})$; $T_C=25°C$

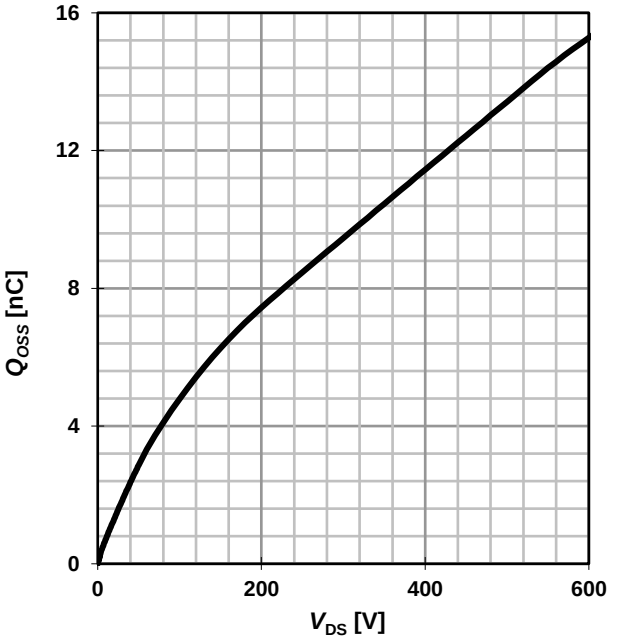


$I_D=f(V_{DS})$; $T_C=125°C$

Figure 13 Safe Operating Area (SOA)



Typical V_{DS}-dependence of terminal capacitances



Typical V_{DS}-dependence of Output charge

Figure 14 Terminal capacitances and output charge (single switch)

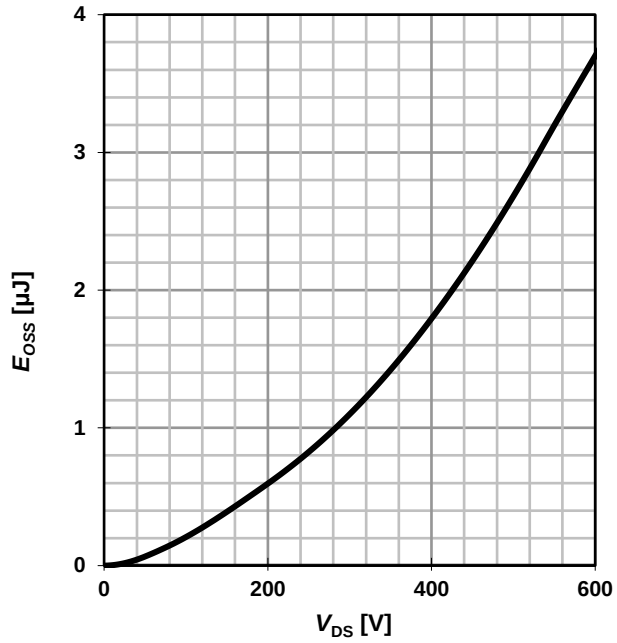
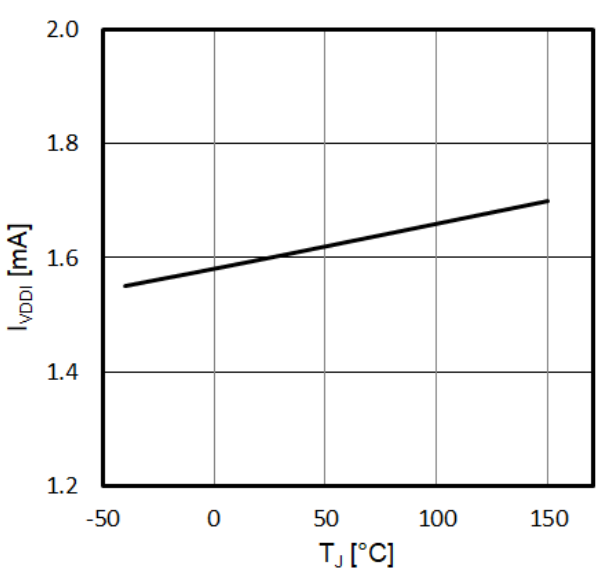
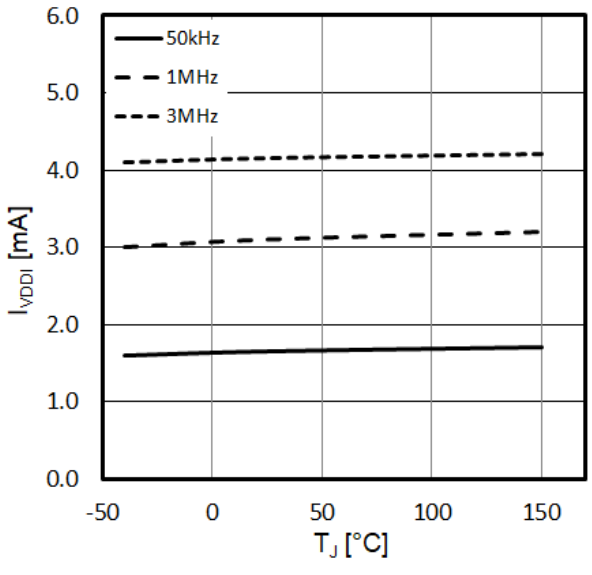


Figure 15 Typical output energy (single switch)

5.2 Gate driver characteristics

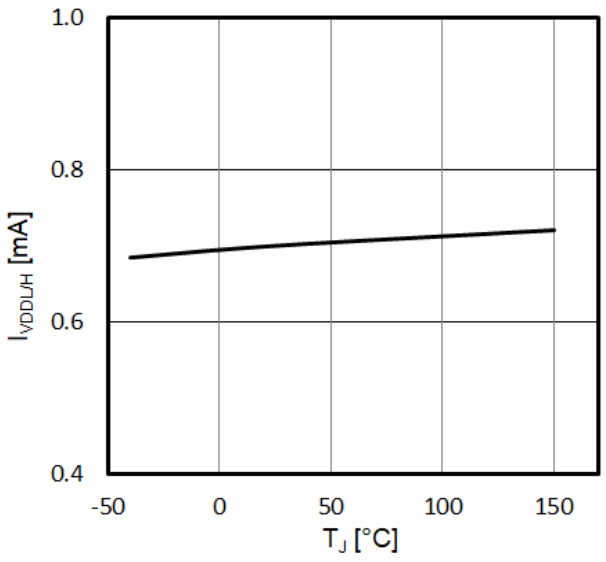


Typical V_{DDI} quiescent current vs. temperature

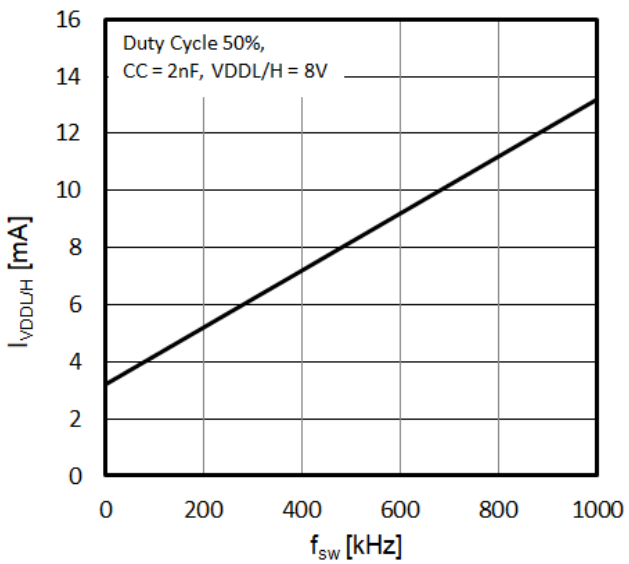


Typical V_{DDI} current vs. temperature and frequency

Figure 16 Supply current V_{DDI}

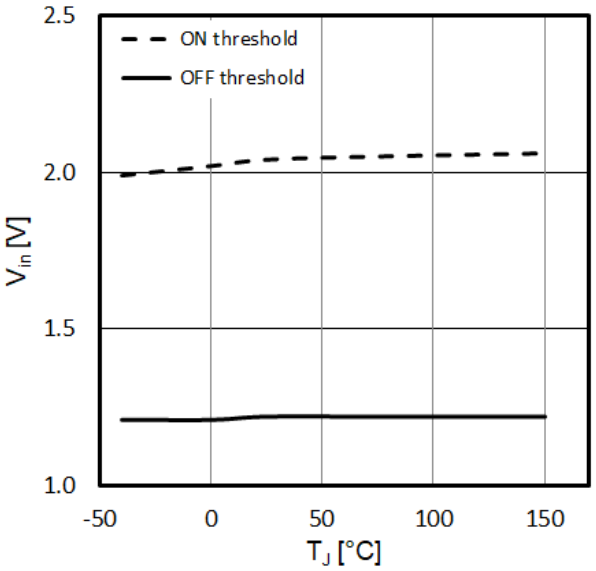


Typical $V_{DDL/H}$ quiescent current vs. temperature

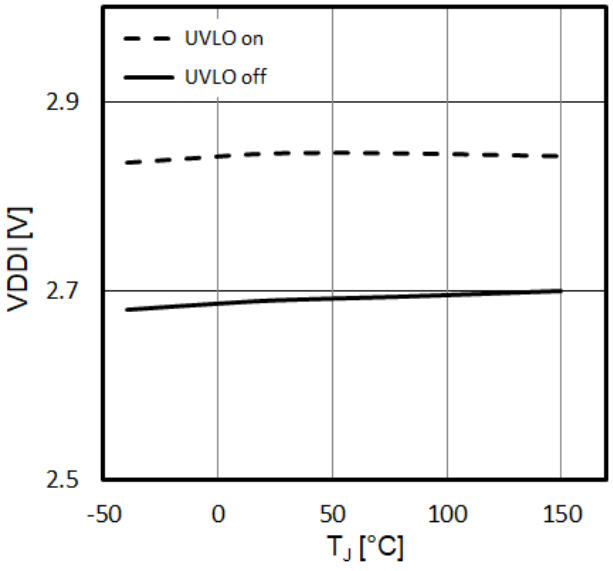


Typical $V_{DDL/H}$ current vs. switching frequency

Figure 17 Supply current $V_{DDL/H}$

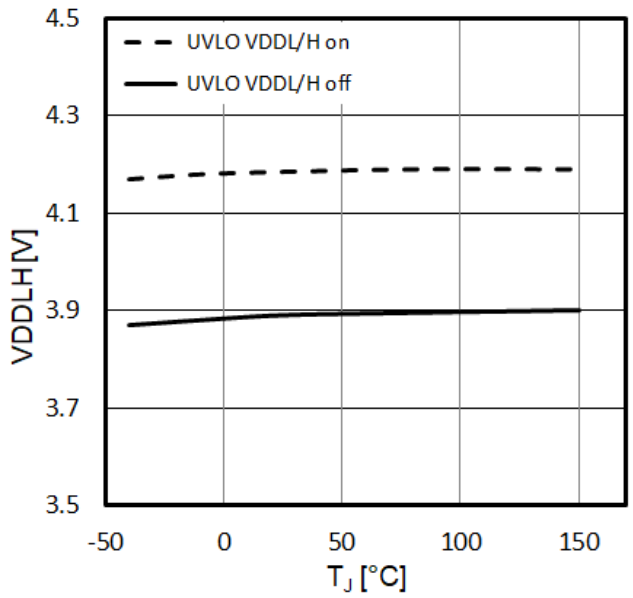


Typical input voltage thresholds vs. temperature



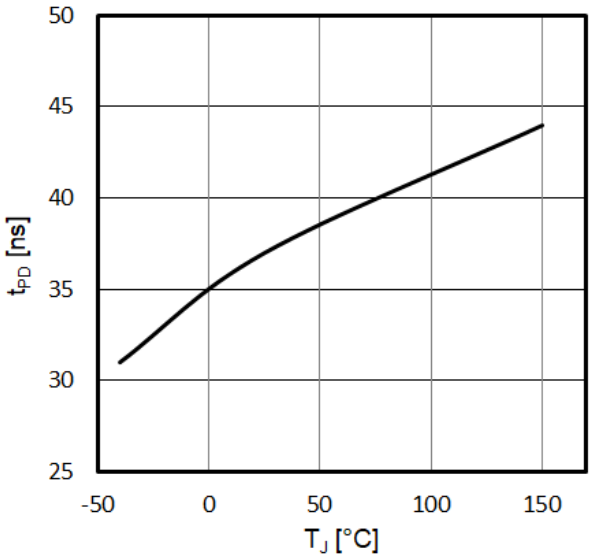
Typical undervoltage lockout thresholds V_{DDI} vs. temperature

Figure 18 Logic input thresholds and V_{DDI} UVLO

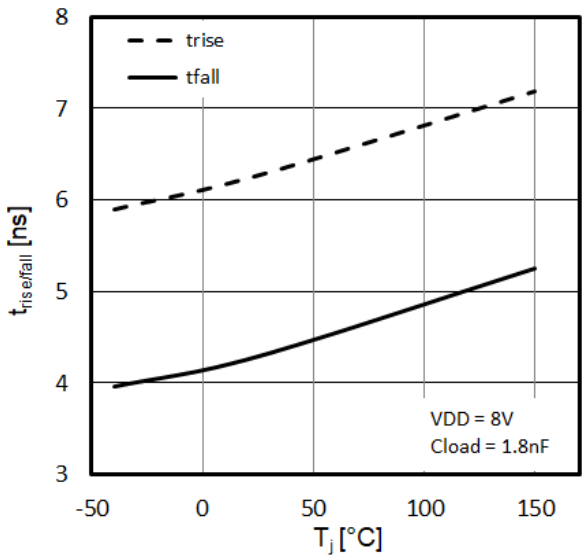


Typical undervoltage lockout thresholds $V_{DDL/H}$ vs. temperature

Figure 19 $V_{DDL/H}$ UVLO



Typical propagation delays vs. temperature



Typical rise and fall time vs. temperature

Figure 20 Propagation delay and rise / fall times

6 Application circuit

In **Figure 21** a typical application example is given with IGI60F2020A1L operated in an actively clamped flyback topology.

In this application the recommended values for the gate drive circuit are as follows:

V_{DD} = 8 V

C_C = 1.2 nF

R_{ss} = 2 kΩ

R_{tr} = 27 … 68 Ω

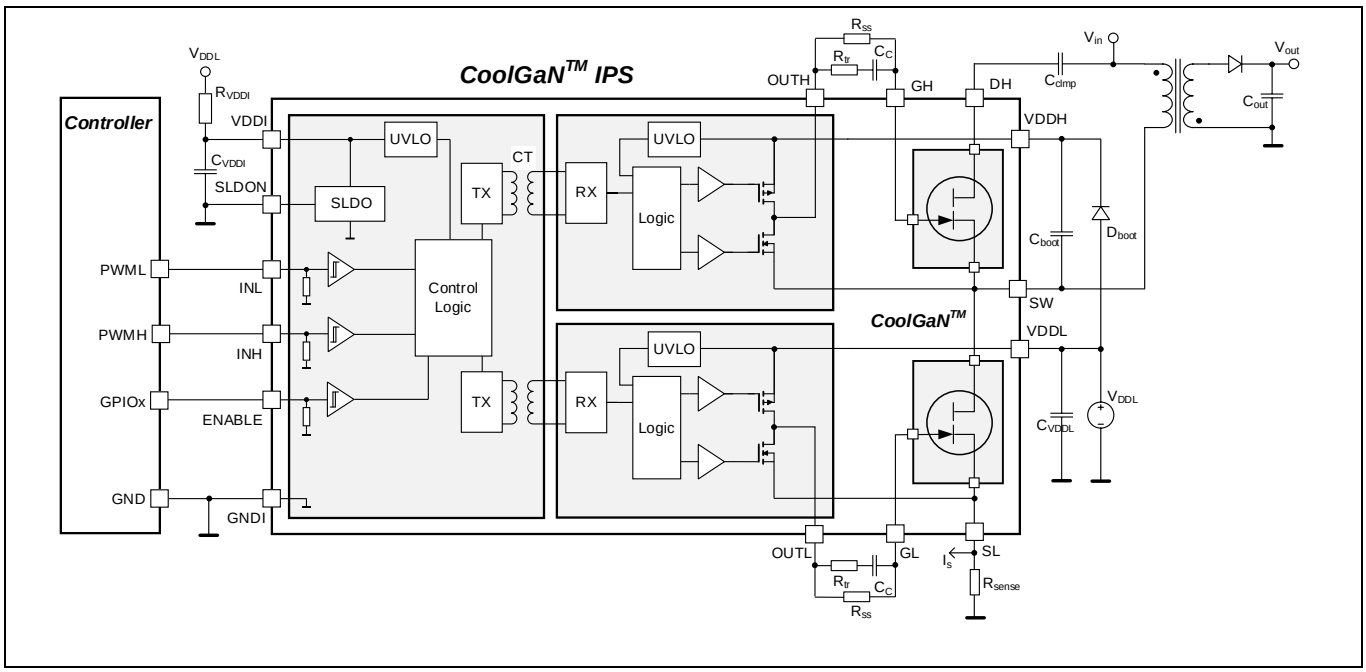


Figure 21 Application Circuit (active clamp flyback converter)

7 Package information

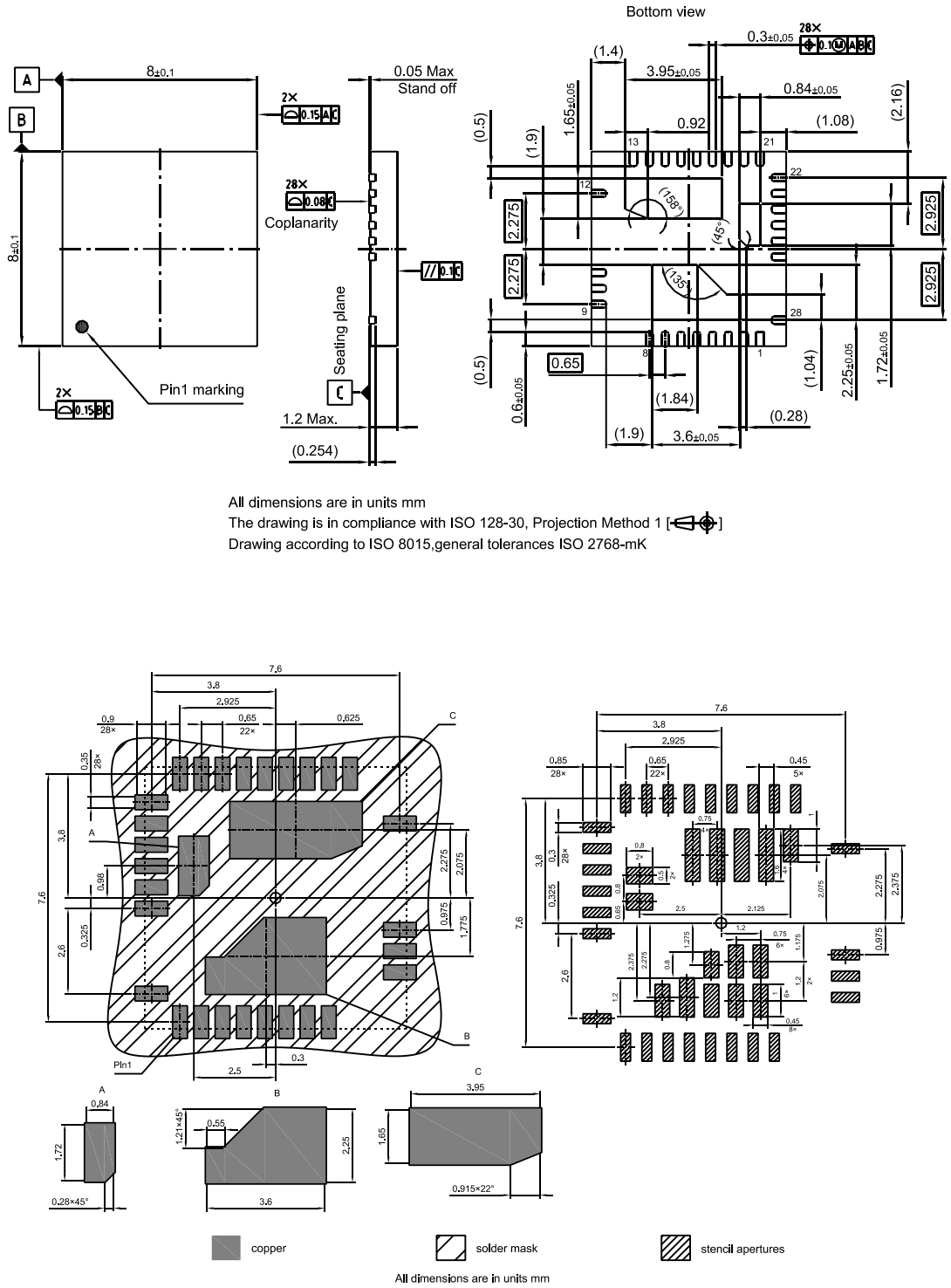


Figure 22 TIQFN-28-1 8x8 package outline and footprint

8 Layout guidelines

Figure 23 shows the suggested arrangement of the power stage and the external components on the PCB based on the schematic shown in the **Figure 24.**

Figure 25 and **Figure 26** show the top and bottom layer of the PCB. The following layout recommendations should be considered:

1. On the exposed pads' landing area place vias with 0.3mm hole size with <0.7mm space (center to center)
2. Use solder mask expansion of 0.05~0.075mm for the chipset footprint pins and pads
3. Place and align the GND trace (PGND node for power return) beneath the DC bus trace on the top layer to minimize the inductance loop in the power path.
4. For the low voltage controller reference (DGND) on the PGND trace select a location free of any switching current to avoid switching-induced noise in DGND (do not connect the DGND trace to any trace which connects the bypass cap to CoolGaN™).

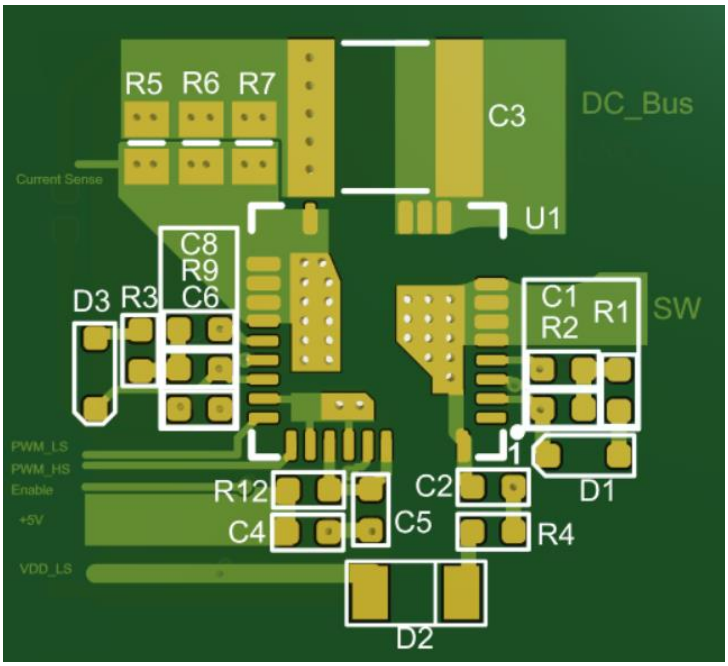


Figure 23 CoolGaN™ IPS external component placement on the PCB

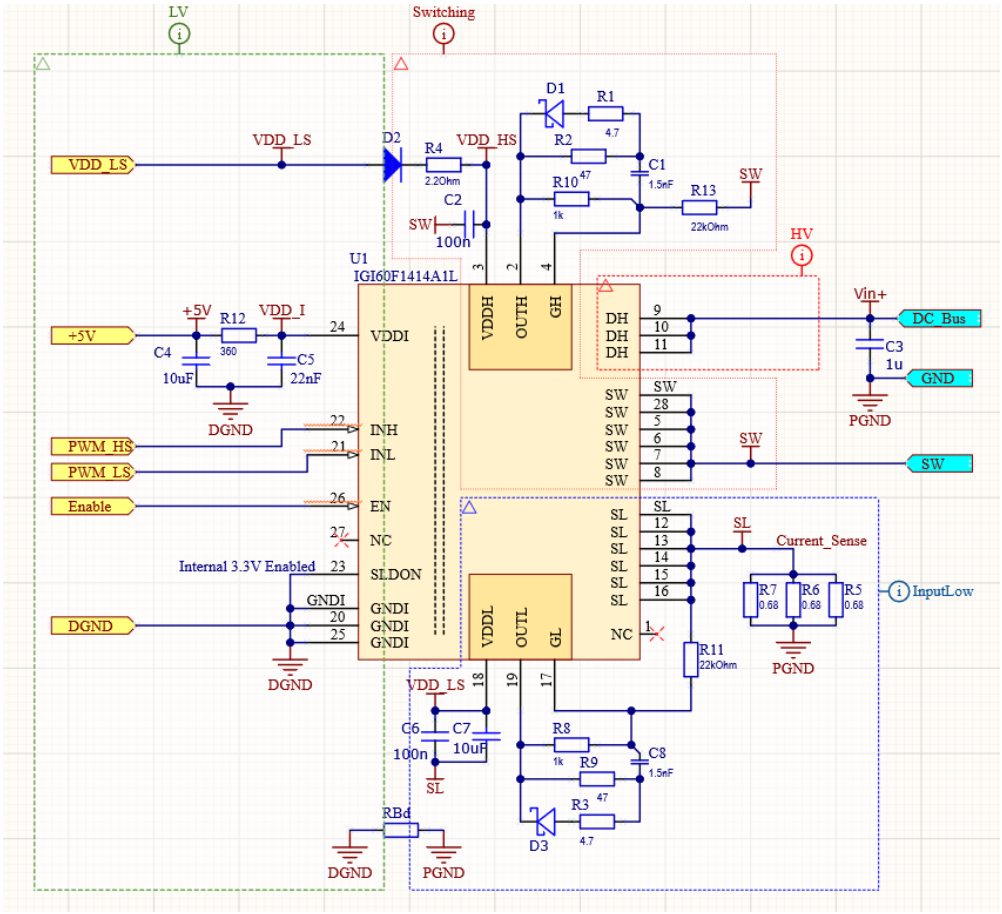


Figure 24 CoolGaN™ IPS circuitry with external passive components

Refer to Appendix (I) to download the footprint and the PCB example for Altium. Also, a complete PCB project with this product is available in the CoolGaN™ Half-Bridge IPS Evaluation Board project.

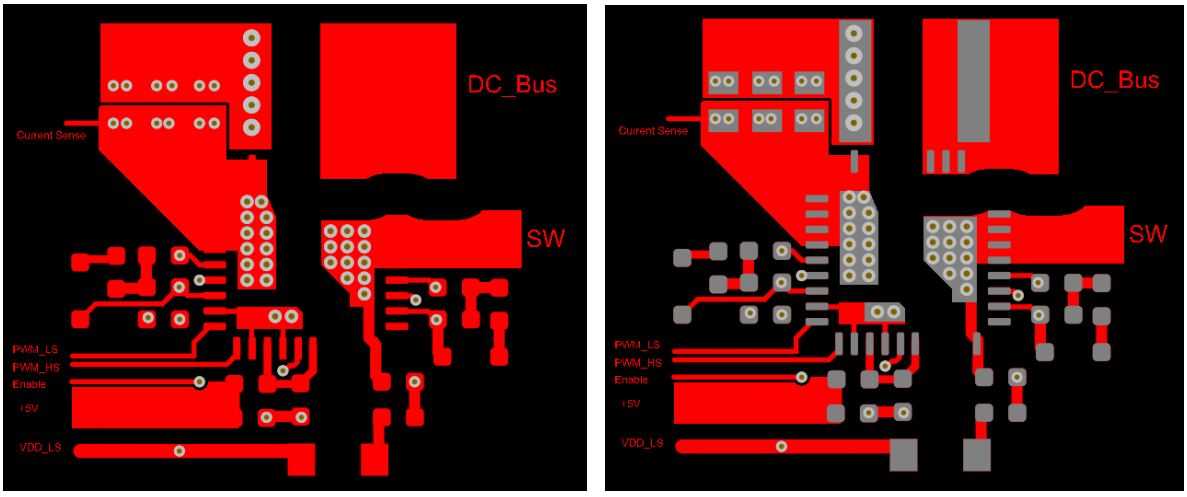


Figure 25 Top layer of the PCB (trace on the left and top solder paste layer on the right)

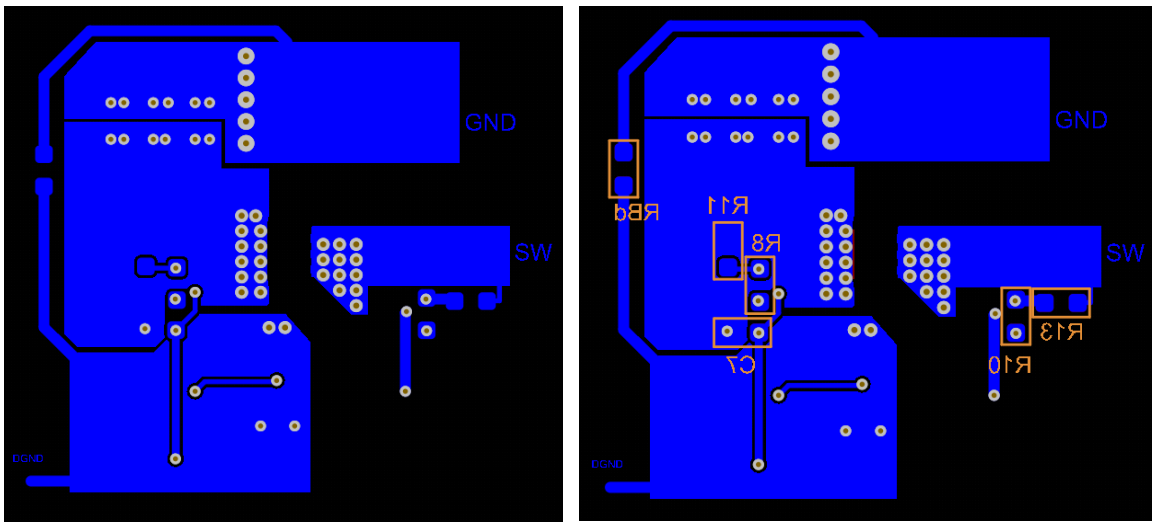


Figure 26 Bottom layer of the PCB - top view (Trace on the left and silk mask on the right)

9 Appendix

I. PCB footpriont and Altium file for the reference PCB design can be found in the CoolGaN™ Half-bridge IPS webpage (product registration is needed to access the design files)

II. Related Links

IFX CoolGaN™ webpage: www.infineon.com/why-coolgan

IFX CoolGaN™ reliability white paper: www.infineon.com/gan-reliability

IFX CoolGaN™ applications information:

www.infineon.com/gan-in-server-telecom

www.infineon.com/gan-in-wirelesscharging

www.infineon.com/gan-in-adapter-charger

10 References

[1] CoolGaN™ application note

[2] Driving CoolGaN™ 600 V high electron mobility transistors

[3] Quick-reference guide to driving CoolGaN™ GIT HEMTs 600V

Revision history

Document version	Date of release	Description of changes
V1.0	2023-02-14	1st version of final datasheet
V1.1	2023-05-05	Products overview update with marking information

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