LG Semicon Co.,Ltd.

GM72V161621ET/ELT

524,288 WORDS x 16BIT x 2BANK
SYNCHRONOUS DYNAMIC RAM

Description

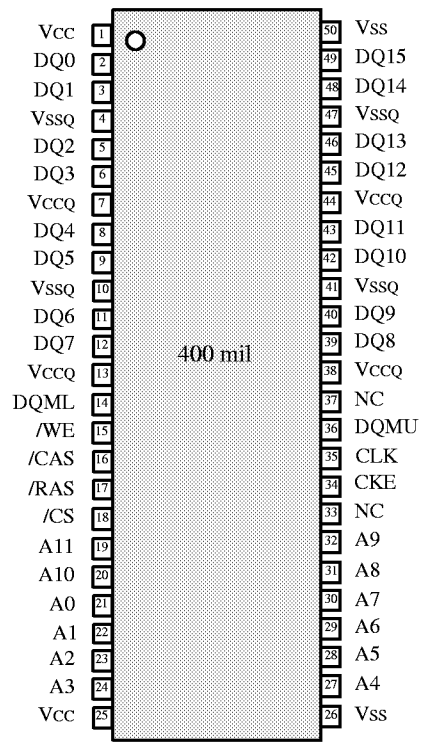
The GM72V161621ET/ELT is new generation synchronous dynamic RAM, organized 534,288 words x 16bit x 2bank. This device offers fully synchronous operation referenced to clock rising edge, and mode register allows programmable of burst length, burst type and column access latency. This device is offered in 50pin 400mil plastic TSOP II.

Features

* 524,288 Words x 16 Bit x 2 Bank Organization
* 3.3V +/- 0.3V Power supply
* Maximum Clock frequency up to 143 MHz
* LVTTL Interface
* 2 Bank can operate simultaneously and independently
* Burst read/write operation and burst read/ single write operation capability
* Programmable burst length ; 1, 2, 4, 8, Full page
* Programmable burst sequence Sequential / Interleave
* Full Page burst length capability Sequential burst Burst stop capability
* Programmable $\overline{CAS}$ Latency ; 2, 3
* CKE power down mode
* Input / Output data masking
* 4096 Refresh Cycles / 64ms
* Auto refresh / Self refresh Capability
* 50Pin 400mil TSOP II Package

Pin Configuration

50 TSOP II

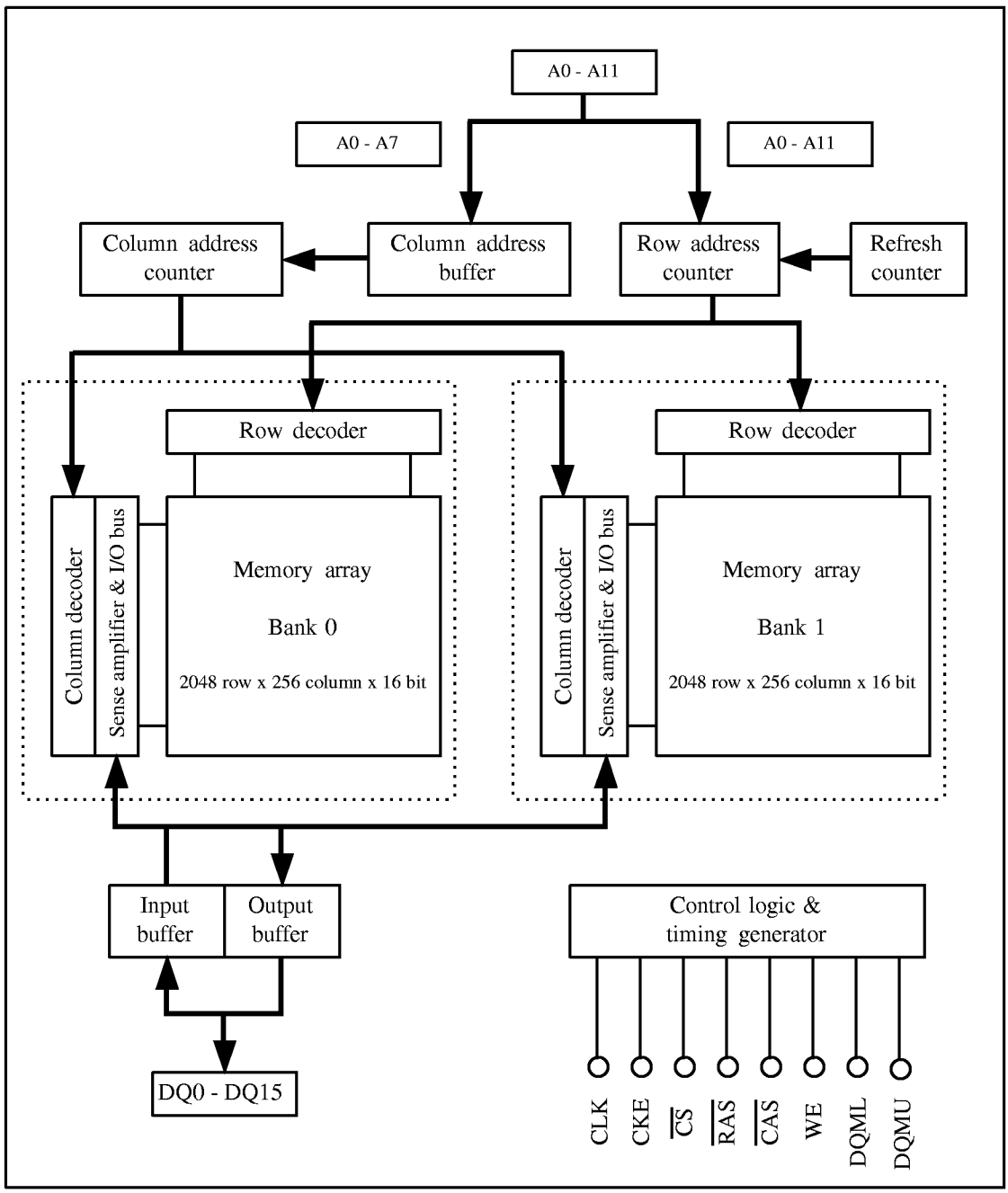


(Top View)

Pin Name

CLK	CLock input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address input
A11 / BS	Address input or Bank Select
DQ0~DQ7	Data input / output
DQM	Data input / output Mask
VCCQ	Power for DQ circuit (3.3V)
VSSQ	Power for DQ circuit
VCC	Power for internal circuit (3.3V)
Vss	Ground for internal circuit
NC	No Connection

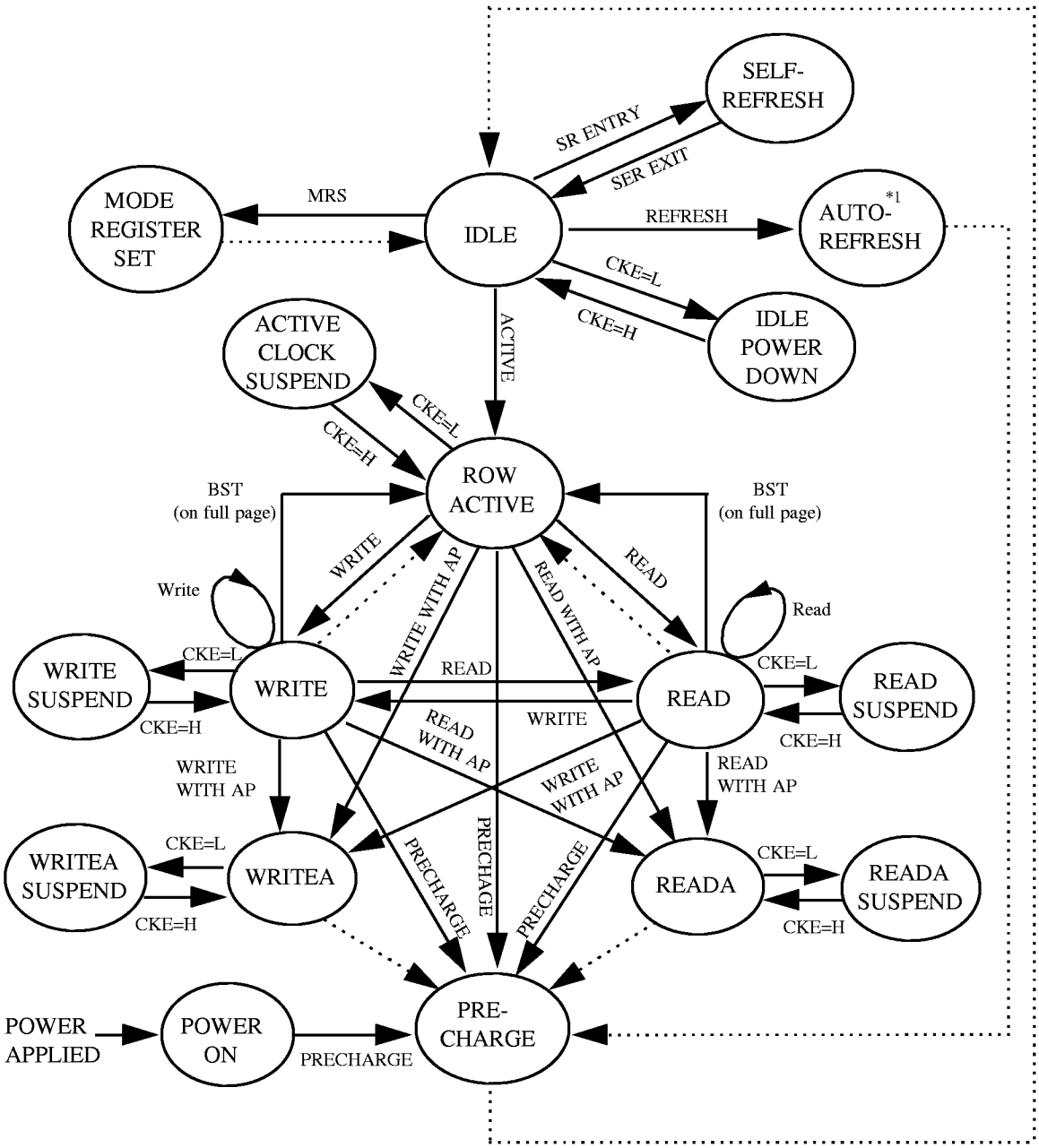
Block Diagram(GM72V161621ET/ELT Series)



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.
A11 (input pin)	A11 is a bank select signal (BS). The memory array of the GM72V161621ET/ELT Series is divided into bank 0 and bank 1. GM72V161621ET/ELT Series contain 2048 row x 256 column x 16bits. If A11 is Low, bank 0 is selected, and if A11 is High , bank 1 is selected.
DQ0 ~ DQ7 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
DQM (input pins)	DQM controls input/output buffers. - Read operation: If DQM is High, The output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. - Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

16M SDRAM Function State Diagram



Note: 1. After the auto-refresh operation, precharge is performed automatically and enter the IDLE state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-1.0 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	C	
Storage temperature	Tstg	-55 to +125	C	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.6V for pulse width <= 3ns

3. V_{IL} (min) = -2.0V for pulse width <= 3ns

DC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3V+/- 0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter	Symbol	-7		-75		-8		-7J		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	-	120	-	115	-	110	-	90	mA	Burst length=1 tRC=min	1, 2, 3
Standby current in Power down	I_{CC2P}	-	2	-	2	-	2	-	2	mA	CKE=V_{IL}, tCK=12ns	5
Standby current in Power down (Input single stable)	I_{CC2PS}	-	1	-	1	-	1	-	1	mA	CKE=V_{IL} tCK=infinity	6
Standby current in non Power down	I_{CC2N}	-	15	-	15	-	15	-	15	mA	CKE,$\overline{CS}$=V_{IH}, tCK=12ns	4
Standby current in non Power down (Input single stable)	I_{CC2NS}	-	5	-	5	-	5	-	5	mA	CKE=V_{IH}, tCK=infinity	4
Active standby current in Power down	I_{CC3P}	-	5	-	5	-	5	-	5	mA	CKE=VIL, tCK=12ns, DQ=High-Z	1, 2, 5
Active standby current in power down (Input single stable)	I_{CC3PS}	-	4	-	4	-	4	-	4	mA	CKE=VIL, tCK=infinity	2,6
Active standby current in non Power down	I_{CC3N}	-	30	-	30	-	30	-	30	mA	CKE,$\overline{CS}$=VIH, tCK=12ns, DQ=High-Z	1, 2, 4
Active standby current in non power down (Input single stable)	I_{CC3NS}	-	20	-	20	-	20	-	20	mA	CKE=V_{IH}, tCK=infinity	2,9
Burst operating current (CL=2)	I_{CC4}	-	140	-	130	-	120	-	120	mA	tCK=min BL = 4	1, 2, 3
Burst operating current (CL=3)		-	170	-	160	-	150	-	120	mA		
Refresh current	I_{CC5}	-	85	-	85	-	85	-	85	mA	tRC=min	3
Self refresh current	I_{CC6}	-	1	-	1	-	1	-	1	mA	V_{IH} >=V_{CC} - 0.2 0V<=V_{IL}<=0.2V	7
			0.4		0.4		0.4		0.4			7,8
Input leakage current	I_{LI}	-5	5	-5	5	-5	5	-5	5	uA	0<=Vin<=V_{CC}	
Output leakage current	I_{LO}	-5	5	-5	5	-5	5	-5	5	uA	0<=Vout<=V_{CC} I/O = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	2.4	-	V	IOH=-2mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	-	0.4	V	IOL=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. L-Version.
9. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25C, V_{CC}, V_{CCQ} = 3.3V +/- 0.3V)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (CLK)	C_{I1}	-	4	pF	1, 3, 4
Input capacitance (Signals)	C_{I2}	-	5	pF	1, 3, 4
Output capacitance (I/O)	C_O	-	6.5	pF	1, 2, 3, 4

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.
4. Measured with 1.4 V bias and 200mV swing at the pin under measurement.

AC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3V+/- 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-7		-75		-8		-7J		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	12	-	12	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	7	-	7.5	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	8	-	8	-	8	-	8	ns	1, 2, 6
	(CL=3)	t_{AC}	-	5.5	-	6	-	6	-	6		
Data-out hold time		t_{OH}	3	-	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence		t_{HZ}	-	6	-	6	-	6	-	6	ns	1, 4
Data-in setup time		t_{DS}	1.5	-	1.5	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	1.5	-	1.5	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	75	-	72	-	70	-	ns	1
Active to Precharge command period		t_{RAS}	49	120000	52.5	120000	48	120000	50	120000	ns	1

AC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3V +/- 0.3V, V_{SS}, V_{SSQ} = 0V)

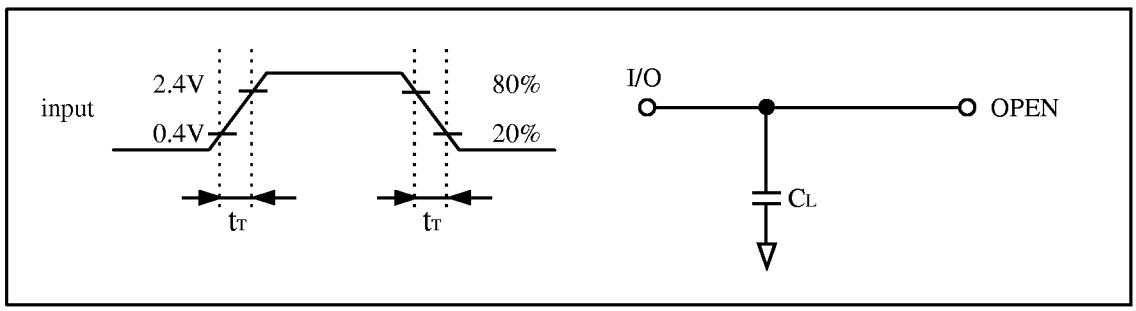
(Continued)

Parameter	Symbol	-7		-75		-8		-7J		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	14	-	15	-	16	-	20	-	ns	1
Precharge to active command period	t_{RP}	21	-	22.5	-	24	-	20	-	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	7	-	7.5	-	8	-	10	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	15	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.50V. Load condition is C_L = 50pF with current source.
3. t_{LZ} (min)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input timing reference levels: 1.4V, Output timing reference levels: 1.5V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-7	-75	- 8	- 7J	Notes
Frequency (MHz)			143	133	125	100	
t_{CK} (ns)			7	7.5	8	10	
Active command to column command (same bank)		t_{RCD}	2	2	2	2	1
Active command to active command period (same bank)		t_{RC}	10	10	9	7	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	7	7	6	5	
Precharge command to active command (same bank)		t_{RP}	3	3	3	2	1
Write recovery or data-in to precharge command (same bank)		t_{DPL}	1	1	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	2	2	1
Self refresh exit time		I_{SREX}	1	1	1	1	
Last data in to active command (Auto precharge, same bank)		I_{APW}	4	4	4	3	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	10	10	9	7	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	
	(CL=2)	I_{HZP}	-	-	-	-	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-	-	-	
Column command to column command		I_{CCD}	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	

Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-7	-75	-8	-7J	Notes
Frequency (MHz)			143	133	125	100	
t_{CK} (ns)			7	7.5	8	10	
CKE to CLK disable		I_{CLE}	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	
	(CL=2)	I_{BSR}	1	1	1	1	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	
	(CL=2)	I_{BSH}	-	-	-	-	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.

Package Dimensions

Unit: Inches (mm)

50 TSOP II