Efficient ISDN Power Converters Using the Si9100

INTRODUCTION

One of the latest technology revolutions, an integrated worldwide telecommunications network, will be accompanied by another advance in power conversion technology. The integrated services digital network (ISDN) will allow different forms of information (voice, computer data, video, facsimile, etc.) to be transmitted over the telephone network. The International Consultative Committee for Telephone and Telegraph (CCITT) has proposed standards for the interfaces required to implement ISDN. Although the standards have yet to be formally adopted, telecommunications companies are moving ahead with pilot test programs, and semiconductor makers are developing chip sets to build ISDN hardware. Every network terminator (NT), signal regenerator (RG), and terminal equipment (TE) unit used for the implementation of ISDN will require a power converter.[1]

A major requirement of these telecom applications (due to the need for emergency-mode operation from a high-impedance source) is high-efficiency energy conversion at fractional-watt power levels. Minimization of parts count, another key factor for the design of these power converters, is sought to simultaneously achieve low cost and high reliability.

BiC/DMOS integrated circuit technology is ideally suited for the power requirements of ISDN. The analog and digital logic functions needed for pulse-width modulation can be implemented in CMOS to minimize quiescent current to the controller. DMOS transistors provide high-voltage power switching with both very low dynamic and gate drive losses. Integration of the CMOS controller on the DMOS power device yields the best overall performance at the lowest cost and component count.

DESIGN OBJECTIVES

While some differences exist between designs, there are several requirements in addition to efficiency which are common to ISDN power converter applications. These include:

- reliable start-up and operation from the high source impedance of telephone subscriber lines (U-interface only)
- current limiting to prevent failure of other network terminals when one power converter output is shorted (S-interface only)
- a free-running internal oscillator for start-up as well as independent operation, which can be synchronized to an external clock signal
- electromagnetic interference (EMI) filtering to limit conducted emissions during both start-up and normal operation, as well as during equipment connections and disconnections.

The Si9100 power IC facilitates compliance with these design requirements with a minimum number of external parts. To illustrate this capability, a discontinuous conduction mode (DCM) flyback converter was built and tested. Measured efficiency was greater than 80% for a wide range of loads, and 60% efficiency was achieved with only a 15-mW load. Before describing the circuit concepts in detail, it is instructive to note the main features of the ISDN power-feeding concept which has been endorsed by the CCITT.

ISDN POWER FEEDING

Figure 1 is a block diagram of the ISDN basic access configuration. The two-wire transmission line defined at the U-interface provides a 192 k-bits-per-second (bps) digital data path which connects subscriber equipment to the local telephone exchange. Although ISDN permits many new services to be offered, the basic service of voice transmission remains a vital function. Therefore, the network power feeding from batteries in the local telephone exchange remains an essential part of modern telephone system planning. The network terminal (NT) connects the local loop, called the S-bus, to the U-interface at the customer's premises. ISDN-compatible terminals (TE1) communicate at a standard 64 k-bps rate over the four-wire S-bus. Non-ISDN-compatible terminal equipment (TE2), such as analog phones, must connect to the S-bus via a terminal adapter (TA).

To minimize noise-coupling problems, the S-bus must be galvanically isolated from the two-wire U-interface. The CCITT recommendations call for an off-line power converter in the NT to supply 4 W at 40 V nominal to the S-bus during normal operation (for up to four telephones with full features). Other terminal equipment (e.g., fax terminals) would be fed solely from local ac power lines. In the event of a power outage, one telephone at the customer premises must be fed from the central office battery. This procedure is accomplished by reversing the voltage polarity on the S-bus. Non-priority terminals have a diode input which isolates them during emergency-mode operation. A single telephone terminal is fed via a full diode bridge, allowing it to operate during the emergency.

A signal regenerator may be required for long loops (U-interface). The Deutsche Bundespost (DBP) proposes to increase the feeding voltage from 60 V to 93 V to compensate for voltage drops on long lines requiring signal regeneration. The standard telephone line voltage used in many other parts of the world is 48 V. Whatever the voltage, the problem for power converters connected to telephone subscriber lines remains the same--they are fed from a high-impedance source.

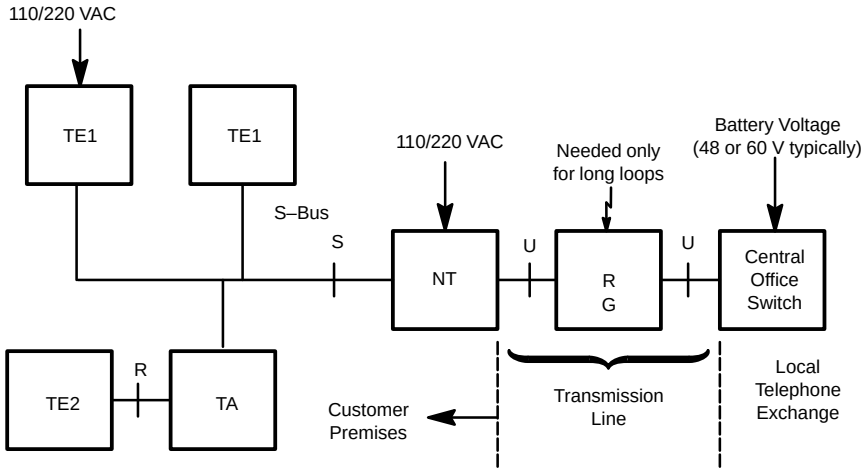


FIGURE 1. ISDN Basic Access Configuration

SOURCE IMPEDANCE EFFECTS

The impedance of telephone subscriber lines limits the amount of power that can be supplied to the load. Referring to Figure 2, for a battery voltage, V_S, and line resistance, R_S, the maximum power to the converter is given by Equation 1, since the power limit occurs when source and load impedances are equal.

$$P_{MAX} = \frac{V_1^2}{R_e} = \frac{\left(\frac{V_S}{2}\right)^2}{R_e} = \frac{V_S^2}{4R_e} \quad (1)$$

R_e is defined as the effective low-frequency input impedance of the power converter.

For a flyback converter, with waveforms as shown in Figure 3, the calculation of the low-frequency input impedance is straightforward. The coupled inductor is designed to ensure operation in the discontinuous conduction mode (DCM). This operation requires that the core flux be reset to zero during each cycle. The current is zero at turn-on and ramps up at a rate given by $di/dt = V_1/L_p$. The maximum value of the peak primary current, I_{pk}, is

$$I_{pk} = \frac{di}{dt}(t_{ON\ (MAX)}) = \frac{V_1}{L_p}\ \frac{T_S}{2} \quad (2)$$

The 50% maximum duty ratio imposed by the Si9100 controller limits the “on” time of Q1 to one-half of the switching period. The average value of the current waveform in Figure 3 is the dc current in the inductor, L1. The current ripple in L1 is small, and the average inductor current, I_{DC}, during start-up is one-fourth the peak current value, as given by

$$I_{DC} = \left(\frac{I_{pk}}{2}\right)(D_{(MAX)}) = \frac{1_{pk}}{4} \quad (3)$$

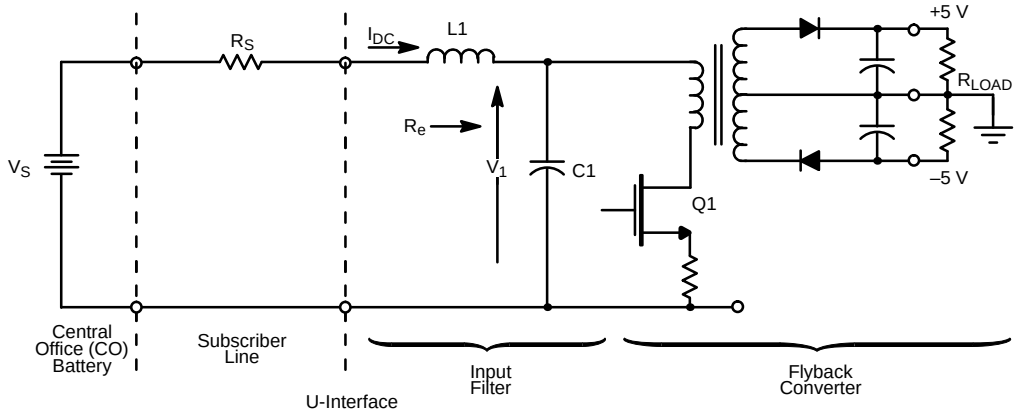


FIGURE 2. Power Converter with High Source Impedance

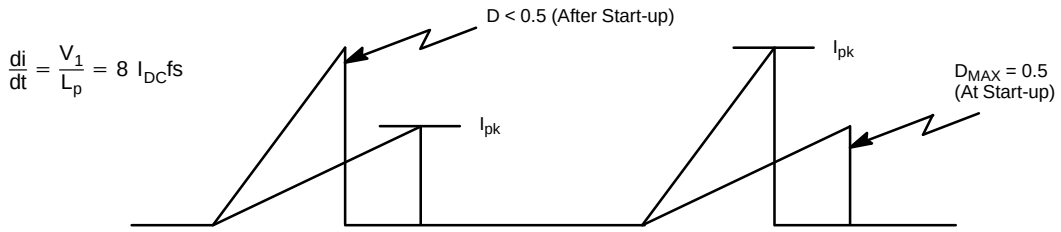


FIGURE 3. Primary Side Current Waveforms

Substituting this result into Equation 2 gives R_e in terms of the primary inductance, L_S, and switching frequency, f_S ($f_S = 1/T_S$).

$$R_e = \frac{V_1}{I_{DC}} = 8L_p f_S \quad (4)$$

L_p effectively acts as a current limiter during start-up, thus eliminating the need for active current limiting circuitry. The value of L_p must be chosen between a minimum value, which sufficiently limits start-up current, and a maximum value, which permits the rated throughput power to the load. Assume, for example, the maximum load condition given in Table 1.[2] The input power to the converter is the output power divided by the efficiency.

$$P_{IN} = \frac{P_O}{\eta} = \frac{0.650}{0.80} = 0.813 \text{ W} \quad (5)$$

Worst-case efficiency at maximum load is assumed to be equal to 80%. The input power to the converter is given by

$$P_{IN} = \frac{1}{2} L_p I_{pk}^2 f_S \quad (6)$$

As seen from Figure 3, if L_p is doubled, I_{pk} is reduced by half. Therefore, P_{IN} varies in inverse proportion to L_p. Referring again to Figure 2, the dc analysis of the input characteristics gives

$$V_1 = V_S - I_{DC} R_S \quad (7)$$

Equations 2, 6, and 7 can be combined to give a quadratic equation which yields the maximum and minimum values for L_p. A graphical approach, however, gives the same answer and, at the same time, provides more insight into system behavior. After start-up has occurred, the power converter no longer presents a constant impedance at the input terminals. Instead, a constant power characteristic pertains, given by

$$P_{IN} = (V_1)\,(I_{DC}) = \text{constant} \quad (8)$$

The demonstration flyback converter was designed to operate from a battery voltage of 48 V and a maximum line resistance of 600 Ω. The constant power curve for (V_1) (I_{DC}) = 0.813, with the load line defined by V_S = 48 V and R_S = 600 Ω, are plotted in Figure 4. The intersection of the load line with the constant power curve determines two operating points, A and B, which occur at (V_1, I_{DC}) = (14.6 V, 55.7 mA) and (33.4 V, 24.3 mA). If V_S is slowly increased from zero, V_S and I_{DC} increase along the line, whose slope is R_e, from the origin to the constant power curve. This analysis is an oversimplification since a step increase in voltage is more likely to occur at power-up. However, worst-case start-up conditions occur at maximum R_S, which guarantees that the input filter is heavily overdamped. Therefore, the increase in V_1 is monotonic, and the results of the simplified analysis are valid.

The lines from the origin to points A and B define the minimum and maximum values for R_e, and with Equation 4, also determine the limits for L_p.

$$R_{e(min)} = 14.6/0.0557 = 263\ \Omega$$
$$R_{e(max)} = 33.4/0.0243 = 1.37\ \text{k}\Omega$$

For a switching frequency design value equal to 20 kHz, Equation 4 gives

$$L_{p(min)} = 1.64 \text{ mH}$$
$$L_{p(max)} = 8.65 \text{ mH}$$

L_p may be chosen near the upper end of the permissible range for maximum start-up current limiting, or it may be chosen for maximum power transfer on a high-resistance line. Setting $R_e = R_S$ = 600 Ω for maximum power transfer gives

$$L_p = \frac{R_e}{8\ f_S} = \frac{600}{(8)(20,000)} = 3.75 \text{ mH}$$

The latter approach was chosen for the demonstration converter (see schematic in Figure 5). The Si9100 functional diagram is given in Figure 6 for reference.

TABLE 1. ISDN POWER REQUIREMENTS				
Operating Mode	**+5-V Current**	**–5-V Current**	**Output Power**	**Measured Efficiency**
Normal—Active	100 mA	30 mA	650 mW	87%
Normal—Power Down	11 mA	3 mA	70 mW	79%
Emergency—Active	55 mA	9 mA	320 mW	88%
Emergency—Power Dpwn	3 mA	0 mA	15 mW	60%

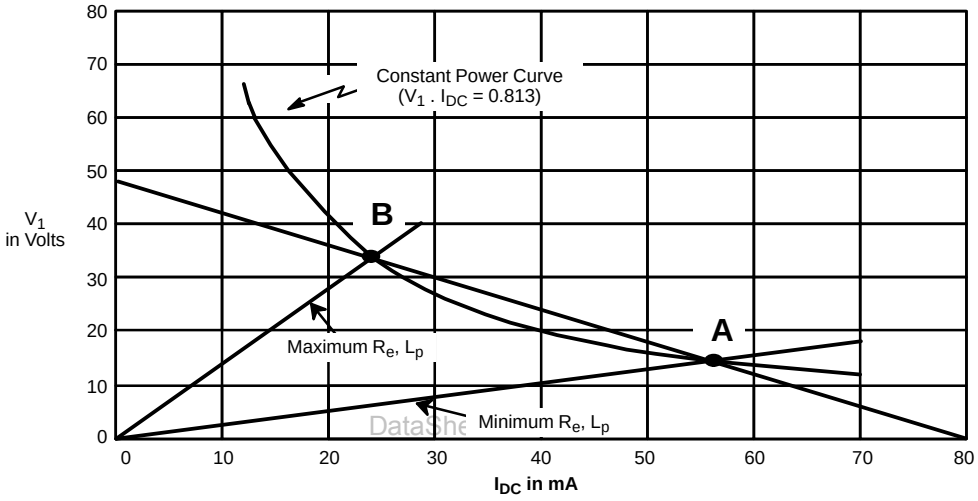


FIGURE 4. Flyback Converter Operating States

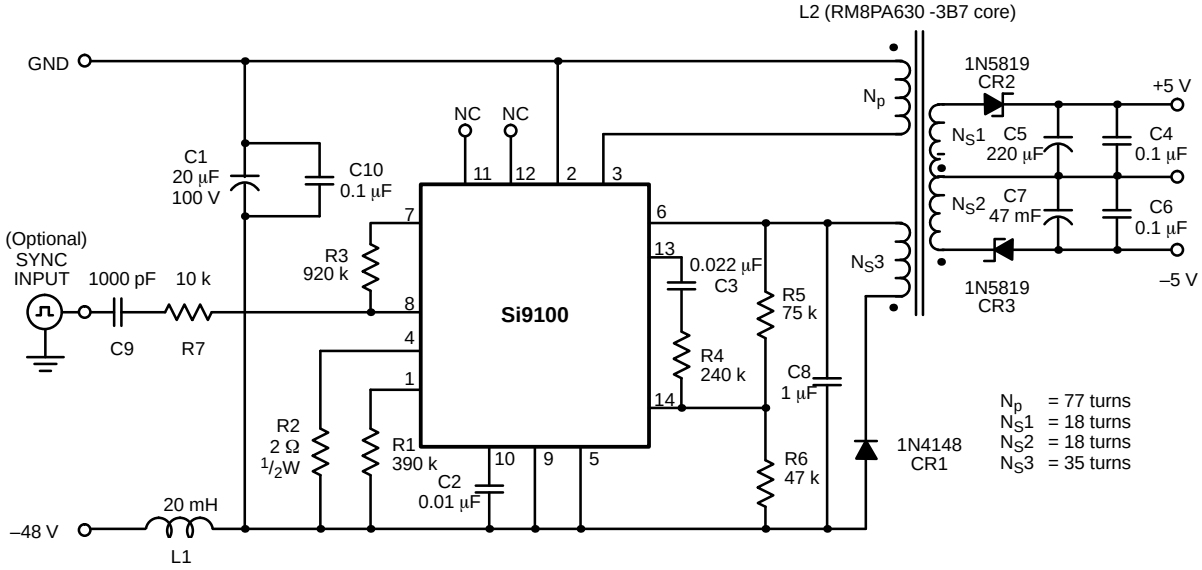
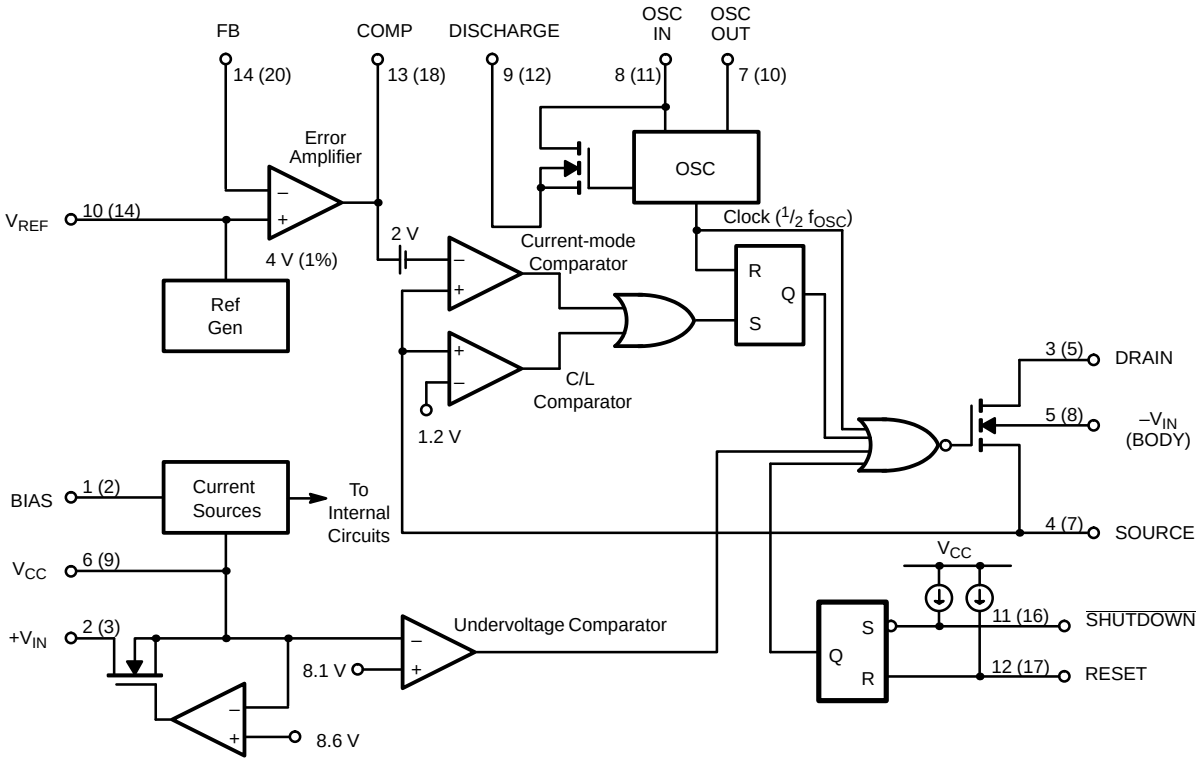


FIGURE 5. ISDN Flyback Converter



NOTE: Figures in parenthesis represent pin numbers for 20-pin package.

FIGURE 6. Si9100 Functional Diagram

CONVERTER PERFORMANCE

Measured efficiency data for the flyback converter is given in the last column of Table 1. Most notable is the 60% efficiency at a load of only 15 mW, which is allowed by the low quiescent current requirement of the CMOS control circuitry in the Si9100. Although power converters can operate at much higher frequencies, the dynamic losses incurred reduce the efficiency during the power-down state. The switching speed (30-ns typical) of the DMOS output transistor in the Si9100 permits operation above audible frequencies with very low dynamic and drive losses. Such performance cannot be achieved with bipolar transistors. A single resistor, R3, sets the oscillator frequency at approximately 34 kHz. A positive sync pulse (5-V amplitude and 0.5-μs pulse width) at 40 kHz was fed through R7 and C9 to pin 8 to demonstrate the principle of synchronization with an external clock. Typically, the free-running frequency should be set at 10 to 20% below the external clock frequency (note that the switching frequency is ½ of the oscillator frequency).

Start-up characteristics were verified by connecting a 600-Ω resistance from a dc power supply to the converter input terminals. Reliable start-up was demonstrated at maximum load for supply voltages as low as 44 V. With zero source resistance inserted in the line, the converter maintained regulation down to an input voltage of 23 V. In both cases, the maximum operating voltage is 70 V for the Si9100 . The inductor, L1, was wound with 540 turns of #32 magnet wire on a #55206 molypermalloy powder core.

The relatively high series resistance of this inductor (6 Ω) provides series damping of the input filter. This damping reduces peaking of the filter output impedance, preventing degradation of the control loop response at the filter resonant frequency when the supply is operated from a low-resistance source.

Measured ripple on both outputs was less than 50 mV peak to peak, and regulation was better than 5% over line and load. The –5-V output increases from –5.05 V to –5.75 V when totally unloaded.

The current-mode controller of the Si9100 provides fast current-limiting response in the event of a shorted output. With either output shorted to ground, the measured value of short-circuit current drawn at the converter input was 30 mA. Any output terminal can be shorted for an indefinite period with no resulting high stress condition on the Si9100. Normal operation resumes when the short circuit is removed.

The input filtering provided by L1 and C1 provides a calculated attenuation of 68 dB at the fundamental of the switching frequency. This allows compliance with FCC Class B and VDE-0871/B requirements; however, conformance testing to these specifications was not performed. Common-mode noise coupling is minimized by the Si9100 since the MOSFET drain is electrically isolated from the package case (a 14-pin DIP). Therefore, very little parasitic capacitance exists from drain to ground. Since the Si9100 places both the driver and MOSFET on the same chip, gate driver lead lengths are reduced from a few centimeters for discrete designs to a few hundred microns.

The 5-mA/µs dynamic current limit required during connection of equipment to the S-bus[3] is met by selecting a suitably high value, 20 mH, for L1. Since several ohms of series resistance is desired, a small wire gauge is used and the inductor is not prohibitively large. A smaller value may be chosen for L1 where the EMI requirements are less critical.

SUMMARY

BiC/DMOS power IC technology is ideally suited for the requirements of low-power dc/dc converters, such as those required for the implementation of ISDN. A circuit design for an 85%-efficient power converter using the Si9100 SMARTPOWER IC has been presented here. Measured performance data is given, along with a graphical analysis method for ensuring reliable start-up when power is fed from a high-impedance source.

REFERENCES

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2. Sigloch, R. “Requirements for Small High Efficiency dc/dc Converters in Complex Communication Networks,” IEEE INTELEC Conference Proceedings, Toronto, Canada, Oct 19-22, 1986, 197-202.

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