

MOSFET – Single N-Channel, SUPERFET® III, FRFET® 650 V, 50 mΩ, 58 A



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NVH4L050N65S3F

Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on) max.} \times Q_{g typ.} \times R_{DS(on) max.} \times E_{OSS}$)
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	650	V
Gate-to-Source Voltage – DC	V_{GSS}	± 30	V
Gate-to-Source Voltage – AC ($f > 1$ Hz)	V_{GSS}	± 30	V
Drain Current – Continuous ($T_C = 25^\circ\text{C}$)	I_D	58	A
Drain Current – Continuous ($T_C = 100^\circ\text{C}$)	I_D	36	A
Drain Current – Pulsed (Note 3)	I_{DM}	145	A
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	403	W
Power Dissipation – Derate Above 25°C	P_D	3.23	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	830	mJ
Repetitive Avalanche Energy (Note 3)	E_{AR}	4.03	mJ
MOSFET dv/dt	dv/dt	100	V/ns
Peak Diode Recovery dv/dt (Note 5)	dv/dt	50	V/ns
Max. Lead Temperature for Soldering Purposes (1/8" from case for 5 s)	T_L	300	$^\circ\text{C}$

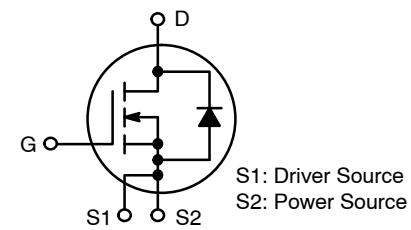
THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max. (Notes 1, 2)	$R_{\theta JC}$	0.31	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient, Max. (Notes 1, 2)	$R_{\theta JA}$	40	

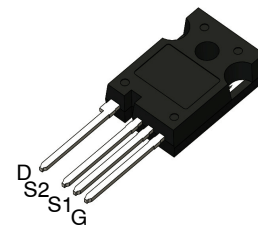
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
3. Repetitive rating: pulse-width limited by maximum junction temperature.
4. $I_{AS} = 7.5$ A, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
5. $I_{SD} \leq 29$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq 400$ V, starting $T_J = 25^\circ\text{C}$.

V_{DSS}	$R_{DS(ON) MAX}$	$I_D MAX$
650 V	50 mΩ @ 10 V	58 A

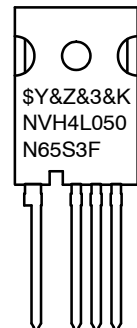


POWER MOSFET



TO-247-4LD
CASE 340CJ

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
 &Z = Assembly Plant Code
 &3 = Data Code (Year & Week)
 &K = Lot
 NVH4L050N65S3F = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NVH4L050N65S3F	TO-247-4LD (Pb-Free)	30 Units / Tube

NVH4L050N65S3F

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D = 10 mA, Referenced to 25°C		640		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 650 V			10	μA
		V _{DS} = 520 V, T _C = 125°C		19		
Gate-to-Body Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 1.7 mA	3.0		5.0	V
Threshold Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	V _{GS} = V _{DS} , I _D = 1.7 mA		-8		mV/°C
Static Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 29 A		40.4	50	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 20 V, I _D = 29 A		31.8		S

DYNAMIC CHARACTERISTICS

Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 400 V, f = 1 MHz		4855		pF
Output Capacitance	C _{oss}			112		
Reverse Transfer Capacitance	C _{rss}			14		
Effective Output Capacitance	C _{oss(eff.)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		1070		pF
Energy Related Output Capacitance	C _{oss(er.)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		198		pF
Total Gate Charge at 10 V	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 400 V, I _D = 29 A (Note 6)		123.8		nC
Threshold Gate Charge	Q _{G(TH)}			22.9		
Gate-to-Source Gate Charge	Q _{GS}			39		
Gate-to-Drain "Miller" Charge	Q _{GD}			48.6		
Equivalent Series Resistance	ESR	f = 1 MHz		1.7		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DD} = 400 V, I _D = 29 A, R _g = 2.2 Ω (Note 6)		38		ns
Turn-On Rise Time	t _r			40		
Turn-Off Delay Time	t _{d(off)}			89		
Turn-Off Fall Time	t _f			5		

SOURCE-DRAIN DIODE CHARACTERISTICS

Maximum Continuous Source-to-Drain Diode Forward Current	I _S	V _{GS} = 0 V			58	A
Maximum Pulsed Source-to-Drain Diode Forward Current	I _{SM}	V _{GS} = 0 V			145	A
Source-to-Drain Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 29 A			1.3	V
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, di _F /dt = 100 A/μs, I _{SD} = 29 A		129		ns
Charge Time	t _a			110		
Discharge Time	t _b			19		
Reverse Recovery Charge	Q _{rr}			588		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

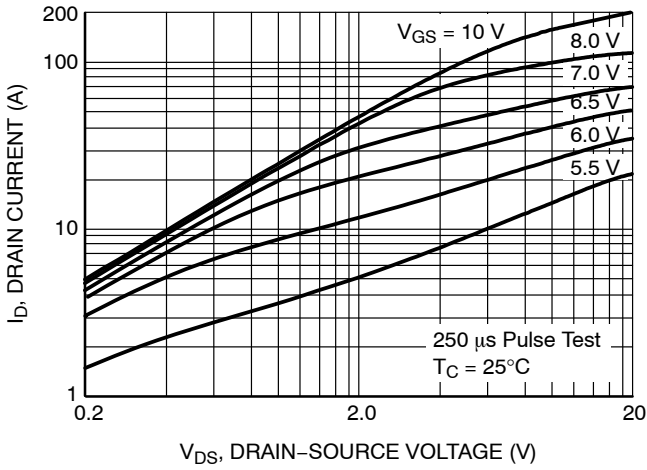


Figure 1. On-Region Characteristics

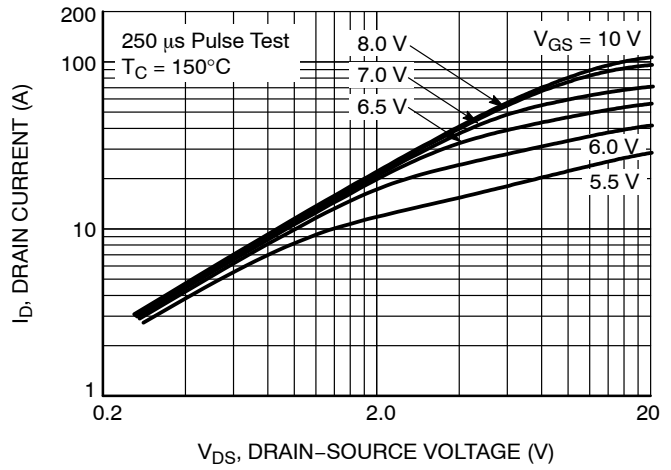


Figure 2. On-Region Characteristics

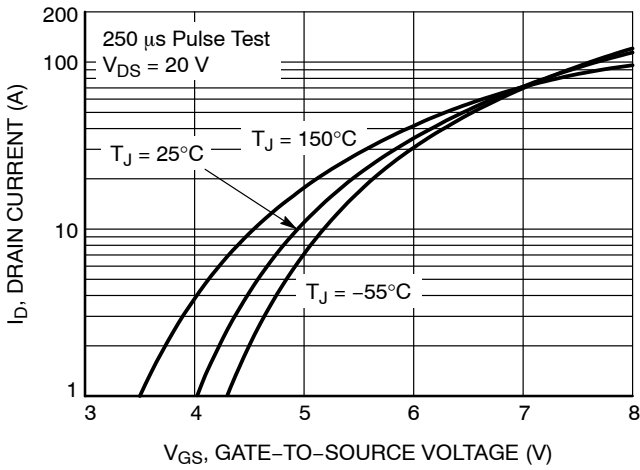


Figure 3. Transfer Characteristics

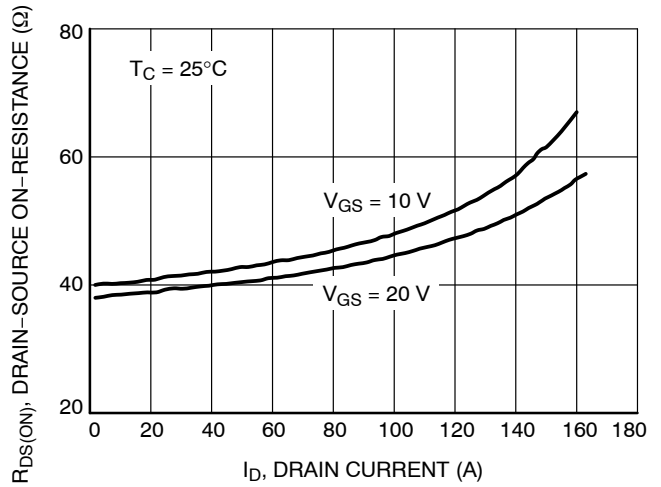


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

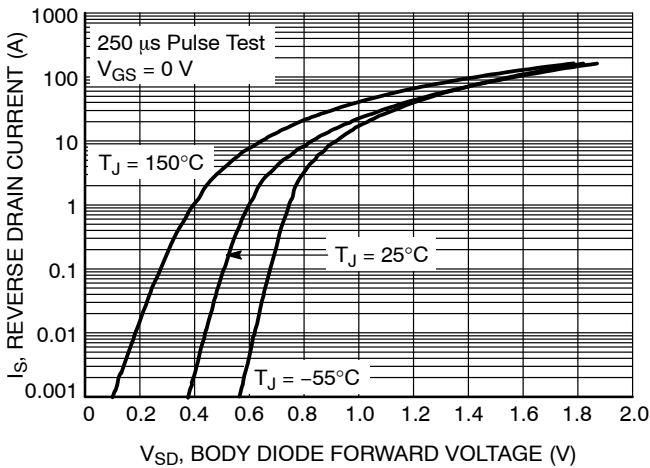


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

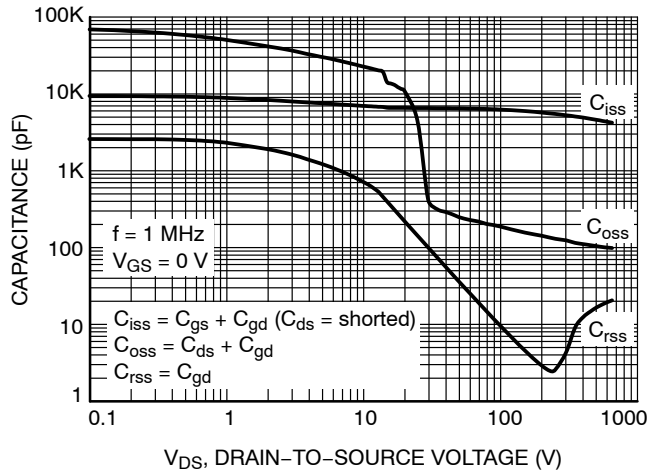


Figure 6. Capacitance Characteristics

NVH4L050N65S3F

TYPICAL CHARACTERISTICS

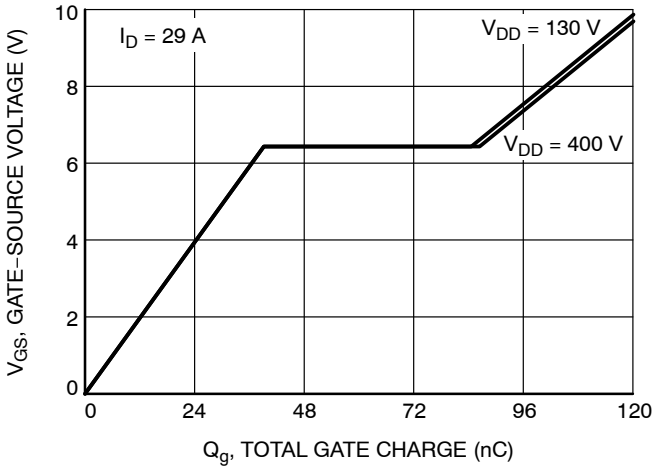


Figure 7. Gate Charge Characteristics

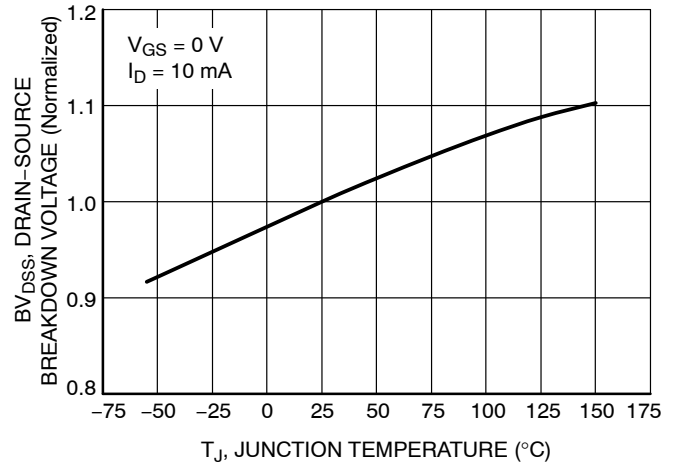


Figure 8. Breakdown Voltage Variation vs. Temperature

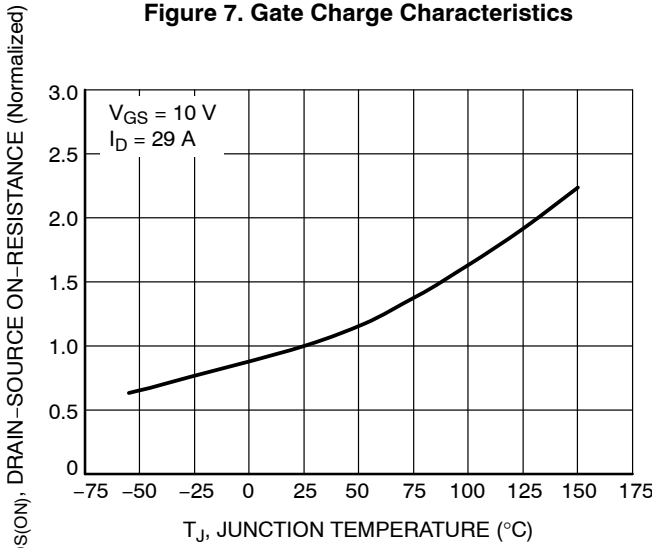


Figure 9. On-Resistance Variation vs. Temperature

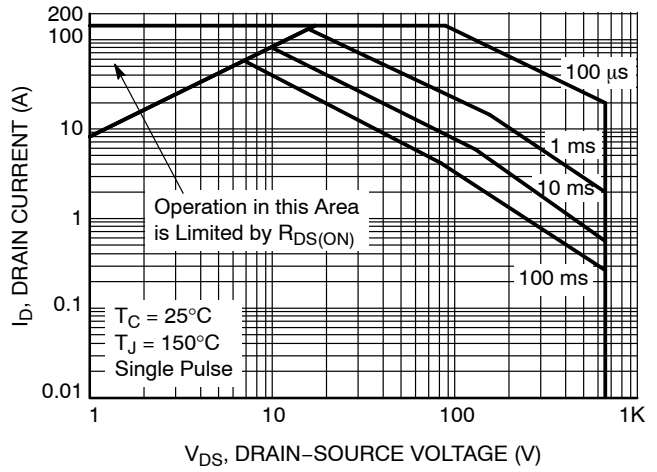


Figure 10. Maximum Safe Operating Area

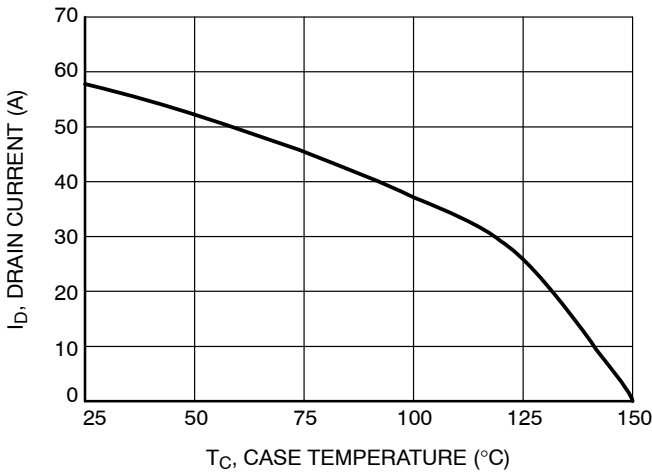


Figure 11. Maximum Drain Current vs. Case Temperature

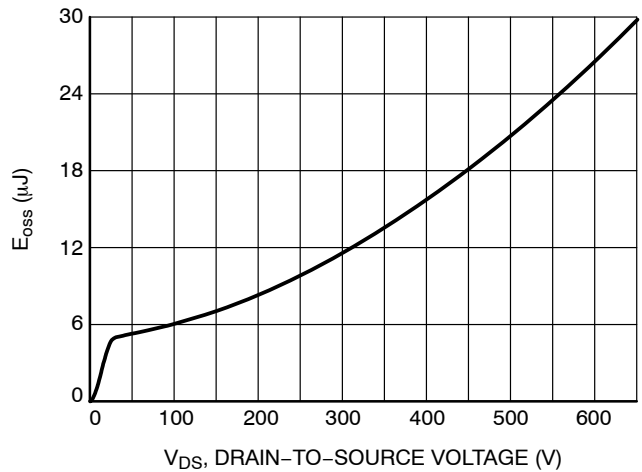


Figure 12. E_OSS vs. Drain-to-Source Voltage

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TYPICAL CHARACTERISTICS

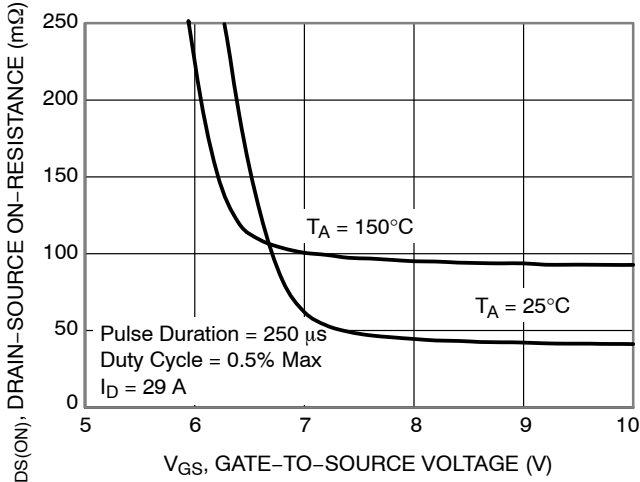


Figure 13. $R_{DS(ON)}$ vs. Gate Voltage

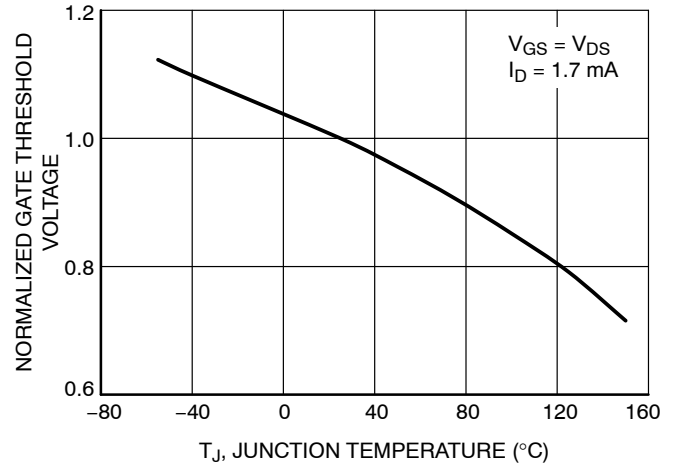


Figure 14. Normalized Gate Threshold Voltage vs. Temperature

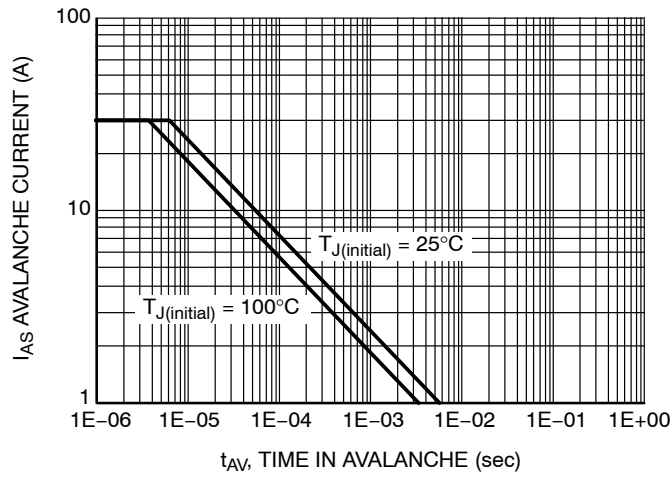


Figure 15. Unclamped Inductive Switching Capability

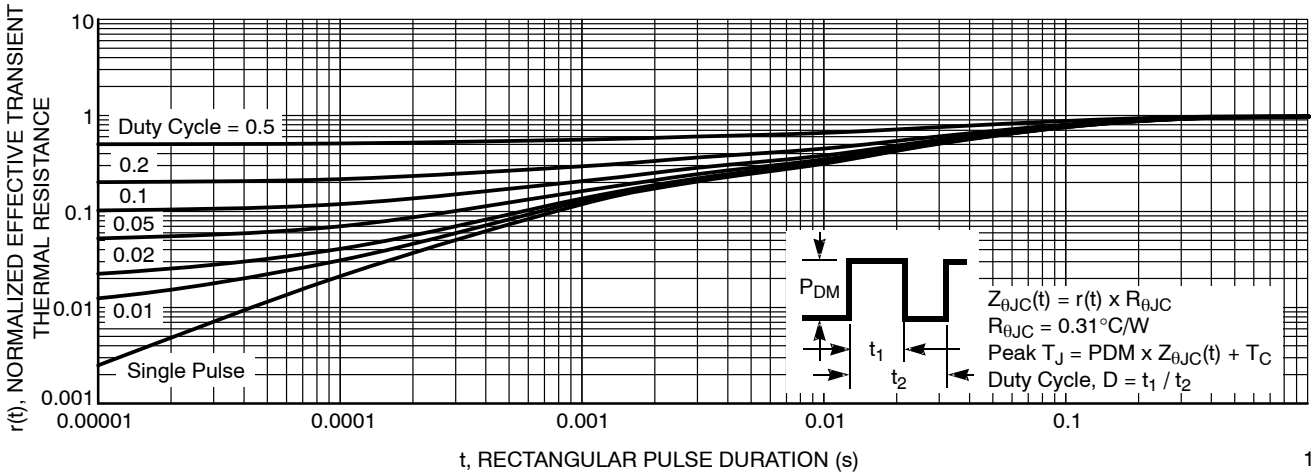


Figure 16. Transient Thermal Response Curve

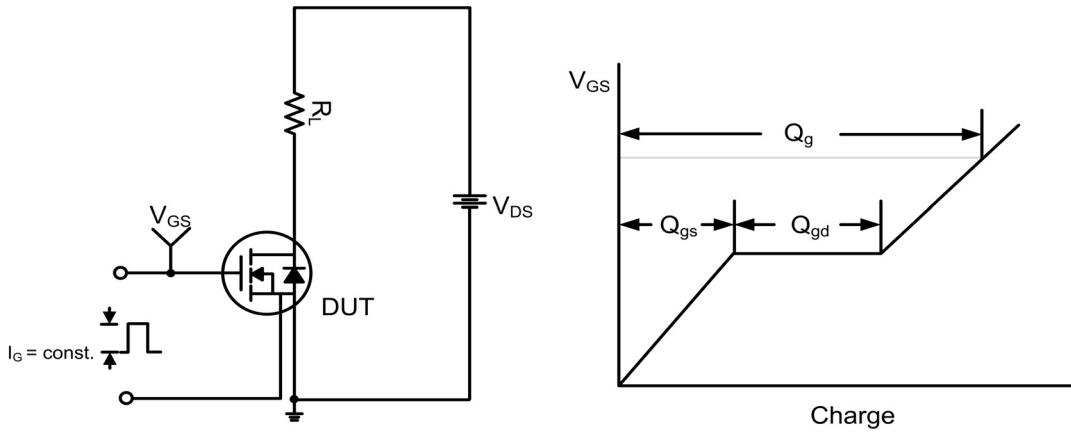


Figure 17. Gate Charge Test Circuit & Waveform

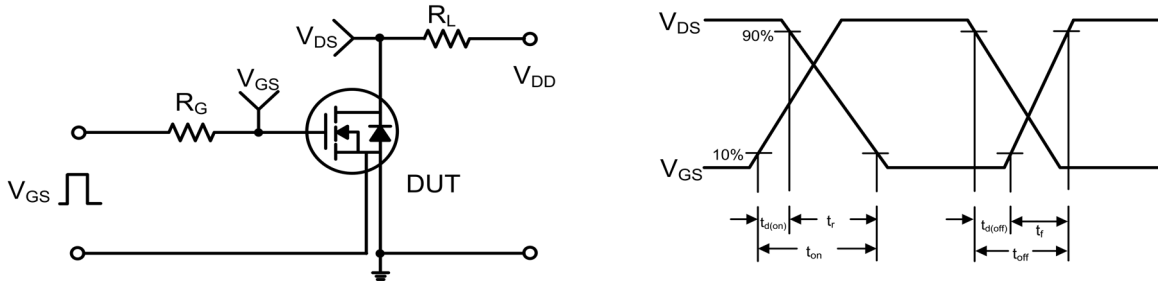


Figure 18. Resistive Switching Test Circuit & Waveforms

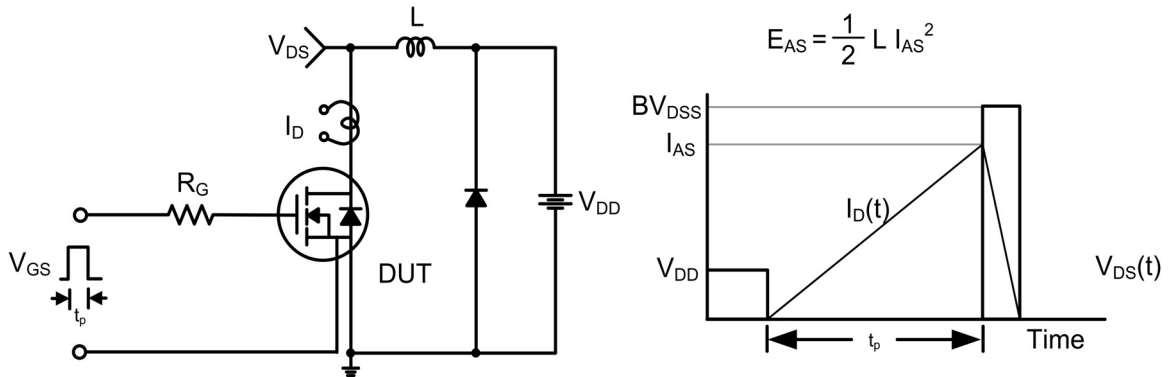


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

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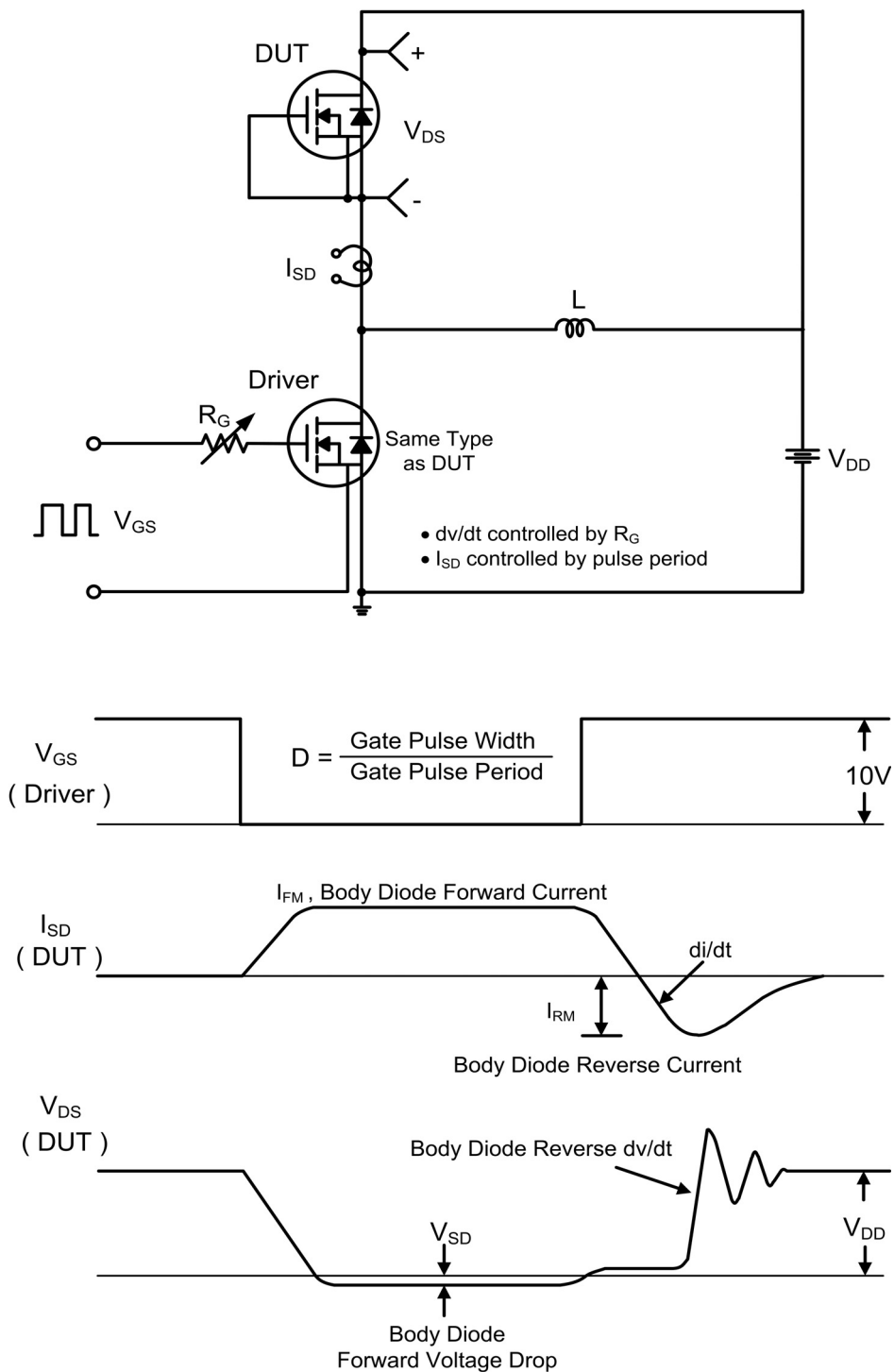


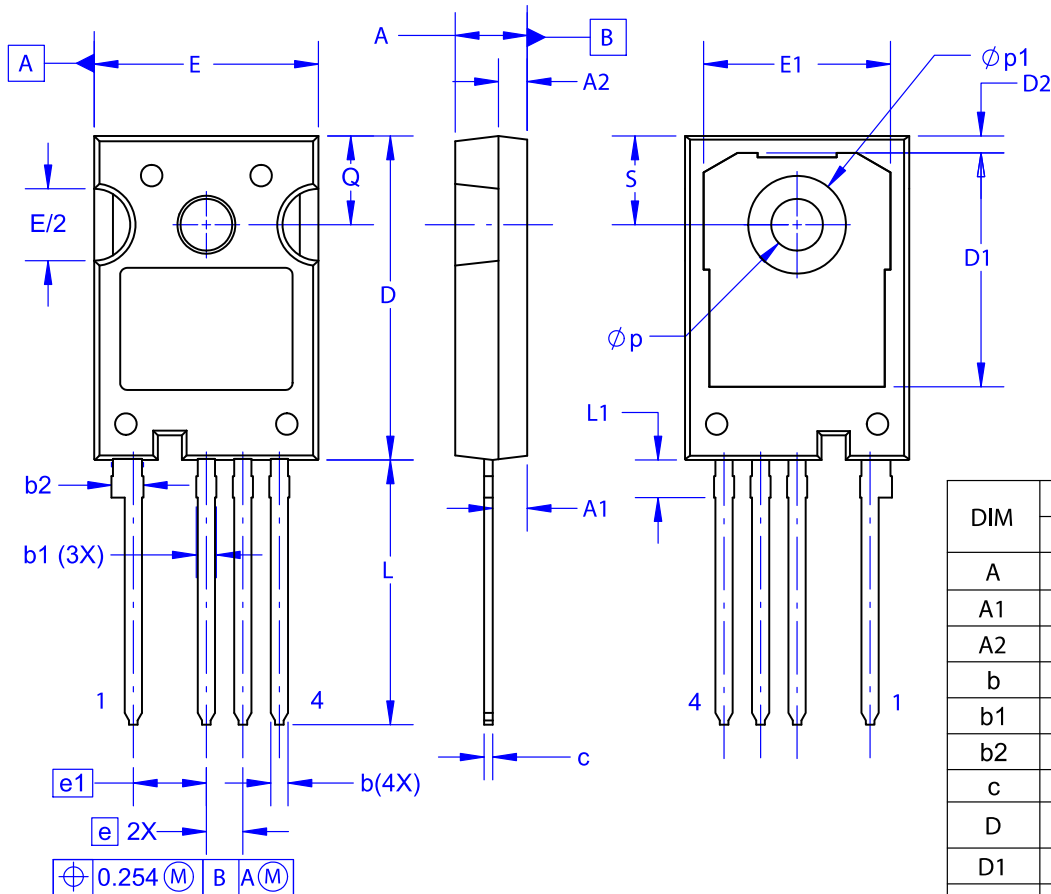
Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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PACKAGE DIMENSIONS


TO-247-4LD
CASE 340CJ
ISSUE A



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.10	2.40	2.70
A2	1.80	2.00	2.20
b	1.07	1.20	1.33
b1	1.20	1.40	1.60
b2	2.02	2.22	2.42
c	0.50	0.60	0.70
D	22.34	22.54	22.74
D1	16.00	16.25	16.50
D2	0.97	1.17	1.37
e	2.54 BSC		
e1	5.08 BSC		
E	15.40	15.60	15.80
E1	12.80	13.00	13.20
E/2	4.80	5.00	5.20
L	18.22	18.42	18.62
L1	2.42	2.62	2.82
p	3.40	3.60	3.80
p1	6.60	6.80	7.00
Q	5.97	6.17	6.37
S	5.97	6.17	6.37

NOTES:

- A. NO INDUSTRY STANDARD APPLIES TO THIS PACKAGE.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5-2009.

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