MP1909

30V, 2.2MHz, 2A Half-Bridge Gate Driver in SOT583 Package

DESCRIPTION

The MP1909 is a high-frequency, 30V, half-bridge, N-channel power MOSFET driver. Its low-side and high-side driver channels are controlled by a signal input. Internal adaptive dead time control circuitry reduces the switching power loss and prevents shoot-through.

Both outputs are disabled when the EN pin is pulled low. The integrated bootstrap diode reduces external component count. Under-voltage lockout (UVLO) functionality protects the IC from operating at insufficient power supplies. Thermal shutdown protection functions can protect the IC from over-temperature conditions.

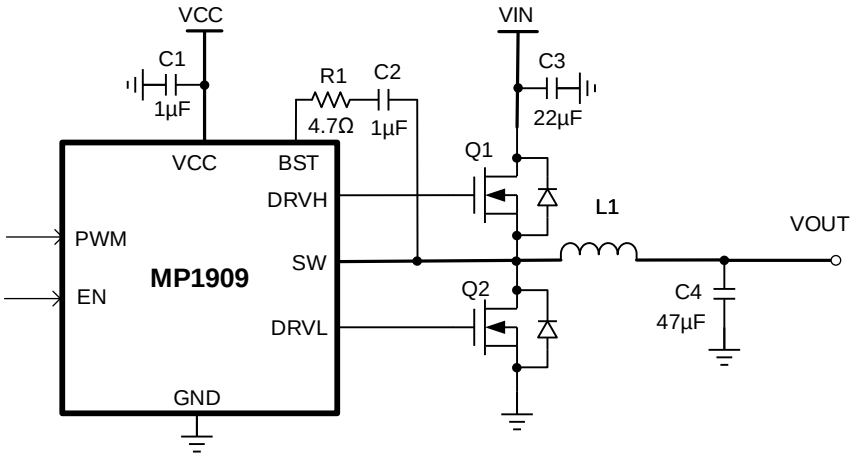
FEATURES

- Drives N-Channel MOSFET Half-Bridge
- Up to 50V V_{BST} Voltage
- 4.5V to 12V Gate Drive Voltage
- On-Chip Bootstrap Diode
- Up to 2.2MHz Switching Frequency
- One PWM Signal Generates Both Drives
- Low Quiescent Current
- 100% Duty Support
- UVLO for High-Side and Low-Side Gate Drives
- Available in an 8-Pin SOT583 (1.6mmx2.1mm) Package

APPLICATIONS

- Electronic Cigarettes
- Wireless Charging
- Drones
- Avionics DC/DC Converters
- Active-Clamp Forward Converters

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MP1909GTL	SOT583	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP1909GTL–Z).

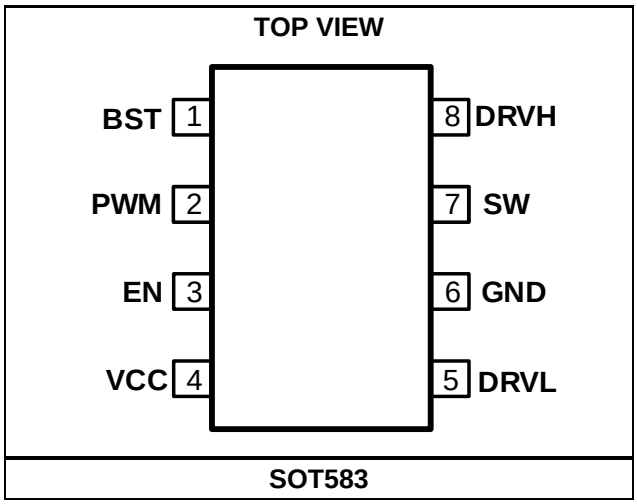
TOP MARKING

BFZY

LLL

BFZ: Product code of MP1909GTL
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between the BST and SW pins.
2	PWM	**Control signal input for the high-side and low-side drivers**. Setting PWM to logic high turns on the high-side MOSFET; setting PWM to logic low turns on the low-side MOSFET.
3	EN	**On/off control.** Set EN high to turn on the IC; set EN low to turn it off.
4	VCC	**Supply input.** This pin supplies power to all the internal circuitry. Place a decoupling capacitor to ground, and close to this pin to ensure stable and clean supply.
5	DRVL	**Low-side driver output.**
6	GND	**Chip ground.**
7	SW	**Switching node.**
8	DRVH	**Floating driver output.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{CC}) .....-0.3V to +15V
SW voltage (V_{SW}).....-0.3V (-5V <10ns)
..... to +35V (45V <10ns)
BST voltage (V_{BST}) .....-0.3V to +50V
BST to SW .....-0.3V to +15V
DRVH to SW..... -0.3V to (BST-SW) + 0.3V
DRVL to GND ..... -0.3V to (V_{CC} + 0.3V)
EN, PWM .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) (5)
.....2.2W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 1000V
Charged device model (CDM).....1000V

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) ..... 4.5V to 12V (4)
Power input voltage (V_{IN}) .....0.8V to 30V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOT583		
EV1909-TL-00A (5)	55	21 °C/W
JESD51-7 (6)	130	60 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) 4.5V/12V is only a typical value for the supply voltage.
5) Measured on EV1909-TL-00A, 2-layer PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{CC} = V_{BST} - V_{SW} = 12V, V_{EN} = 3.3V, V_{PWM} = 3.3V, no load at DRVH and DRVL, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
VCC shutdown current	I_{SHDN}	V_{EN} = 0, SW = GND, T_J = 25°C		100	165	µA
		V_{EN} = 0, SW = GND, T_J = -40°C to +125°C			180	µA
		V_{EN} = 0, SW float, T_J = 25°C		50	100	µA
		V_{EN} = 0, SW float, T_J = -40°C to +125°C			120	µA
VCC quiescent current	I_{DDQ1}	PWM = 0, SW = GND, V_{EN} = 3.3V		150	230	µA
		PWM = 0, SW float, V_{EN} = 3.3V		100	170	µA
VCC operating current	I_{DDQ2}	f_{SW} = 250kHz, C_{LOAD} = 1nF		7.5	9.5	mA
Floating driver quiescent current	I_{BSTQ}	PWM = high		110	170	µA
Leakage current	I_{LK}	BST = 35V, SW = 35V			1	µA
Inputs						
PWM high	V_{PWM_H}		2.2			V
PWM low	V_{PWM_L}				0.8	V
PWM hysteresis	V_{PWM_HYS}			0.5		V
PWM leakage current	I_{PWM}	No internal pull-up or pull-down, V_{PWM} = 3.3V	-1		+1	µA
Under-Voltage Protection						
VCC rising threshold	V_{CCR}		3.6	4.1	4.6	V
VCC falling threshold	V_{CCF}		3.6	3.8	4.2	V
(BST-SW) rising threshold	V_{BSTR}		2.4	2.9	3.4	V
(BST-SW) falling threshold	V_{BSTF}			2.8		V
EN input logic low	V_{EN_L}				0.7	V
EN input logic high	V_{EN_H}		1.5			V
EN hysteresis	V_{EN_HYS}			300		mV
EN internal pull-down resistance	R_{EN}			1		MΩ
EN turn-on delay	t_{EN_ON}	BST - SW = 12V		3.6		µs
EN shutdown delay	t_{EN_OFF}			20		ns
Bootstrap Diode						
Bootstrap diode VF at 100µA	V_{F1}			0.2		V
Bootstrap diode VF at 100mA	V_{F2}			1.6		V
Bootstrap diode dynamic R	R_D	At 100mA		13		Ω
Low-Side Gate Driver						
Output resistance, sourcing current	R_{OHL}	V_{PWM} = 0V, V_{CC} = 5V		4		Ω
		V_{PWM} = 0V, V_{CC} = 12V		1.5		Ω
	I_{OHL} (8)	V_{PWM} = 0V, V_{CC} = 12V		2		A

ELECTRICAL CHARACTERISTICS *(continued)*

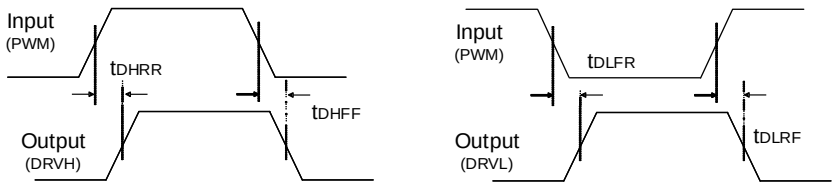
V_{CC} = V_{BST} - V_{SW} = 12V, V_{EN} = 3.3V, V_{PWM} = 3.3V, no load at DRVH and DRVL, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output resistance, sinking current	R_{OLL}	V_{PWM} = 3.3V, V_{CC} = 5V		1		Ω
		V_{PWM} = 3.3V, V_{CC} = 12V		0.6		Ω
	I_{OLL} [8]	V_{PWM} = 3.3V, V_{CC} = 12V		4		A
Output resistance, unbiased	R_{OUL}	V_{CC} = GND		250		kΩ
Floating Gate Driver						
Output resistance, source current	R_{OHH}	V_{PWM} = 3.3V, V_{BST} - V_{SW} = 5V		4		Ω
		V_{PWM} = 3.3V, V_{BST} - V_{SW} = 12V		2		Ω
Output resistance, sink current	R_{OLH}	V_{PWM} = 0V, V_{BST} - V_{SW} = 5V		1.2		Ω
		V_{PWM} = 0V, V_{BST} - V_{SW} = 12V		0.6		Ω
Output resistance, unbiased	R_{OUH}	V_{BST} - V_{SW} = 0V		250		kΩ
Switching Specifications (Low-Side Gate Driver)						
Turn-off propagation delay, PWM rising to DRVL falling	t_{DLRF}			30		ns
Turn-on propagation delay, PWM falling to DRVL rising	t_{DLFR}			110		ns
DRVL rise time [8]	t_{DRVL_R}	C_L = 1nF		10		ns
DRVL fall time [8]	t_{DRVL_F}	C_L = 1nF		6		ns
Switching Specifications (Floating Gate Driver)						
Turn-off propagation delay, PWM falling to DRVH falling	t_{DHFF}			40		ns
Turn-on propagation delay, PWM rising to DRVH rising	t_{DHRR}			80		ns
DRVH rise time [8]	t_{DRVH_R}	C_L = 1nF		10		ns
DRVH fall time [8]	t_{DRVH_F}	C_L = 1nF		6		ns
Switching Specifications (Matching)						
Minimum input pulse width that changes the output [8]	t_{PW}			50		ns
Thermal shutdown [8]	T_{STD}			150		°C
Thermal hysteresis [8]	T_{STD_HYS}			20		°C

Notes:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by design and engineering sample characterization.

TIMING DIAGRAM

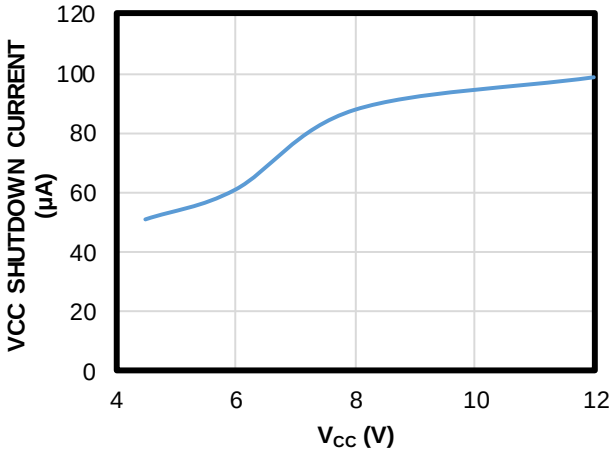


TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

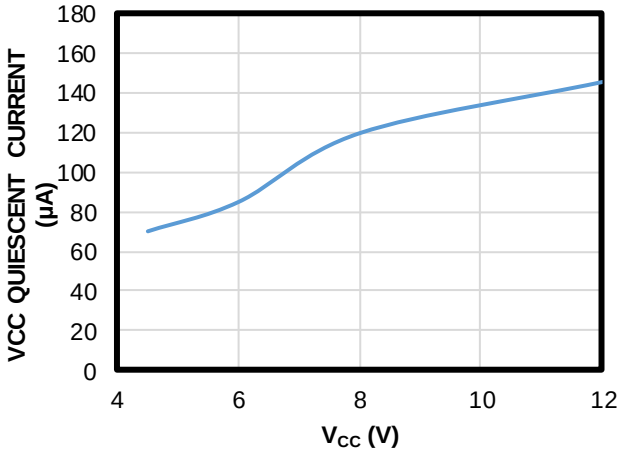
VCC Shutdown Current

V_{EN} = 0V, short SW to GND



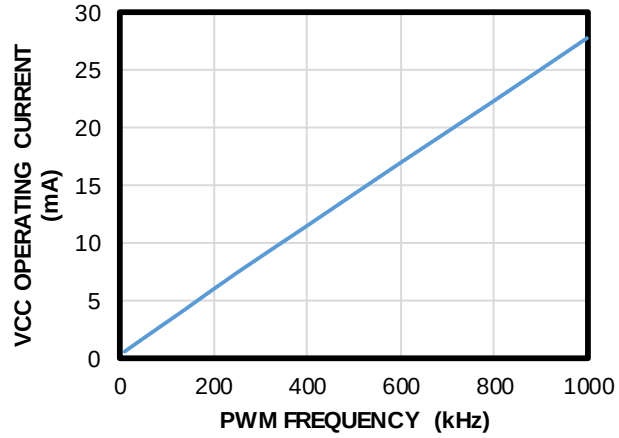
VCC Quiescent Current

V_{EN} = 3.3V, V_{PWM} = 0V, short SW to GND

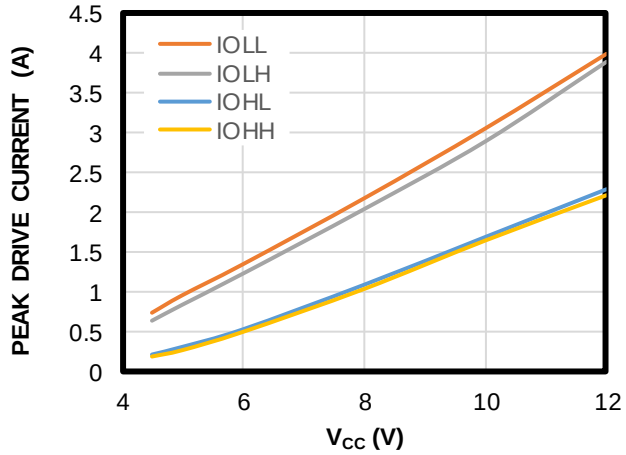


VCC Operating Current

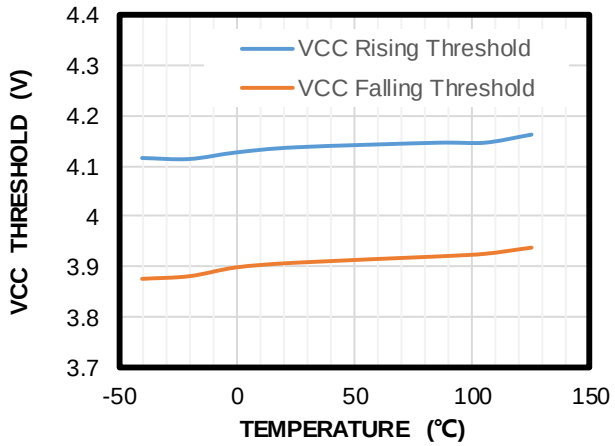
V_{CC} = 12V, C_{LOAD} = 1nF at DRVH and DRVL



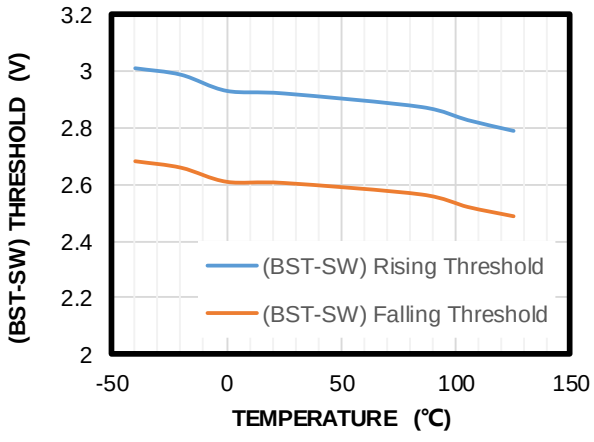
Peak Drive Current vs. VCC Voltage



VCC Threshold vs. Temperature



(BST-SW) Threshold vs. Temperature

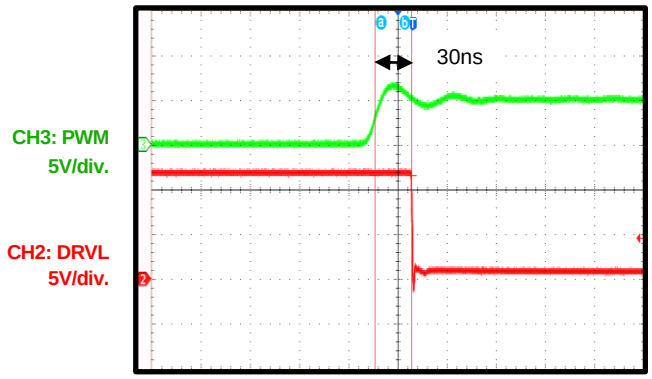


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

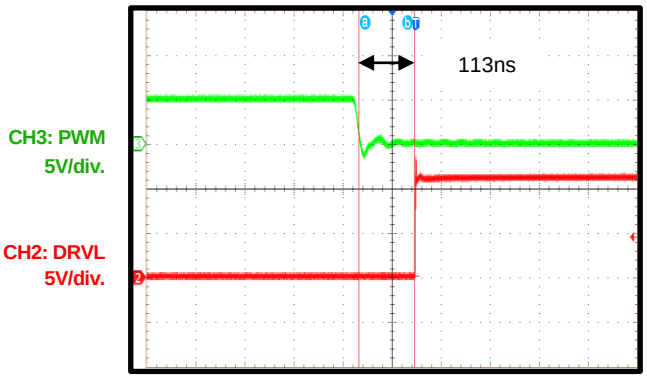
Turn-Off Propagation Delay

PWM rising to DRVL falling



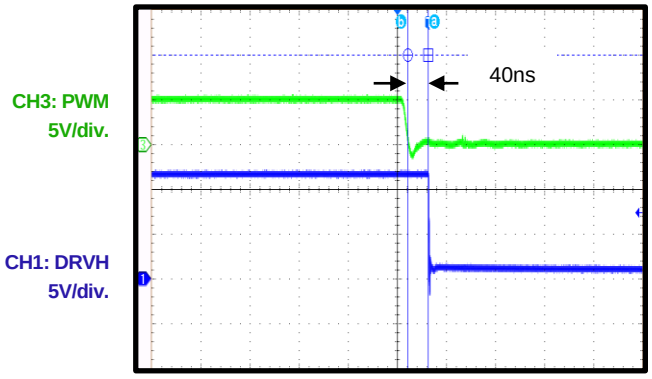
Turn-On Propagation Delay

PWM falling to DRVL rising



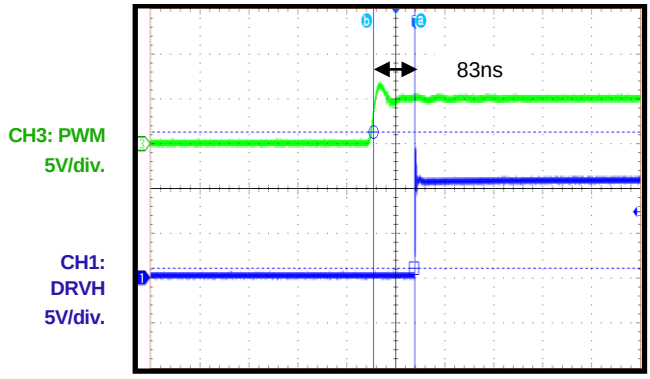
Turn-Off Propagation Delay

PWM falling to DRVH falling



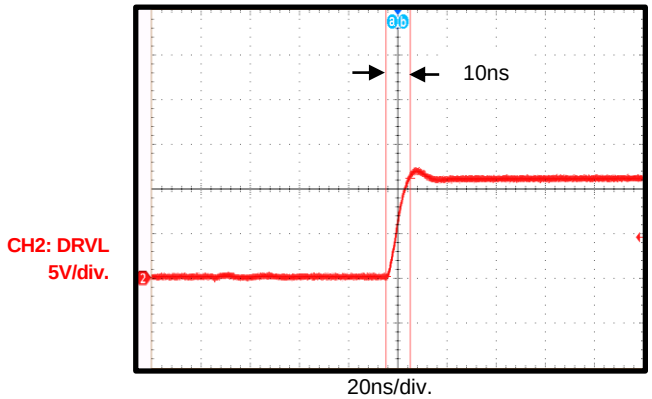
Turn-On Propagation Delay

PWM rising to DRVH rising



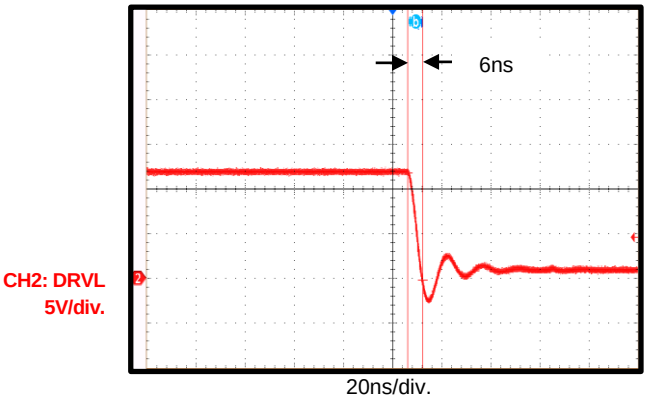
DRVL Rising Time

C_{LOAD} = 1nF



DRVL Falling Time

C_{LOAD} = 1nF

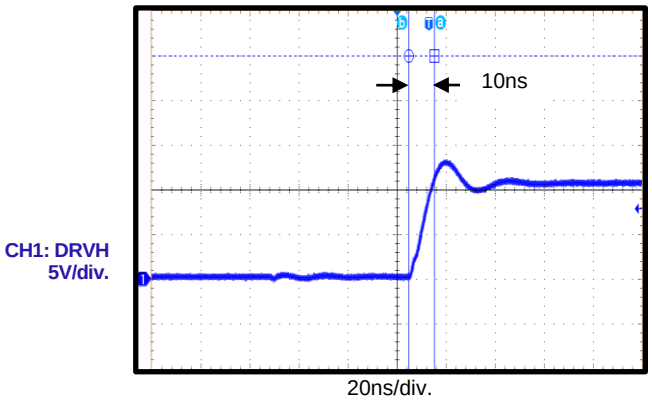


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

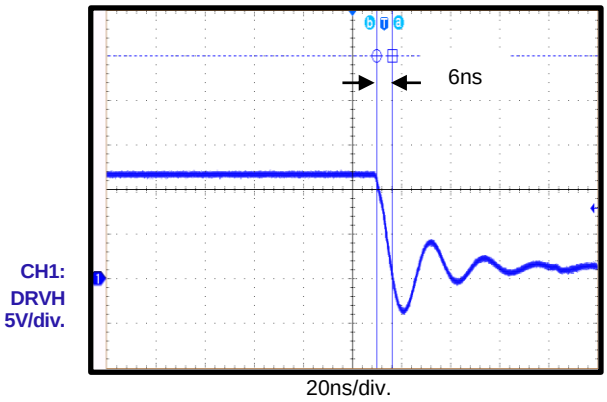
DRVH Rising Time

C_{LOAD} = 1nF



DRVH Falling Time

C_{LOAD} = 1nF



FUNCTIONAL BLOCK DIAGRAM

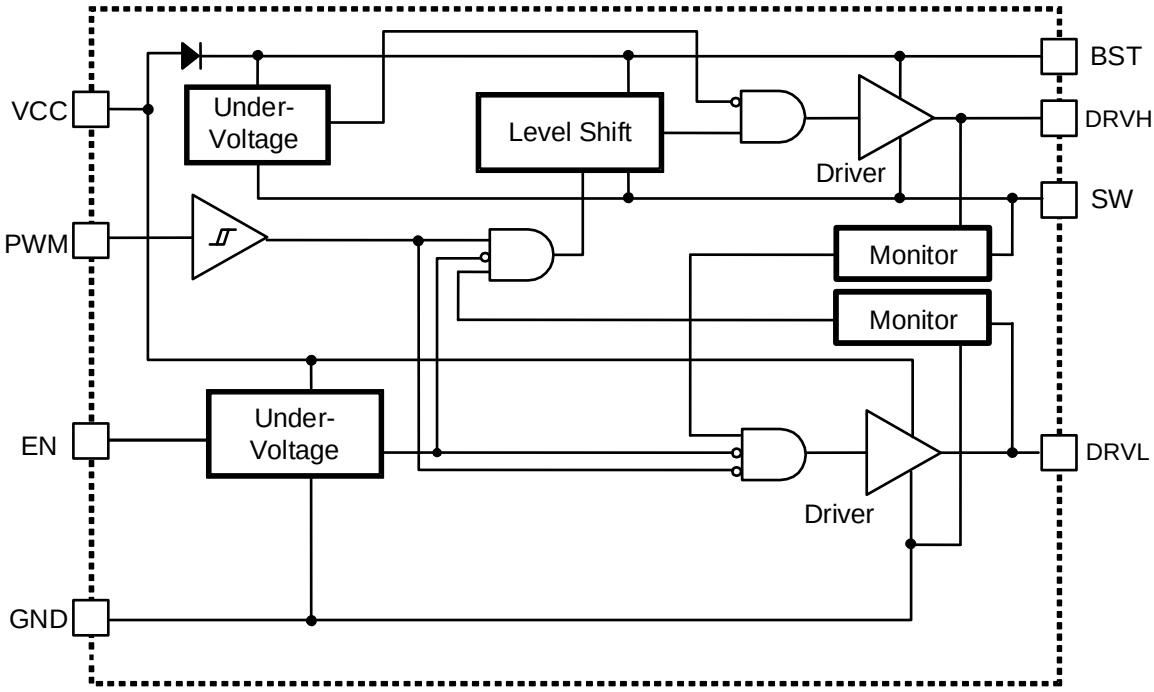


Figure 2: Functional Block Diagram

OPERATION

Theory of Operation

The MP1909 can drive two N-channel MOSFETs in a synchronous buck or boost converter topology. It can work at a 12V gate drive voltage to minimize the external MOSFET's $R_{DS(ON)}$ and achieve higher efficiency. A single PWM input signal can generate the well-controlled high-side and low-side drivers.

100% Duty Cycle

The high-side driver can turn on with 100% duty cycle as long as the difference between V_{CC} and V_{IN} exceeds 3.4V.

Switch Shoot-Through Protection

Internal anti-shoot-through circuitry protects the high-side and low-side MOSFETs from turning on at the same time. Adaptive dead time control greatly reduces the dead time and switching power loss.

When the PWM input goes high, the DRVL pin goes low. The time it takes for the low-side MOSFET (LS-FET) to turn off is determined by the total gate charge. The MP1909 monitors the LS-FET's V_{GS} and level shifts this voltage information to the high-side driver. The high-side driver does not turn on the high-side MOSFET (HS-FET) until the LS-FET is completely turned off.

Under-Voltage Lockout

When BST-SW goes below its under-voltage lockout (UVLO) threshold, the DRVH pin's output goes low to turn off the HS-FET.

When V_{CC} falls below its UVLO threshold, both the DRVH and DRVL outputs go low to turn off the MOSFETs.

Table 1 lists the operation of the HS-FET and LS-FET under different PWM and UVLO conditions.

Table 1: States of Driver Outputs under Different Conditions

EN	BST-SW Voltage	V_{CC} Voltage	PWM	DRVH	DRVL	Operating Conditions
0	X	X	X	250kΩ pull-down resistor	250kΩ pull-down resistor	X
1	Above UVLO	Above UVLO	1	1	0	Normal operation
	Above UVLO	Above UVLO	0	0	1	
	Falls below UVLO	Above UVLO	1	0	0	
	Falls below UVLO	Above UVLO	0	0	1	
	Above UVLO	Falls below UVLO	X	0	0	Normal-to-tripped transition
	Below UVLO	Falls below UVLO	X	0	0	

Note:

9) "X" means not applicable.

APPLICATION INFORMATION

It is not recommended to add a resistor (R_{GATE}) between DRVH/DRVL and the MOSFET gate. If R_{GATE} is required to slow down the MOSFET's turn-on speed, a turn-off diode must be placed within the system. Figure 3 shows the turn-off diode circuit. This circuit significantly reduces the turn-off delay time, which reduces the risk of shoot-through.

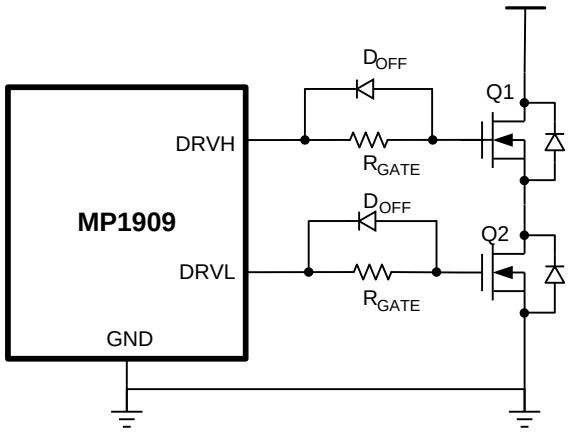


Figure 3: Turn-Off Diode Circuit

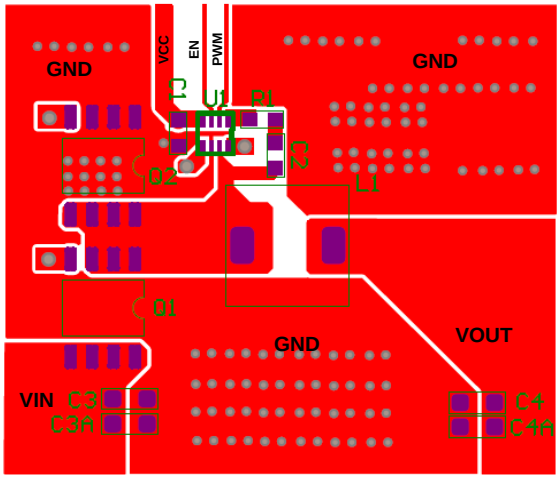
PCB Layout Guidelines (10)

Proper PCB layout of the driver is very important. For the best results, refer to Figure 4 and follow the guidelines below:

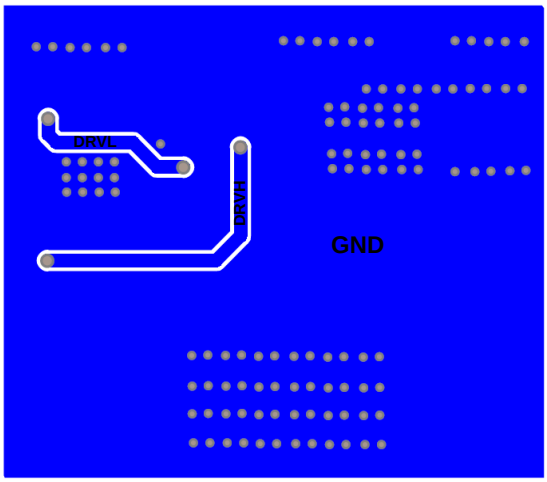
1. Put the VCC capacitor close to VCC and GND pins.
2. Use wide PCB traces to connect the MP1909 to the GND pin.
3. Place the BST capacitor close to the BST and SW pins. A 4.7Ω BST resistor is recommended to reduce the spike voltage.
4. Use wide and short PCB traces to connect DRVH/DRVL to the MOSFET gate.

Note:

10) The recommended layout is based on the circuit on Figure 5.



Top Layer



Bottom Layer

Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

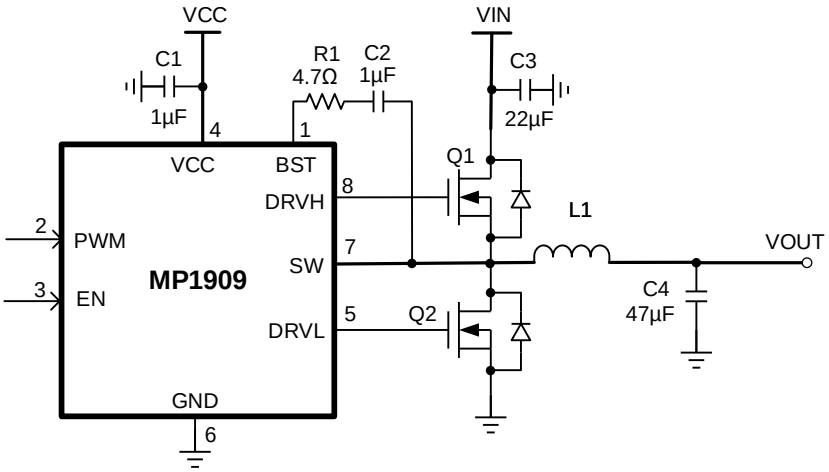


Figure 5: Buck Driver

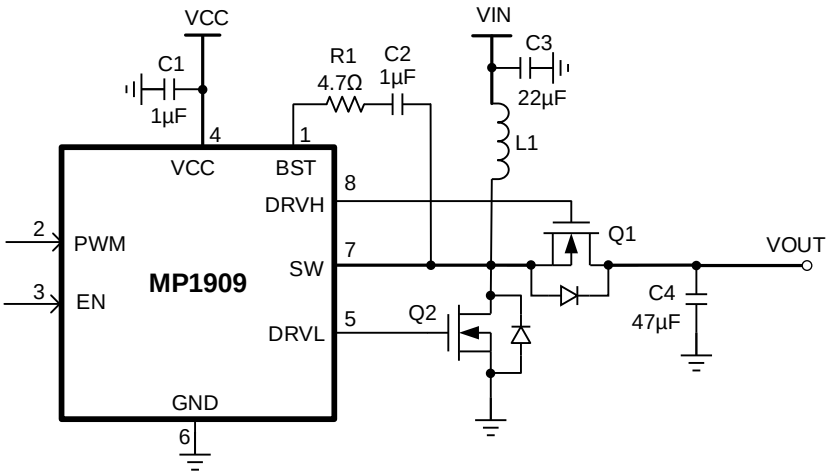
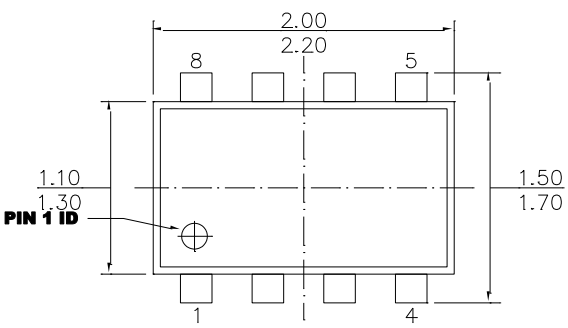


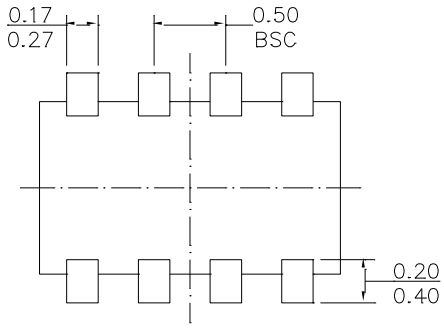
Figure 6: Boost Driver

PACKAGE INFORMATION

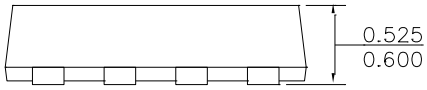
SOT583 (1.6mmx2.1mm)



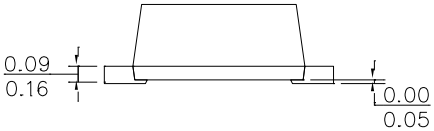
TOP VIEW



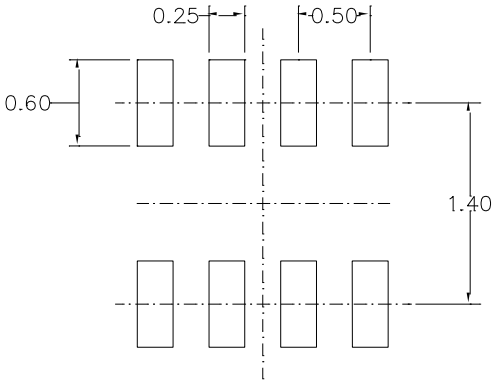
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

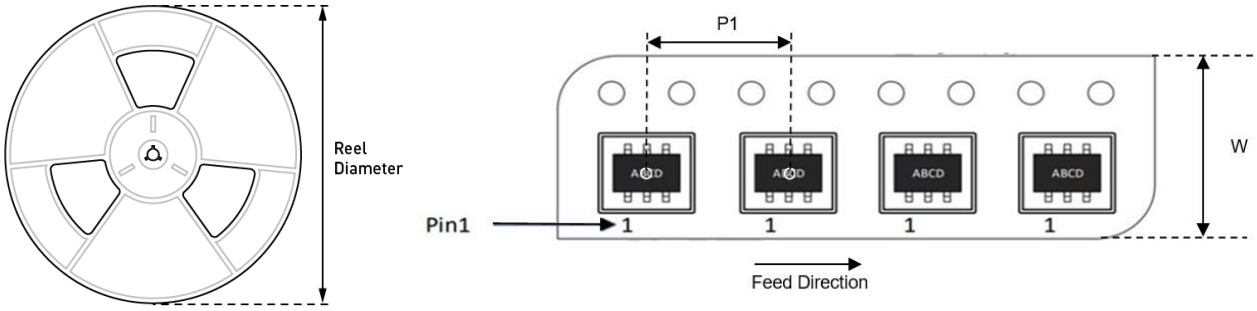


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP1909GTL–Z	SOT583	5000	N/A	7in	8mm	4mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	7/10/2020	Initial Release	-