Data Sheet

ADCA3280

DOCSIS 4.0, 24 V Power Doubler Amplifier, 45 MHz to 1794 MHz

FEATURES

- Excellent linearity for TCP up to 75 dBmV
- Power gain: 22.7 dB at 1794 MHz
- S11: <−17 dB from 108 MHz to 1794 MHz
- S22: <−19 dB from 108 MHz to 1794 MHz
- Flexible supply voltage range: 24 V to 18 V
- Adjustable supply current: 570 mA to 450 mA
- Internal precision voltage reference to improve current stability over process and temperature
- Internal temperature monitor
- Industry standard, 9-terminal, 9 mm x 8 mm LGA_CAV, surface-mounted package
- Excellent thermal conductivity

APPLICATIONS

- 258 MHz to 1794 MHz extended spectrum CATV infrastructure amplifier systems
- 108 MHz to 1218 MHz CATV infrastructure amplifier systems
- Remote nodes
- DOCSIS 3.1 and 4.0 compliant

FUNCTIONAL BLOCK DIAGRAM

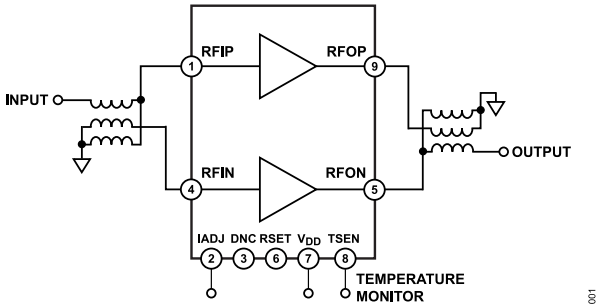


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADCA3280 is a power doubler with 22.7 dB of power gain at 1794 MHz designed for operation in 24 V applications. The amplifier can also be operated with a lower supply voltage, providing superior efficiency as seen in Figure 10, Figure 17, and Figure 20. The device achieves high RF output up to 75 dBmV total composite power (TCP) with excellent noise power ratio (NPR), or equivalently modulation error ratio (MER), with channel loading to 1.8 GHz as well as 1.2 GHz, making it an ideal output stage device for DOCSIS 4.0 as well as DOCSIS 3.1 equipment. The DC current and supply voltage can be adjusted externally for optimum distortion performance vs. power consumption over a range of output levels. The ADCA3280 provides high performance, simplifying the design and manufacturing of DOCSIS 3.1 and DOCSIS 4.0 infrastructure equipment.

The ADCA3280 is packaged in an industry standard 9-terminal, 9 mm x 8 mm LGA package.

Rev. A

TABLE OF CONTENTS

REVISION HISTORY

8/2023—Rev. 0 to Rev. A

Change to Features Section ... 1

7/2023—Revision 0: Initial Version

SPECIFICATIONS

GENERAL PERFORMANCE

Using the application circuit shown in Figure 24. Supply voltage (V_{DD}) = 21 V, paddle temperature (T_{PADDLE}) = 35°C, source impedance (Z_S) = load impedance (Z_L) = 75 Ω, and DC current (I_{DD}) = 540 mA, unless otherwise noted. Device performance is similar at 24 V.

Table 1. General Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER GAIN	S21		21.3		dB	Frequency = 108 MHz
			21.4		dB	Frequency = 258 MHz
			21.7		dB	Frequency = 1218 MHz
			22.7		dB	Frequency = 1794 MHz
SLOPE OF STRAIGHT LINE[1]			0.4		dB	Frequency = 108 MHz to 1218 MHz
			1.3		dB	Frequency = 108 MHz to 1794 MHz
FLATNESS OF FREQUENCY RESPONSE[2]			0.1		dB	Frequency = 108 MHz to 1218 MHz
			0.35		dB	Frequency = 108 MHz to 1794 MHz
REVERSE ISOLATION	S12		−26.5		dB	Frequency = 108 MHz to 1794 MHz
RETURN LOSS						See Figure 3 and Figure 6
Input	S11		−20		dB	Frequency = 108 MHz to 258 MHz
			−17		dB	Frequency = 258 MHz to 870 MHz
			−17		dB	Frequency = 870 MHz to 1218 MHz
			−17		dB	Frequency = 1218 MHz to 1794 MHz
Output	S22		−20		dB	Frequency = 108 MHz to 258 MHz
			−19		dB	Frequency = 258 MHz to 870 MHz
			−19		dB	Frequency = 870 MHz to 1218 MHz
			−19		dB	Frequency = 1218 MHz to 1794 MHz
NOISE FIGURE						Includes losses of baluns shown in Figure 24
			2.8		dB	Frequency = 108 MHz
			3.3		dB	Frequency = 1218 MHz
			4.6		dB	Frequency = 1794 MHz
SUPPLY						Supply voltage and current can be adjusted for different applications, see the Applications Information section
DC Current	I_{DD}		540		mA	See the Supply Voltage and Current section for information on current adjustment

[1] The slope is defined as the delta of the gain at the start frequency and the gain at the stop frequency.

[2] Flatness is defined as the maximum deviation from a linear best-fit of the gain in the frequency range of operation.

SPECIFICATIONS

DISTORTION DATA

Downstream All Digital Channel Plan, 8× Orthogonal Frequency Division Multiplexing (OFDM) Channels, 258 MHz to 1794 MHz

Using the application circuit shown in Figure 24. V_{DD} = 21 V, I_{DD} = 540 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted. Device performance is similar to 24 V, as shown in Figure 10.

Table 2. DOCSIS4.0 Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR		48		dB	20 dB tilt, 6 dB offset at 1026 MHz, TCP = 74 dBmV, frequency = 273 MHz, see Figure 7
			46		dB	20 dB tilt, 6 dB offset at 1026 MHz, TCP = 74 dBmV, frequency = 1041 MHz, see Figure 7
			47.5		dB	20 dB tilt, 6 dB offset at 1026 MHz, TCP = 74 dBmV, frequency = 1773 MHz, see Figure 7
BIT ERROR RATE	BER		$<1 \times 10^{-10}$			Pre-forward error correction (Pre-FEC) errors, 20 dB tilt, 6 dB offset at 1026 MHz, TCP = 74 dBmV, 4096 QAM

[1] The noise power ratio gives an equivalent result to the standard modulation error rate (MER) testing but with improved dynamic range using an industry-accepted method.

Downstream All Digital Channel Plan, 190×, ITU-T J.83B, Single-Channel Quadrature Amplitude Modulation (SCQAM) 6 MHz Channels, 54 MHz to 1218 MHz

Using the application circuit shown in Figure 24. V_{DD} = 21 V, I_{DD} = 540 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted. Device performance is similar at 24 V, as shown in Figure 17 and Figure 20.

Table 3. DOCSIS3.1 Distortion Data

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE POWER RATIO[1]	NPR					
			48		dB	13 dB tilt, TCP = 74 dBmV, frequency = 111 MHz, see Figure 13 and Figure 14
			56		dB	13 dB tilt, TCP = 74 dBmV, frequency = 1218 MHz, see Figure 13 and Figure 14
			44		dB	18 dB tilt, TCP = 74 dBmV, frequency = 111 MHz, see Figure 11 and Figure 12
			57		dB	18 dB tilt, TCP = 74 dBmV, frequency = 1218 MHz, see Figure 11 and Figure 12
BIT ERROR RATE	BER					
			$<1 \times 10^{-10}$			Post-Viterbi errors, 13 dB tilt, TCP = 75 dBmV
			$<1 \times 10^{-10}$			Post-Viterbi errors, 18 dB tilt, TCP = 74 dBmV

[1] The noise power ratio gives an equivalent result to the standard modulation error rate (MER) testing but with improved dynamic range using an industry-accepted method.

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	
DC Supply over Voltage (5 minutes)	30 V
RF Input Power (RF_{INPUT}), Single Tone	75 dBmV
Temperature	
Operating Range, T_{PADDLE}	−30°C to +100°C
Peak Reflow (Moisture Sensitivity Level (MSL) 3)	260°C
Junction (T_J) to Maintain 1 Million Hour Mean Time to Failure (MTTF)	170°C
Storage (T_S) Range	−40°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the thermal resistance from the operating portion of the active device to the exposed paddle on the bottom of the case. See the Thermal Considerations section for additional information.

Table 5. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CE-9-4	3.2°C/W	°C/W

[1] *θ_{JC} is defined as between the external T_{PADDLE} and the internal T_J.*

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADCA3280

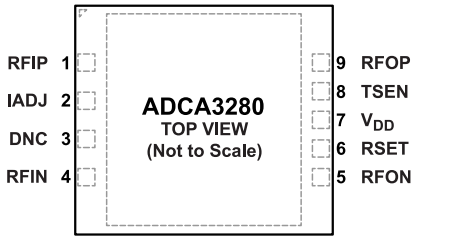
Table 6. ADCA3280, 9-Terminal LGA_CAV

ESD Model	Withstand Threshold	Class
HBM	250 V	1A, passed

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DO NOT CONNECT. THIS PIN IS RESERVED AND MUST BE LEFT FLOATING.
2. EXPOSED PAD. SOLDER THE EXPOSED PADDLE ON THE BOTTOM OF THE PACKAGE TO A LOW IMPEDANCE ELECTRICAL AND THERMAL GROUND PLANE.

002

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	RFIP, RFIN	RF Differential Inputs.
2	IADJ	Bias Adjust. See the Supply Voltage and Current section for information about adjusting the I_{DD} bias current.
3	DNC	Do Not Connect. This pin is reserved and must be left floating.
5, 9	RFON, RFOP	RF Differential Outputs.
6	RSET	The RSET pin is currently reserved for future feature enhancement.
7	V_{DD}	Positive Supply Voltage, 21 V Typical.
8	TSEN	Temperature Sensing Pin.
	EPAD	Exposed Pad. Solder the exposed paddle on the bottom of the package to a low impedance electrical and thermal ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

S-PARAMETERS

Using the downstream schematic and bill of materials (BOM) per the Recommended Applications Circuit and BOM section. V_{DD} = 21 V, I_{DD} = 540 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

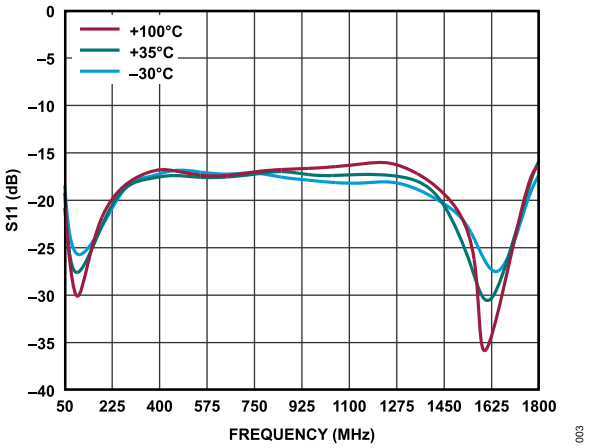


Figure 3. S11 vs. Frequency Over Temperature

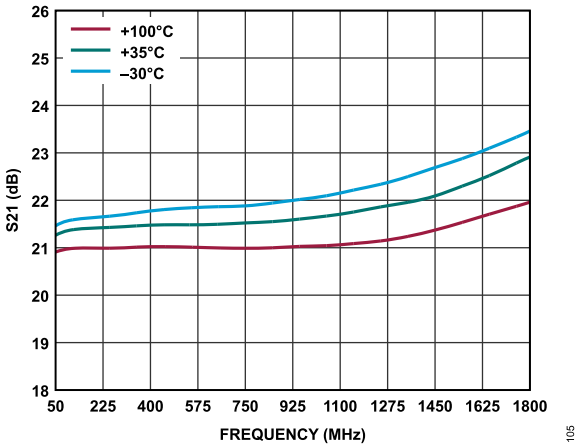


Figure 5. S21 vs. Frequency Over Temperature

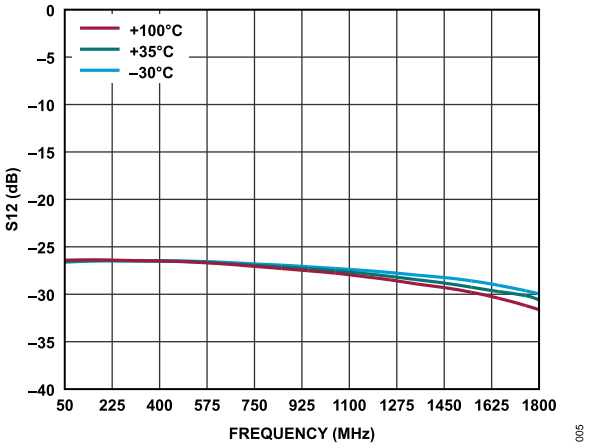


Figure 4. S12 vs. Frequency Over Temperature

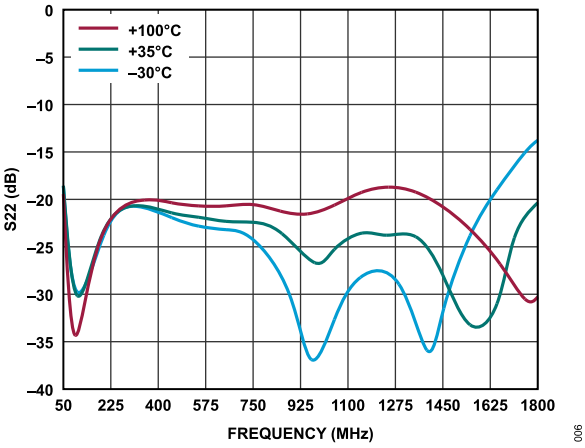


Figure 6. S22 vs. Frequency Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 4.0 DOWNSTREAM PERFORMANCE

8× OFDM channels, 20 dB virtual tilt from 258 MHz to 1794 MHz, and 6 dB offset at 1026 MHz. In Figure 7 to Figure 10, the performance at lower output powers is limited by the test equipment and is not indicative of the noise performance of the device. Results are not corrected for system contributions. Using the downstream schematic and bill of materials (BOM) per the Recommended Applications Circuit and BOM section. V_{DD} = 21 V, I_{DD} = 540 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

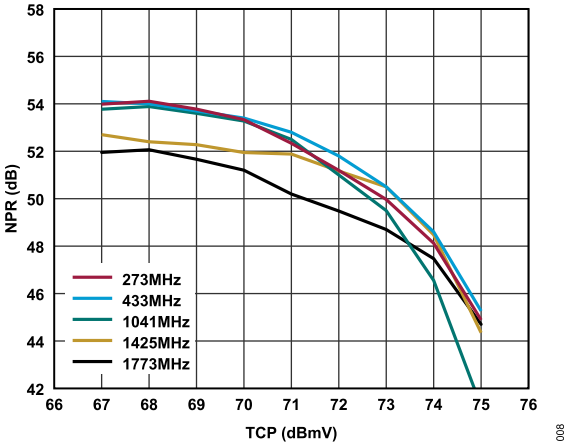


Figure 7. NPR vs. TCP over Frequency, 20 dB Tilt

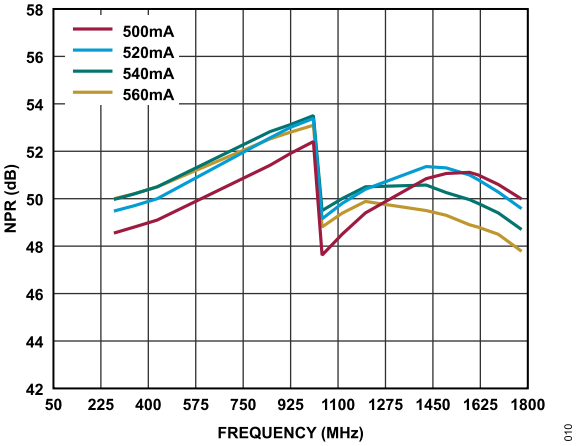


Figure 9. NPR vs. Frequency over Current, 73 dBmV TCP, 20 dB Tilt

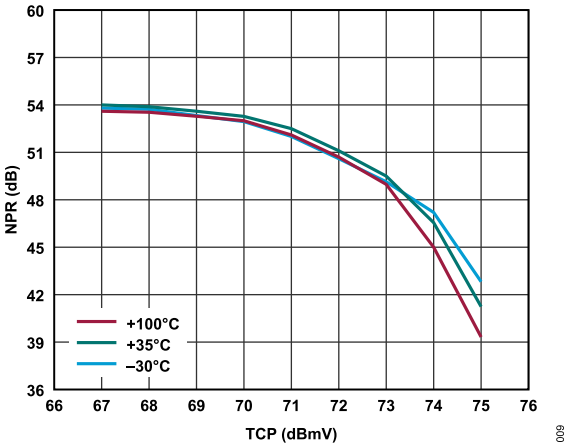


Figure 8. NPR vs. TCP over Temperature, 1041 MHz, 20 dB Tilt

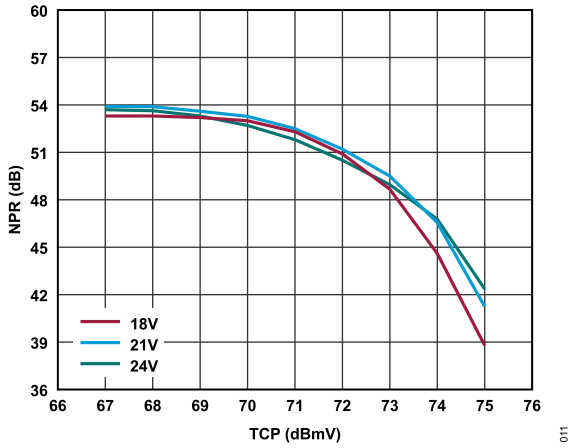


Figure 10. NPR vs. TCP over Voltage, 1041 MHz, 20 dB Tilt

TYPICAL PERFORMANCE CHARACTERISTICS

DOCSIS 3.1 DOWNSTREAM PERFORMANCE

185× ITU-T J.83B, SCQAM 6 MHz channels from 108 MHz to 1218 MHz. In Figure 11 to Figure 20, the performance at lower output powers is limited by the test equipment and is not indicative of the noise performance of the device. Data is presented with both 13 dB and 18 dB tilt from lowest to highest channels. Results are not corrected for system contributions. Using the downstream schematic and bill of materials (BOM) per the Recommended Applications Circuit and BOM section. V_{DD} = 21 V, I_{DD} = 540 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

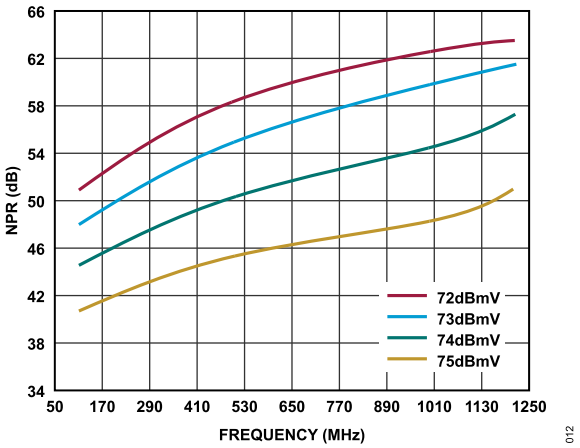


Figure 11. NPR vs. Frequency over TCP, 18 dB Tilt

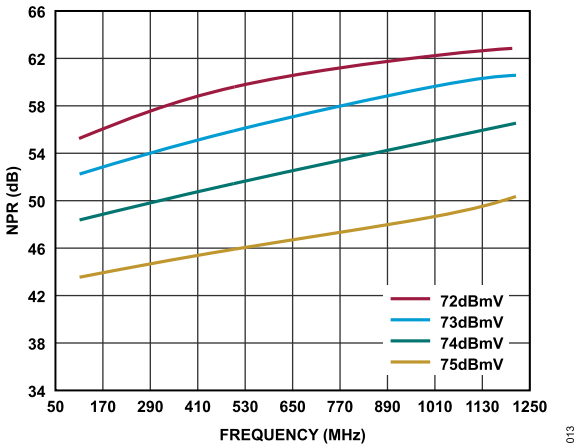


Figure 13. NPR vs. Frequency over TCP, 13 dB Tilt

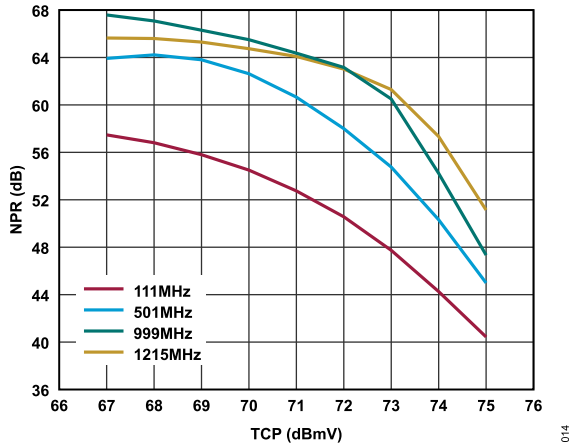


Figure 12. NPR vs. TCP over Frequency, 18 dB Tilt

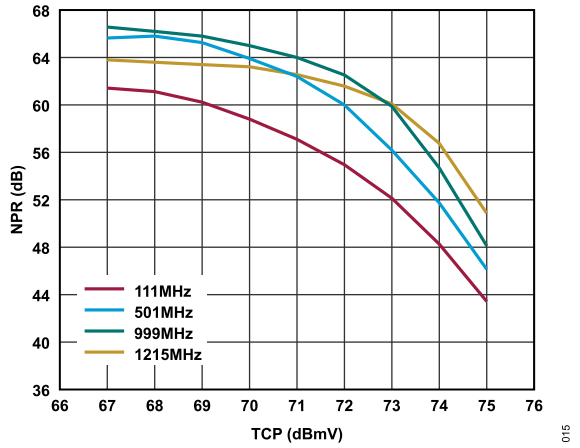


Figure 14. NPR vs. TCP over Frequency, 13 dB Tilt

TYPICAL PERFORMANCE CHARACTERISTICS

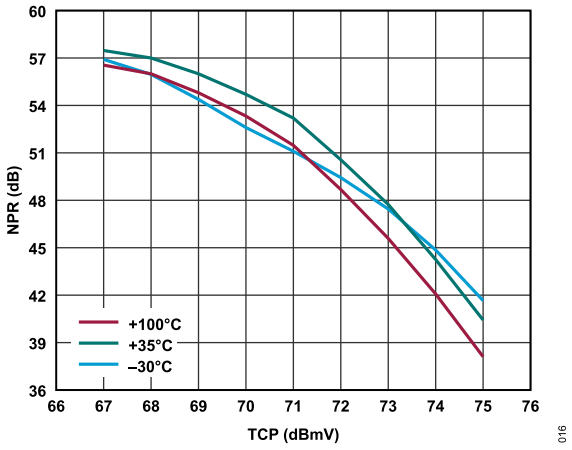


Figure 15. NPR vs. TCP over Temperature, 111 MHz, 18 dB Tilt

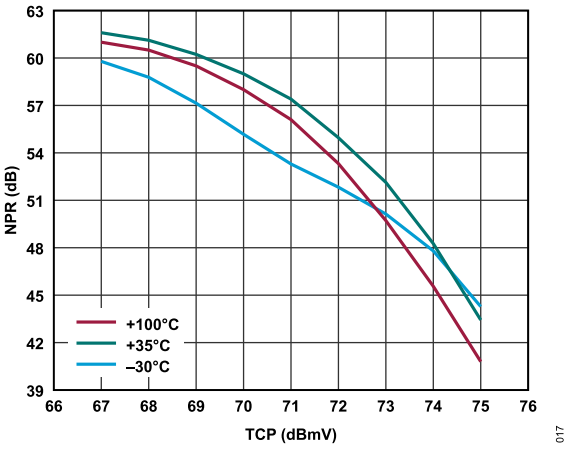


Figure 18. NPR vs. TCP over Temperature, 111 MHz, 13 dB Tilt

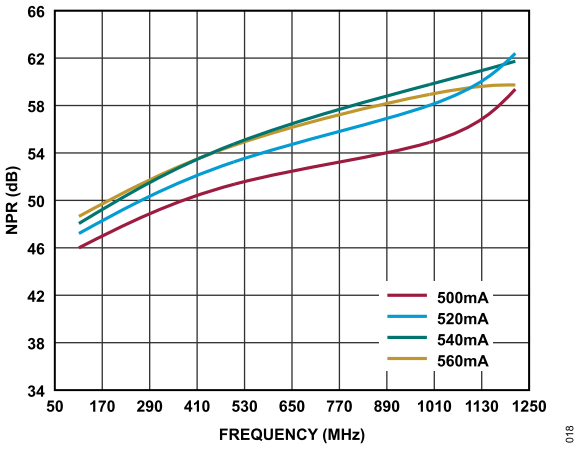


Figure 16. NPR vs. Frequency over Current, 73 dBmV TCP, 18 dB Tilt

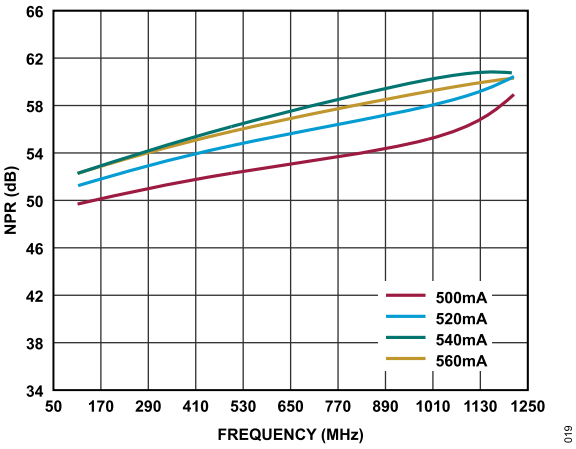


Figure 19. NPR vs. Frequency over Current, 73 dBmV TCP, 13 dB Tilt

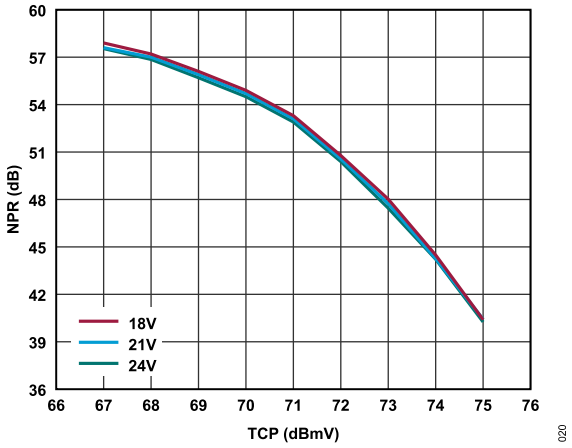


Figure 17. NPR vs. TCP over Voltage, 111 MHz, 18 dB Tilt

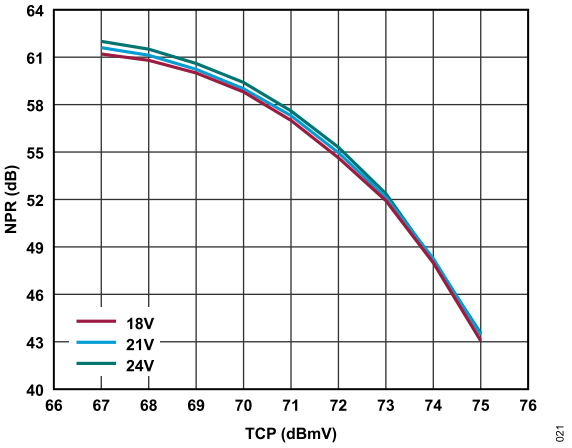


Figure 20. NPR vs. TCP over Voltage, 111 MHz, 13 dB Tilt

TYPICAL PERFORMANCE CHARACTERISTICS

NOISE PERFORMANCE

Noise figure measured using the schematic and layout shown in Figure 24. Reported values include the losses of the balun, PCB traces, and other components in the input circuit. V_{DD} = 21 V, I_{DD} = 540 mA, T_{PADDLE} = 35°C, and Z_S = Z_L = 75 Ω, unless otherwise noted.

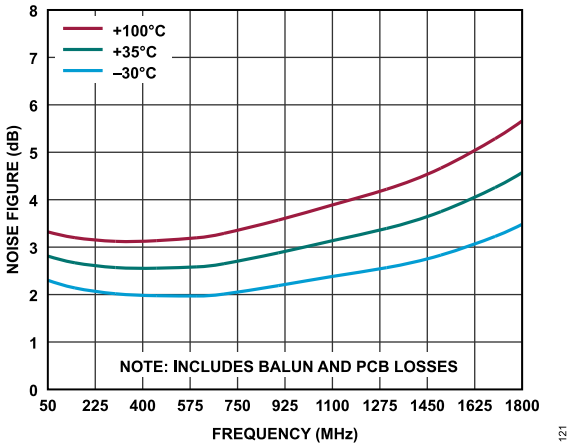


Figure 21. Noise Figure vs. Frequency over Temperature

THEORY OF OPERATION

The ADCA3280 is a balanced amplifier packaged in a 9-terminal LGA_CAV package. The application circuit interfaces the ADCA3280 to a 75 Ω input and output matched impedance consistent with a matched module designed for community access television (CATV) applications. The ADCA3280 uses cascode field effect transistor (FET) feedback amplifiers in a Class A push-pull configuration. The bottom half of the cascode stages are implemented in a single die, linear gallium arsenide (GaAs), FET process that minimizes parasitics, enabling higher gain. The top devices in the cascodes are implemented using a linear gallium nitride (GaN) process that is able to swing high RF voltages. The frequency of operation is from 45 MHz to 1794 MHz. Application circuits that use the 45 MHz to 108 MHz frequency range can be developed as required.

Depending on the application, the ADCA3280 can be biased from 18 V through 24 V with a range of bias currents. The ADCA3280 is unconditionally stable in the recommended application circuit for robust operation in systems targeting DOCSIS 4.0 and legacy DOCSIS standards.

APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

The ADCA3280 is packaged in an industry-standard 9-terminal, 9 mm x 8 mm LGA_CAV package. The thermal resistance from θ_{JC} is 3.2°C/W at 24 V, where the case is defined by the exposed pad on the bottom of the package. For the best thermal performance, it is recommended to add as many thermal vias as possible under the exposed pad of the LGA_CAV. Thermal transfer is maximized when the amount of copper under the exposed pad is maximized. A solid copper slug captured in the PCB can also be used in place of vias to provide additional thermal benefits; however, this slug is not required for typical operation. The array of vias under the ADCA3280 must interface to an external heat sink such as a pedestal on the system chassis.

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 22 shows the recommended land pattern for the ADCA3280. To minimize thermal impedance, the exposed pad on the 9 mm × 8 mm LGA_CAV is soldered to a ground plane. To improve thermal dissipation, 188 thermal vias are arranged in an array under the exposed pad. The array consists of alternating rows of 13 vias and 12 vias, maximizing the number of vias within the area. The area under the exposed pad is also tied to ground on the bottom layer of the PCB. If multiple ground layers exist, tie these layers together by the vias. The external layer of the PCB must be a minimum of 1 oz. copper. The minimum average plated hole wall thickness of the vias must not be less than 0.001 inches. Additional copper and vias extending beyond the top and bottom of the ADCA3280 package can provide a small additional thermal benefit.

Figure 23 shows the recommended solder dispense pattern for the ADCA3280. The pads are fully covered with solder, while the thermal pad has 40% coverage broken into squares to minimize solder voiding.

For further information on optimizing the thermal performance while using the ADCA3280, refer to the AN-1604 Application Note, *Thermal Management Calculations for RF Amplifiers in LFCSP and Flange Packages*.

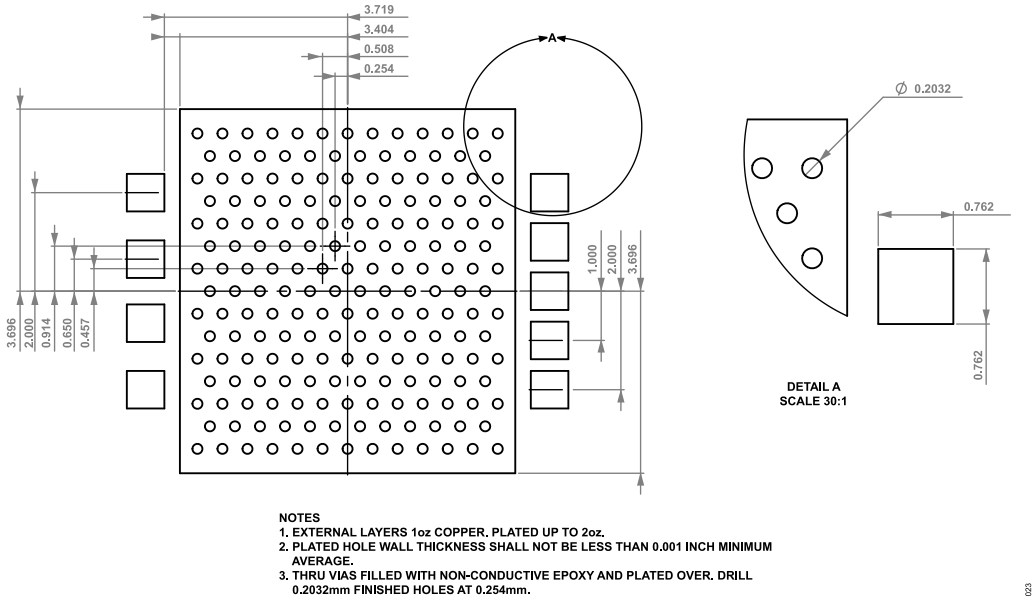


Figure 22. Recommended PCB Layout (Dimensions Shown in Millimeters)

APPLICATIONS INFORMATION

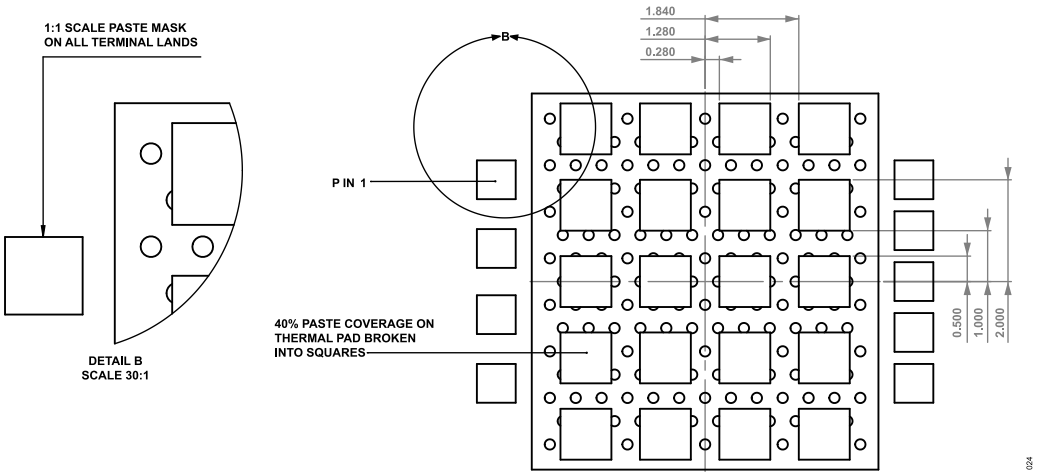


Figure 23. Recommended Solder Pattern (Dimensions Shown in Millimeters)

APPLICATIONS INFORMATION

RECOMMENDED APPLICATIONS CIRCUIT AND BOM

The schematic in Figure 24 is recommended for downstream cable system applications from 108 MHz to 1794 MHz, for both DOCSIS 3.1 and DOCSIS 4.0. Recommended values for all components are in the BOM listed in Table 8. T1 and T2 are RF transformers configured to transform the single-ended 75 Ω RF input and output to differential signals that drive the 37.5 Ω inputs and outputs of the ADCA3280 (RFIN, RFIP, RFON, and RFOP).

The C1, C2, C4, C7, C8, C9, C10, C14, C15, C16, C17, and R1 components are intended for impedance matching, and these components must be optimized to match the RF input source and RF output load. Capacitors C1, C9, and C10 also serve as DC blocks for the RF input and output pins. Inductors L2 and L3 are RF chokes connected to the filtered V_{DD} supply voltage. Components C11, C12, C13, C18, C19, C20, C21, C22, C23, L1, E2, and E3 are present to filter the DC supply lines. If these lines are otherwise filtered in the application, then some or all of these components may not be necessary.

The network connected to the IADJ pin (Pin 2) sets up a voltage to control the bias current of the amplifier. The RT1 component trims the adjustment voltage as a function of temperature and provides more stable bias current over temperature. Expect bias current to vary ±15 mA over temperature extremes from a nominal set point. If bias adjustment is not required for the application, R5, C19, and the IADJ net can be removed, and the ADCA3280 is passively set to a nominal current by R3 and RT1. Adjustment of the bias current via IADJ is discussed in detail in the Supply Voltage and Current section.

When laying out a circuit for the ADCA3280, it is recommended to follow the layout for the evaluation board shown in the EVAL-ADCA3280 User Guide. Particularly important are the relative distances between the ADCA3280 and T1, T2, as well as the tuning components in between those components (C4, C7, C8, and C14).

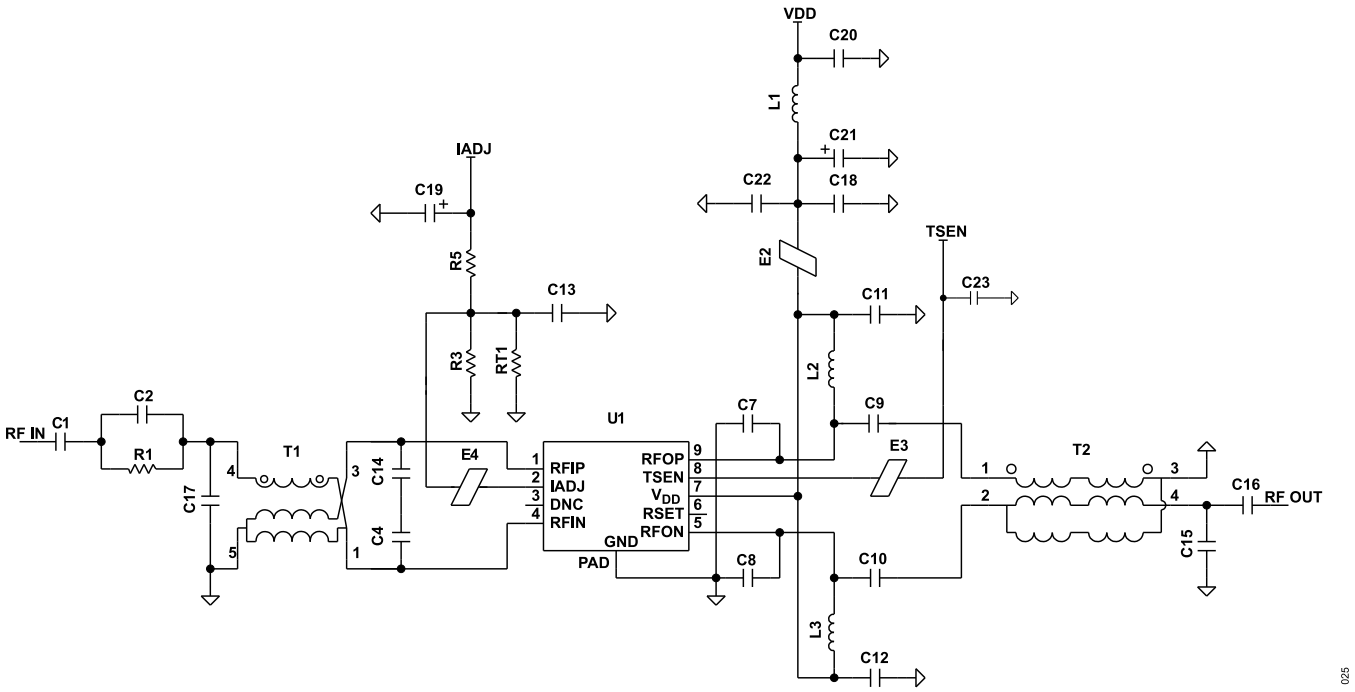


Figure 24. Recommended Application Circuit Schematic

APPLICATIONS INFORMATION

Table 8. Recommended Application Circuit BOM[1]

Reference Designator	Value	Tolerance	Minimum Rating	Footprint	Suggested Manufacturer	Suggested Part Number
C1, C11, C12, C16, C22, C23	0.01 µF	±10%	50 V	0402	Samsung	CL05B103KB5NNNC
C2	82 pF	±5%	50 V	0402	Yageo	CC0402JRNPO9BN820
C4, C14	2.6 pF	±0.05 pF	25 V	0201	Murata	GJM0335C1E2R6WB01D
C7, C8	0.5 pF	±0.01 pF	100 V	0201	AVX Corporation	02011J0R5ZBSTR
C9, C10	150 pF	±5%	50 V	0201	Murata	GRM0335C1H151JA01D
C13	1000 pF	±10%	100 V	0402	Murata	GRM0335C2AR30BA01D
C17	0.3 pF	±20%	100 V	0201	Murata	GRM155R72A102KA01D
C19, C21	2.2 µF	±10%	50 V	1210	AVX Corporation	TAJB225K050RNJ
C20	0.01 uF	±10%	100 V	0603	TDK	C1608X7R2A103K080AA
E3	1.8 kΩ at 100 MHz	±25%	N/A	0201	Murata	BLM03HD182FN1D
E2	220 Ω at 100 MHz	±25%	N/A	0603	Taiyo Yuden	FBMH1608HM221-T
E4	220 Ω at 100 MHz	±25%	N/A	0402	Murata	BLM15GG221SN1D
L1	2.2 µH	±20%	N/A	1210	Taiyo Yuden	BRL3225T2R2M
L2, L3	420 nH	±5%	N/A	0402	Coilcraft	0402DF-421XJR
R1	7.15 Ω	±1%	N/A	0402	Vishay	CRCW04027R15FKED
R3	3000 Ω	±1%	N/A	0402	Panasonic	ERJ-2RKF3001X
R5	200 Ω	±1%	N/A	0402	Panasonic	ERJ-2RKF2000X
RT1	100 kΩ negative temperature coefficient (NTC)	±1%	240 mW	0402	Mitsubishi	TH05-4B104FR
T1	1:1 transformer	N/A	N/A	S20	MiniRF	MRFXF0835
T2	1:1 transformer	N/A	N/A	TT1618-2	Mini-Circuits	TRS1-182-75-3+
U1	CATV amplifier	N/A	N/A	9 mm x 8 mm, 9-terminal LGA_CAV	Analog Devices, Inc.	ADCA3280
C15, C18	Do not install (DNI)	N/A	N/A	N/A	N/A	N/A

[1] N/A means not applicable.

APPLICATIONS INFORMATION

SUPPLY VOLTAGE AND CURRENT

The ADCA3280 can operate over a range of supply voltage and current, allowing for optimization of performance for a given DC power target, or to operate on a range of established power supply voltage rails.

Supply voltage variation is a straightforward way to alter the device power consumption, and performance, as a function of the bias voltage, can be seen for both DOCSIS 3.1 and DOCSIS 4.0 loading in the DOCSIS 3.1 Downstream Performance section and the DOCSIS 4.0 Downstream Performance section, respectively. While the ADCA3280 is designed with 24 V supply rails in mind, significant efficiency gains are possible with a lower supply voltage. The majority of the data presented in this data sheet demonstrates operation at 21 V with little or no loss of performance compared with 24 V. For some applications, such as those with 1.2 GHz channel loading, as seen in the DOCSIS 3.1 Downstream Performance section, there is no significant change in performance with bias as low as 18 V.

The ADCA3280 also offers adjustable supply current. The IADJ pin (Pin 2) allows the user to adjust the bias current of the device. If left floating, the current self sets to more than the nominal operating current by 20 mA to 40 mA. The voltage at the IADJ pin can be directly set with a supply capable of sinking current, set by using a supply and an external resistor network, or set with a resistor directly to ground. An internal voltage reference die is used to keep the bias current well centered as a function of process and temperature variation. Generally, to increase I_{DD} more than a nominal set point, a supply must source current into the IADJ network. To decrease I_{DD}, the supply must sink current from the IADJ network. The typical device current as a function of the voltage at the IADJ pin can be seen in Figure 25. The typical device current as a function of voltage at the IADJ node in the recommended application circuit can be seen in Figure 26.

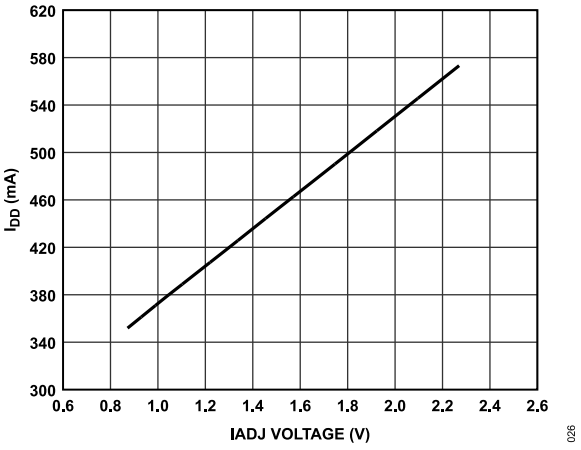


Figure 25. I_{DD} vs. IADJ Voltage over V_{DD}

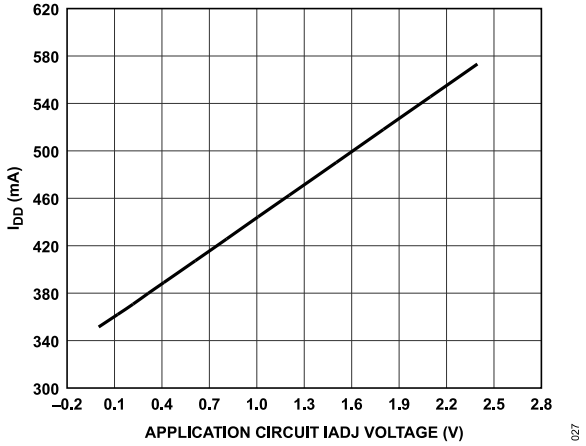


Figure 26. I_{DD} vs. Application Circuit IADJ Voltage over V_{DD}

INTERNAL THERMAL MONITOR

The ADCA3280 has an internally mounted 10 kΩ NTC resistor that can be used to monitor the temperature of the backside paddle of the device. The NTC can be monitored directly through the TSEN pin (Pin 8) with an ohmmeter, or by applying a small constant voltage (such as 0.1 V) or current (such as 0.01 mA) and calculating the resulting resistance. Take care to minimize power dissipation in the NTC because inaccuracies due to self heating or damage can occur. Ideally, power dissipated in the thermistor must be less than 1 mW and not exceed 5 mW at any operating temperature. Figure 27 shows the relationship of the thermistor resistance measurement to the paddle temperature of the ADCA3280.

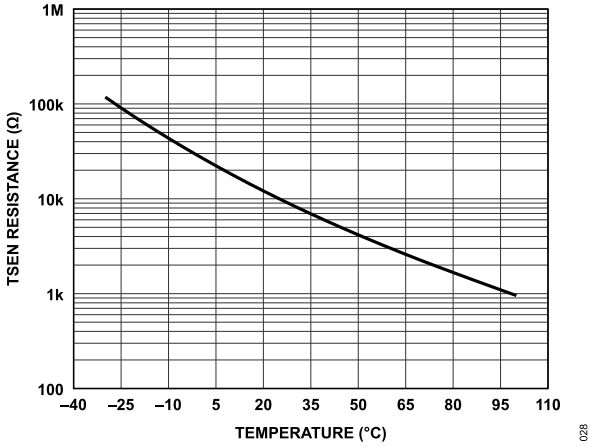


Figure 27. TSEN Resistance vs. Temperature

OUTLINE DIMENSIONS

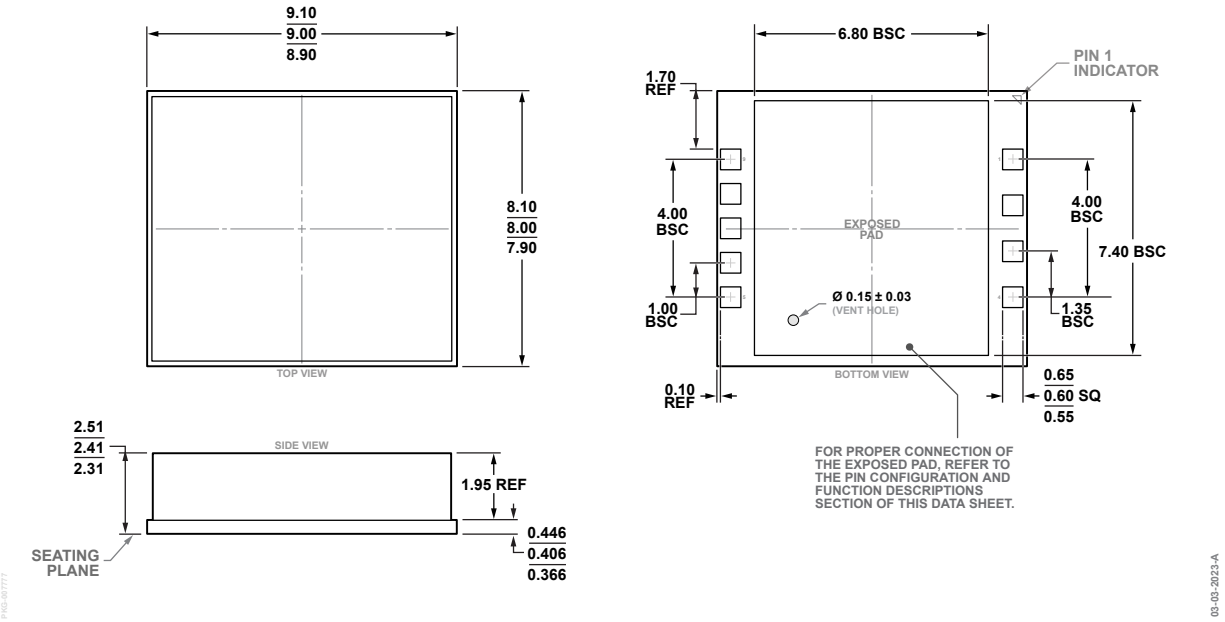


Figure 28. 9-Terminal Chip Array Small Outline, No Lead Cavity [LGA_CAV]
9.00 mm × 8.00 mm Body and 2.41 mm Package Height
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADCA3280ACEZ	−30°C to +100°C	9-Terminal Chip Array Small Outline, No Lead Cavity [LGA_CAV]		CE-9-4
ADCA3280ACEZ-R7	−30°C to +100°C	9-Terminal Chip Array Small Outline, No Lead Cavity [LGA_CAV]	Reel, 400	CE-9-4

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADCA3280-EVALZ	Evaluation Board for the Downstream Cable System Application

[1] Z = RoHS Compliant Part.