Data Sheet

ADA4661-2-KGD

Known Good Die

18 V, Precision, 725 µA, 4 MHz, CMOS RRIO Operational Amplifier

FEATURES

- Low power at high voltage (18 V): 725 µA maximum
- Low offset voltage
  - 150 µV maximum at $V_{SY}/2$
  - 300 µV maximum over entire common-mode range
- Low input bias current: 15 pA maximum
- Gain bandwidth product: 4 MHz typical at A_V = 100
- Unity-gain crossover: 4 MHz typical
- −3 dB closed-loop gain: 2.1 MHz typical
- Single-supply operation: 3 V to 18 V
- Dual-supply operation: ±1.5 V to ±9 V
- Unity-gain stable

APPLICATIONS

- Current shunt monitors
- Active filters
- Portable medical equipment
- Buffer/level shifting
- High impedance sensor interfaces
- Battery-powered instrumentation

GENERAL DESCRIPTION

The ADA4661-2-KGD is a dual, precision, rail-to-rail input/output amplifier optimized for low power, high bandwidth, and wide operating supply voltage range applications.

The ADA4661-2-KGD performance is guaranteed at 3.0 V, 10 V, and 18 V power supply voltages. It uses the Analog Devices, Inc., patented DigiTrim® trimming technique, which achieves low offset voltage. Additionally, the unique design architecture of the ADA4661-2-KGD allows it to have excellent power supply rejection, common-mode rejection, and offset voltage when operating in the common-mode voltage range of $-V_{SY}$ + 1.5 V to $+V_{SY}$ − 1.5 V.

The ADA4661-2-KGD is specified over the extended industrial temperature range (−40°C to +125°C). Additional application and technical information can be found in the ADA4661-2 data sheet.

Known Good Die (KGD): these die are guaranteed to data sheet specifications.

FUNCTIONAL BLOCK DIAGRAM

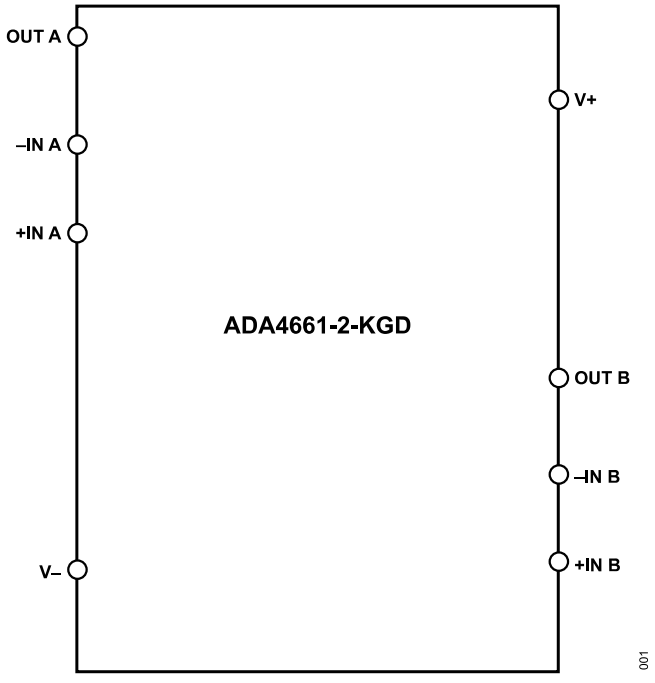

Figure 1.

Rev. 0

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

TABLE OF CONTENTS

REVISION HISTORY

12/2021—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS–18 V

V_{SY} = 18 V, V_{CM} = V_{SY}/2 V, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			30	150	µV
		V_{CM} = 1.5 V to 16.5 V			150	µV
		V_{CM} = 1.5 V to 16.5 V, −40°C ≤ T_A ≤ +125°C			500	µV
		V_{CM} = 0 V to 18 V			300	µV
		V_{CM} = 0 V to 18 V, −40°C ≤ T_A ≤ +125°C			600	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.6	3.1	µV/°C
Input Bias Current	I_B			0.5	15	pA
		−40°C ≤ T_A ≤ +85°C			100	pA
		−40°C ≤ T_A ≤ +125°C			900	pA
Input Offset Current	I_{OS}				11	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
		−40°C ≤ T_A ≤ +125°C			300	pA
Input Voltage Range			0		18	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.5 V to 16.5 V	115	135		dB
		V_{CM} = 1.5 V to 16.5 V, −40°C ≤ T_A ≤ +125°C	110			dB
		V_{CM} = 0 V to 18 V	100	118		dB
		V_{CM} = 0 V to 18 V, −40°C ≤ T_A ≤ +125°C	91			dB
Large Signal Voltage Gain	A_{VO}	Load resistance (R_L) = 100 kΩ, output voltage (V_{OUT}) = 0.5 V to 17.5 V	120	147		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Input Resistance						
Differential Mode	R_{INDM}			>10		GΩ
Common Mode	R_{INCM}			>10		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			8.5		pF
Common Mode	C_{INCM}			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	R_L = 10 kΩ to V_{CM}		17.97		V
		R_L = 1 kΩ to V_{CM}		17.97		V
Low	V_{OL}	R_L = 10 kΩ to V_{CM}		14		mV
		R_L = 1 kΩ to V_{CM}		120		mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		40		mA
Short-Circuit Current	I_{SC}	Pulse width = 10 ms		±220		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, voltage gain (A_V) = 1		0.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current per Amplifier	I_{SY}	Output current (I_{OUT}) = 0 mA		630	725	µA
		−40°C ≤ T_A ≤ +125°C			975	µA

SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	Source resistance (R_S) = 1 kΩ, R_L = 10 kΩ, load capacitance (C_L) = 10 pF, A_V = 1		2		V/µs
Gain Bandwidth Product	GBP	Input voltage (V_{IN}) = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		4		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		2.1		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		60		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		1.3		µs
Channel Separation	CS	V_{IN} = 17.9 V p-p, f = 10 kHz, R_L = 10 kΩ		80		dB
Electromagnetic Interference (EMI) Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV peak (200 mV p-p)				
f = 400 MHz				34		dB
f = 900 MHz				42		dB
f = 1800 MHz				50		dB
f = 2400 MHz				60		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	A_V = 1, V_{IN} = 5.4 V rms at 1 kHz				
Bandwidth = 80 kHz				0.0004		%
Bandwidth = 500 kHz				0.0008		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		360		fA/√Hz

ELECTRICAL CHARACTERISTICS–10 V

Power supply voltage (V_{SY}) = 10 V, common-mode voltage (V_{CM}) = V_{SY}/2 V, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			30	150	µV
		V_{CM} = 1.5 V to 8.5 V			150	µV
		V_{CM} = 1.5 V to 8.5 V, −40°C ≤ T_A ≤ +125°C			450	µV
		V_{CM} = 0 V to 10 V			300	µV
		V_{CM} = 0 V to 10 V, −40°C ≤ T_A ≤ +125°C			600	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.6	3.1	µV/°C
Input Bias Current	I_B			0.25	15	pA
		−40°C ≤ T_A ≤ +85°C			80	pA
		−40°C ≤ T_A ≤ +125°C			750	pA
Input Offset Current	I_{OS}				11	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
		−40°C ≤ T_A ≤ +125°C			270	pA
Input Voltage Range			0		10	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.5 V to 8.5 V	115	140		dB
		V_{CM} = 1.5 V to 8.5 V, −40°C ≤ T_A ≤ +125°C	115			dB
		V_{CM} = 0 V to 10 V	95	114		dB
		V_{CM} = 0 V to 10 V, −40°C ≤ T_A ≤ +125°C	86			dB

SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Large Signal Voltage Gain	A_{VO}	Load resistance (R_L) = 100 kΩ, output voltage (V_{OUT}) = 0.5 V to 9.5 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Input Resistance						
Differential Mode	R_{INDM}			>10		GΩ
Common Mode	R_{INCM}			>10		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			8.5		pF
Common Mode	C_{INCM}			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	R_L = 10 kΩ to V_{CM}		9.98		V
		R_L = 1 kΩ to V_{CM}		9.88		
Low	V_{OL}	R_L = 10 kΩ to V_{CM}		10		mV
		R_L = 1 kΩ to V_{CM}		77		
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		40		mA
Short-Circuit Current	I_{SC}	Pulse width = 10 ms		±220		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, voltage gain (A_V) = 1		0.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current per Amplifier	I_{SY}	Output current (I_{OUT}) = 0 mA		620	725	µA
		−40°C ≤ T_A ≤ +125°C			975	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	Source resistance (R_S) = 1 kΩ, R_L = 10 kΩ, load capacitance (C_L) = 10 pF, A_V = 1		1.8		V/µs
Gain Bandwidth Product	GBP	Input voltage (V_{IN}) = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		4		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		2.1		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		60		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		1.3		µs
Channel Separation	CS	V_{IN} = 9.9 V p-p, f = 10 kHz, R_L = 10 kΩ		85		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV peak (200 mV p-p)				
f = 400 MHz				34		dB
f = 900 MHz				42		dB
f = 1800 MHz				50		dB
f = 2400 MHz				60		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	A_V = 1, V_{IN} = 2.2 V rms at 1 kHz				
Bandwidth = 80 kHz				0.0004		%
Bandwidth = 500 kHz				0.0008		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		360		fA/√Hz

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS–3 V

V_{SY} = 3 V, V_{CM} = V_{SY}/2 V, and T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			30	150	µV
		V_{CM} = V_{SY}/2, −40°C ≤ T_A ≤ +125°C			450	µV
		V_{CM} = 0 V to 3.0 V			300	µV
		V_{CM} = 0 V to 3.0 V, −40°C ≤ T_A ≤ +125°C			600	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.6	3.1	µV/°C
Input Bias Current	I_B			0.15	8	pA
		−40°C ≤ T_A ≤ +85°C			45	pA
		−40°C ≤ T_A ≤ +125°C			650	pA
Input Offset Current	I_{OS}				11	pA
		−40°C ≤ T_A ≤ +85°C			30	pA
		−40°C ≤ T_A ≤ +125°C			270	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3.0 V	85	100		dB
		V_{CM} = 0 V to 3.0 V, −40°C ≤ T_A ≤ +125°C	75			dB
Large Signal Voltage Gain	A_{VO}	Load resistance (R_L) = 100 kΩ, output voltage (V_{OUT}) = 0.5 V to 2.5 V	105	130		dB
		−40°C ≤ T_A ≤ +125°C	105			dB
Input Resistance						
Differential Mode	R_{INDM}			>10		GΩ
Common Mode	R_{INCM}			>10		GΩ
Input Capacitance						
Differential Mode	C_{INDM}			8.5		pF
Common Mode	C_{INCM}			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage						
High	V_{OH}	R_L = 10 kΩ to V_{CM}		2.99		V
		R_L = 1 kΩ to V_{CM}		2.96		V
Low	V_{OL}	R_L = 10 kΩ to V_{CM}		4		mV
		R_L = 1 kΩ to V_{CM}		25		mV
Continuous Output Current	I_{OUT}	Dropout voltage = 1 V		30		mA
Short-Circuit Current	I_{SC}	Pulse width = 10 ms		±220		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, voltage gain (A_V) = 1		0.2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 3.0 V to 18 V	120	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current per Amplifier	I_{SY}	Output current (I_{OUT}) = 0 mA		615	725	µA
		−40°C ≤ T_A ≤ +125°C			975	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	Source resistance (R_S) = 1 kΩ, R_L = 10 kΩ, load capacitance (C_L) = 10 pF, A_V = 1		1.7		V/µs
Gain Bandwidth Product	GBP	Input voltage (V_{IN}) = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		4		MHz

SPECIFICATIONS

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		4		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		1.7		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		60		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF		1.3		µs
Channel Separation	CS	V_{IN} = 2.9 V p-p, f = 10 kHz, R_L = 10 kΩ		90		dB
EMI Rejection Ratio of +IN x	EMIRR	V_{IN} = 100 mV peak (200 mV p-p)				
f = 400 MHz				34		dB
f = 900 MHz				42		dB
f = 1800 MHz				50		dB
f = 2400 MHz				60		dB
NOISE PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD + N	A_V = 1, V_{IN} = 0.44 V rms at 1 kHz				
Bandwidth = 80 kHz				0.002		%
Bandwidth = 500 kHz				0.003		%
Peak-to-Peak Noise	e_n p-p	f = 0.1 Hz to 10 Hz		3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		18		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		360		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	20.5 V
Input Voltage Range	(V−) − 300 mV to (V+) + 300 mV
Input Current[1]	±10 mA
Differential Input Voltage	Limited by maximum input current
Output Short-Circuit Duration to Ground	See ADA4661-2 data sheet
Temperature Range	
Storage	−65°C to +150°C
Operating	−40°C to +125°C
Junction	−65°C to +150°C

[1] The input pins have clamp diodes connected to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings for ADA4661-2-KGD

Table 4. ADA4661-2-KGD, 8-Pad CHIP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	IV
MM	±400	Not applicable

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

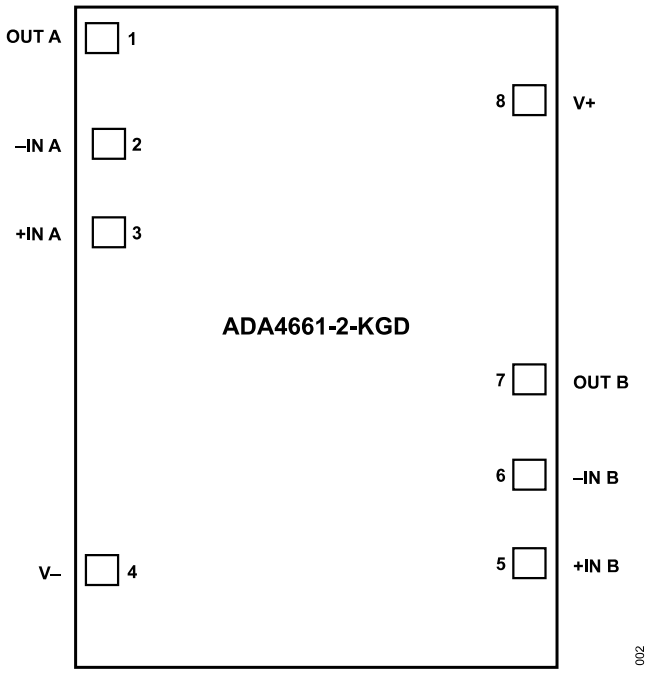

Figure 2. Pad Configuration

Table 5. Pad Configuration Descriptions[1]

Pad No.	Mnemonic	X Coordinate	Y Coordinate	Description
1	OUT A	−566	+792	Output, Channel A
2	−IN A	−553	+512	Inverting Input, Channel A
3	+IN A	−553	+281	Noninverting Input, Channel A
4	V−	−566	−624	Negative Supply Voltage
5	+IN B	+553	−601	Noninverting Input, Channel B
6	−IN B	+553	−370	Inverting Input, Channel B
7	OUT B	+566	−112	Output, Channel B
8	V+	+566	+628	Positive Supply Voltage

[1] All dimensions are referenced from the center of the die to the center of each bond pad.

OUTLINE DIMENSIONS

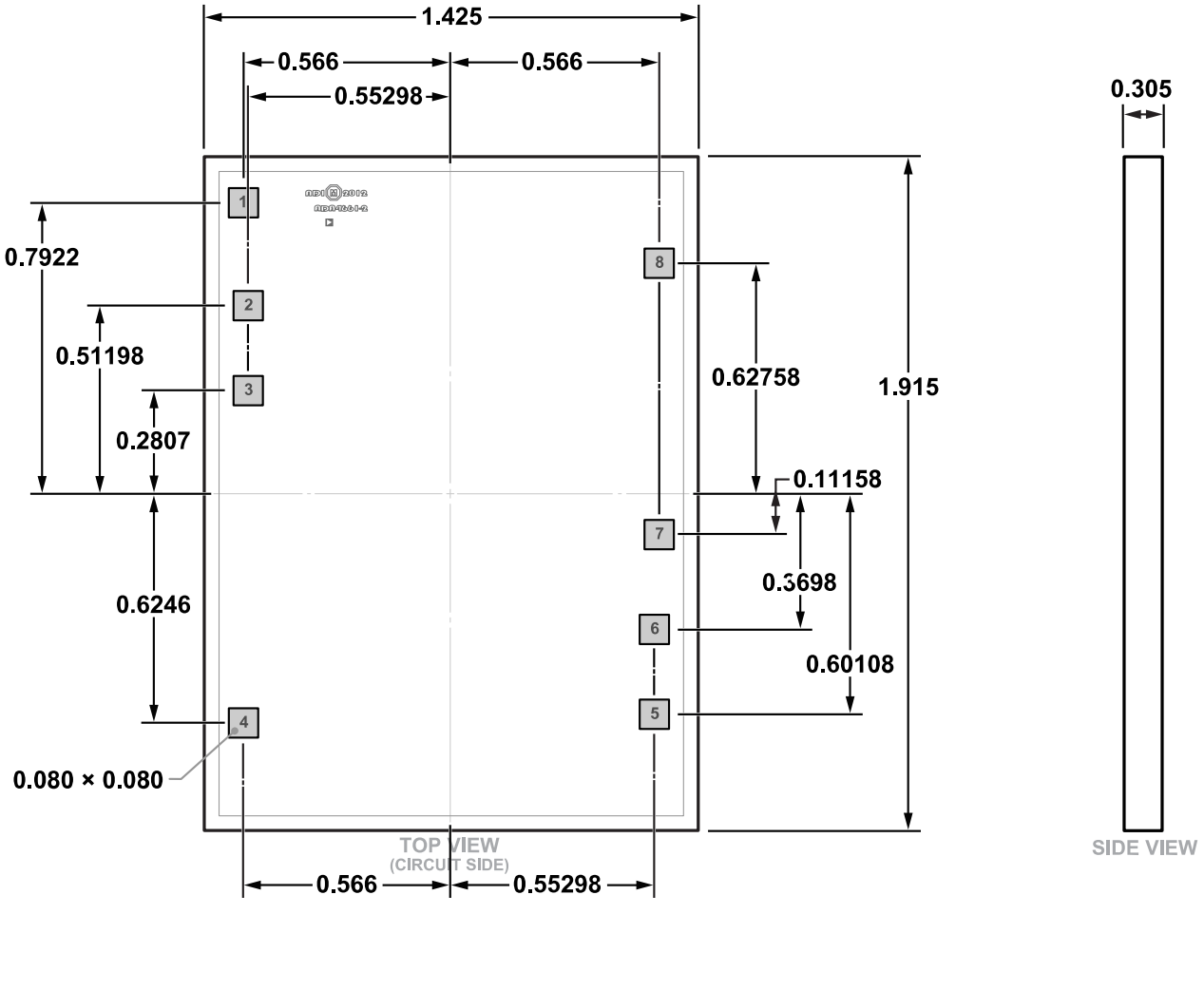

Figure 3. 8-Pad Bare Die [CHIP]
(C-8-25)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Chip Size	1265 × 1755	µm
Scribe Line Width	160	µm
Die Size	1425 × 1915	µm
Thickness	305	µm
Backside	V− or left floating	V
Passivation	10 kA high density plasma oxide + 7 kA nitride	Not applicable
Topcoat Thickness	7, Polyimide	µm
Bond Pads (Minimum)	80 × 80	µm
Bond Pad Composition	Aluminum (Al), 0.5 Copper (Cu)	%

OUTLINE DIMENSIONS

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Hitachi CEL 9240HF10AK
Bonding Method	1 mil gold
Bonding Sequence	Unspecified

Updated: December 15, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
ADA4661-2-KGD-WP	-40°C to +125°C	CHIPS OR DIE	Tray, 320	C-8-25	A33

[1] ADA4661-2-KGD-WP is an RoHS compliant part.