**NuMicro® Family**

**Arm® 32-bit Cortex®-M4 Microcontroller**

# M471M/M471R1/M471S Series Datasheet



For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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# 1 GENERAL DESCRIPTION

The NuMicro® M471M/M471R1/M471S series is a 32-bit microcontroller based on Arm® Cortex®-M4F core, with DSP instruction set and single-precision floating-point unit (FPU), targeted for smart home appliance applications. For the growing requirement of the safety functions on the home appliance, the M471M/M471R1/M471S series provides certified Software Test Library (STL) and an application note for IEC60730-1 Class B Annex H. This certified STL can significantly reduce the development time and efforts to pass IEC60730-1 Class B certification for home appliances. The M471M/M471R1/M471S series runs up to 72 MHz, and features 2.5V to 5.5V wide operating voltage, -40°C to 105°C wide operating temperature, a variety of packages with wide pin pitch, and excellent high immunity characteristics by ESD HBM 8 KV and EFT 4.4 KV, which greatly meet the rigid requirements for stability, reliability and safety of home appliance systems.

As the new smart function added on home appliances, the M471M/M471R1/M471S series provides up to 128 KB Flash memory for code storage, 32 KB SRAM for run time operation. Data Flash could be configured in the 128 KB Flash memory to store parameters. In order to reduce the data access overhead of CPU core to peripherals, a peripheral direct memory access (PDMA) is provided.

The M471M/M471R1/M471S series supports plenty of peripherals including up to 16 channels of 12-bit SAR ADC, up to 12 channels of 16-bit PWM, 1 set of USB 2.0 full speed Device/Host (crystal-less), 4 sets of UART, 1 set of SPI/I²S, 1 set of Quad-SPI, 2 sets of I²C, 1 set of ISO-7816, and a real-time clock (RTC).

For the development, Nuvoton provides the NuMaker-M471R1 evaluation board, and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, Eclippse IDE with GNU GCC compilers are also supported.

| Product Line | Core (MHz) | PDMA | CRC | Timer (32-bit) | PWM | UART | I²C | QSPI/SPI | ADC | ACMP | DAC | CIR | PRNG | USB H/D |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| M471M/M471R1/ M471S Series | 72 | √ | √ | 4 | 12 | 4 | 2 | SPI x1 QSPI x1 | 16 | - | - | - | - | √ |

Table 1-1 NuMicro® M471M/M471R1/M471S Series Key Features Support Table

This series supports three package choices which are designed for home appliance PCB demands.

- LQFP44: 10 mm x 10 mm, pin pitch 0.8 mm
- LQFP64: 7 mm x 7 mm, pin pitch 0.4 mm
- LQFP64: 14 mm x 14 mm, pin pitch 0.8 mm

The NuMicro® M471M/M471R1/M471S series is suitable for a wide range of applications such as:

- Washing Machine
- Refrigerator
- Air conditioner
- PM2.5 detector
- Other home appliances

# 2 FEATURES

## 2.1 M471M/M471R1/M471S Features

- Core
  - Arm® Cortex®-M4F core running up to 72 MHz
  - Supports DSP extension with hardware divider
  - Supports IEEE 754 compliant Floating-point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports Low Power Sleep mode by WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 16 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports programmable mask-able interrupts
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Flash Memory
  - Supports 128/64 KB application ROM (APROM)
  - Supports 4 KB Flash for loader (LDROM)
  - Supports Data Flash with configurable memory size
  - Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded Flash memory
  - Supports 2 KB page erase for all embedded Flash
- SRAM Memory
  - 32 KB embedded SRAM
  - Supports byte-, half-word- and word-access
  - Supports PDMA mode
- PDMA (Peripheral DMA)
  - Supports 8 independent configurable channels for automatic data transfer between memories and peripherals
  - Supports Normal and Scatter-Gather Transfer modes
  - Supports two types of priorities modes: Fixed-priority and Round-robin modes
  - Supports byte-, half-word- and word-access
  - Auto increment of the source and destination address
  - Supports single and burst transfer type
- Clock Control
  - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (variation < 2% at -40˚C ~ +105˚C)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
  - Built-in 4~20 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Built-in 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation
  - Supports one PLL up to 144 MHz for high performance system operation, sourced from HIRC and HXT
  - Supports clock failure detection for high/low speed external crystal oscillator
  - Supports exception (NMI) generated once a clock failure detected
  - Supports clock output
- GPIO
  - Four I/O modes

- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level trigger setting
- Supports high driver and high sink current I/O (up to 20 mA at 5V)
- Supports software selectable slew rate control
- Supports 5V-tolerance function for following pins
  - PA.0 ~ PA.3, PC.0 ~ PC.7, PD.2 ~ PD.3, PD.7, PD.12 ~ PD.15, PE.0, PE.8 ~ PE.13, PF.2, PF.5 ~ PF.7
- Supports up to 49/35 GPIOs for LQFP64/44 respectively

- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
  - Supports event counting function to count the event from external pin
  - Supports input capture function to capture or reset counter value
- Watchdog Timer
  - Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
  - Window set by 6-bit counter with 11-bit prescale
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on time-out
- RTC
  - Supports external power pin $V_{BAT}$
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Supports wake-up function
  - Supports 80 bytes spare registers
  - Programmable spare register erase function
  - Supports 32KHz Oscillator gain control
  - Supports tamper detection function
- PWM
  - Supports up to 12 independent PWM outputs with 16-bit resolution
  - Supports maximum clock frequency up to 144MHz
  - Supports 12-bit clock prescale
  - Supports one-shot or auto-reload counter operation mode
  - Supports up, down or up-down PWM counter type
  - Supports synchronous function
  - Supports dead time with maximum divided 12-bit prescale
  - Supports brake function source from pin, comparator output and system safety events
  - Supports PWM auto recovery function after brake condition removed
  - Supports mask function and tri-state output for each PWM pin
  - Supports PWM events interrupt
  - Supports trigger EADC start conversion
  - Supports up to 12 independent input capture channels with rising/falling capture and

with counter reload option
- Supports capture counter with 16-bit resolution
- Supports capture interrupt
- Supports capture PDMA mode

- UART
  - Supports up to four UARTs – UART0, UART1, UART2 and UART3
  - Supports 16-byte FIFOs with programmable level trigger
  - Supports auto flow control ( CTS and RTS)
  - Supports IrDA (SIR) function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports wake-up function
  - Supports PDMA mode
- Smart Card Interface
  - One set of ISO-7816-3 port
  - Compliant to ISO-7816-3 T=0, T=1
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - A 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports stop clock level and clock stop (clock keep) function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation/deactivation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART function
- Quad SPI
  - Supports one set of SPI Quad controller – SPI0
  - Supports Master or Slave mode operation
  - Supports 2-bit Transfer mode
  - Supports Dual and Quad I/O Transfer mode
  - Configurable bit length of a transfer word from 8 to 32-bit
  - Provides separate 8-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports the byte reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA operation
  - Supports 3-wired, no slave select signal, bi-direction interface
  - Master up to 32 MHz, and Slave up to 16 MHz (when chip works at $V_{DD}$ = 5V)
- SPI
  - Supports one set of SPI controller – SPI1
  - Supports Master or Slave mode operation
  - Configurable bit length of a transfer word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports the byte reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA operation
  - Supports 3-wire, no slave select signal, bi-direction interface
  - Master mode up to 36 MHz and Slave mode up to 18 MHz (when chip works at $V_{DD}$ =

5V)

- I²C
  - Supports up to two sets of I²C devices
  - Supports Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
  - Supports SMBus and PMBus
  - Supports speed up to 1Mbps
  - Supports multi-address Power-down wake-up function
- USB 2.0 Full-Speed Device Controller
  - Supports one set of USB 2.0 FS device
  - Compliant to USB specification version 2.0
  - On-chip USB Transceiver
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Supports 512 Bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
  - Start of Frame (SOF) locked clock pulse generation for crystal-less feature (48MHz internal RC oscillator for USB crystal-less only)
  - On-chip 5V to 3.3V LDO for USB PHY
- USB 2.0 Full-Speed Host Controller
  - Compliant with USB Revision 1.1 Specification
  - Compatible with OHCI (Open Host Controller Interface) Revision 1.0
  - Supports full-speed (12 Mbps) and low-speed (1.5 Mbps) USB devices
  - Supports Control, Bulk, Interrupt, Isochronous transfers
  - Supports an integrated Root Hub
  - Supports port power control and port over current detection
  - Built-in DMA
- EBI
  - Supports two dedicated external chip select pins for each memory block
  - Supports external accessible space up to 1 Mbytes (need 20-bit address width) for each bank. Real addressable space size is dependent on package pin out
  - Supports 8-/16-bit data width
  - Supports byte write in 16-bit data width mode
  - Supports PDMA mode
  - Supports Address/Data multiplexed Mode
  - Supports LCD interface i80 mode
  - Supports Timing parameters individual adjustment for each memory block
- EADC
  - Analog input voltage range: 0~ $V_{REF}$ (Max to $AV_{DD}$)
  - Supports single 12-bit SAR ADC conversion
  - 12-bit resolution and 10-bit accuracy is guaranteed
  - Up to 1MSPS conversion rate at 5.0V

- Up to 16 external single-ended analog input channels
- Up to 8 differential analog input pairs
- Supports single ADC interrupt
- Supports external $V_{REF}$ pin
- Support internal reference voltages from Band-gap and Voltage divider
- An A/D conversion can be triggered by Software enable, External pin, Timer 0~3 overflow pulse trigger and PWM trigger
- Supports 3 internal channels for $V_{BAT}$, band-gap VBG input and Temperature sensor input
- Supports PDMA transfer

- Cyclic Redundancy Calculation Unit
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - Programmable initial value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum.
  - Supports 8-/16-/32-bit of data width
  - Interrupt generated once checksum error occurs
- Voltage Adjustable Interface
  - Supports user Configurable 1.8~5.5V I/O Interface with a dedicated power input ($V_{DDIO}$)
  - Supports UART1, SPI0, SPI1, $I^2C1$ or $I^2C0$ interface
- Supports 96-bit Unique ID (UID)
- Supports 128-bit Unique Customer ID (UCID)
- One built-in temperature sensor with 1℃ resolution
- Brown-out detector
  - With 4 levels: 4.4 V/ 3.7 V/ 2.7 V/ 2.2 V
  - Supports Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Operating Temperature: -40℃~105℃
- Packages
  - LQFP 64-pin (14mm x 14mm)
  - LQFP 64-pin (7mm x 7mm)
  - LQFP 44-pin (10mm x 10mm)

# 3 PARTS INFORMATION

## 3.1 Package Type

| LQFP44 | LQFP64 (14x14mm) | LQFP64 (7x7mm) |
|---|---|---|
| M471MD6AE | M471R1E6AE | M471SE6AE |

## 3.2 M471M/M471R1/M471S Series Naming Rule

| M4 | 71 | R1 | E | 6 | A | E |
|---|---|---|---|---|---|---|
| **Core** | **Series** | **Package** | **Flash Size** | **SRAM Size** | **Revision** | **Temperature** |
| Cortex®-M4F | 71: Base | M: LQFP44 (10x10 mm)<br>S: LQFP64 (7x7 mm)<br>R1: LQFP64 (14x14 mm) | D: 64 KB<br>E: 128 KB | 6: 32 KB | A | E:-40°C ~ 105°C |

### 3.3 M471M/M471R1/M471S Series Selection Guide

| Part Number | | M471 | | |
|---|---|---|---|---|
| | | MD6AE | R1E6AE | SE6AE |
| Flash (KB) | | 64 | 128 | 128 |
| SRAM (KB) | | 32 | | |
| Data Flash (KB) | | Configurable (Share with Flash) | | |
| LDROM (KB) | | 4 | | |
| System Frequency (MHz) | | 72 | | |
| I/O | | 35 | 49 | 49 |
| 32-bit Timer | | 4 | | |
| Connectivity | UART* | 3+1 | 4+1 | 4+1 |
| | SC*(ISO-7816) | 1 | | |
| | SPI | 1 | | |
| | Quad SPI | 1 | | |
| | $I^2C$ | 2 | | |
| | USB | - | Device/Host | Device/Host |
| PWM | | 10 | 12 | 12 |
| EBI | | 8-bit | 16-bit | 16-bit |
| PDMA | | 8-ch | | |
| RTC ($V_{BAT}$) | | √ | | |
| 12-bit SAR ADC | | 10 | 16 | 16 |
| VAI | | √ | | |
| Package | | LQFP44 (10x10mm) | LQFP64 (14x14mm) | LQFP64 (7x7mm) |

*Marked in this table (4+1) means 4 UART + 1 SC UART

*SC (ISO-7816) supports full duplex UART mode

# 4 PIN CONFIGURATION

The pin configuaration information can be found in Multi-function Pin Diagram sections or by using NuTool - PinConfig. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function pins correctly and handily.

## 4.1 Pin Configuration

### 4.1.1 Pin Diagram

#### *4.1.1.1 LQFP44 Pin Diagram*

Corresponding Part Number: M471MD6AE

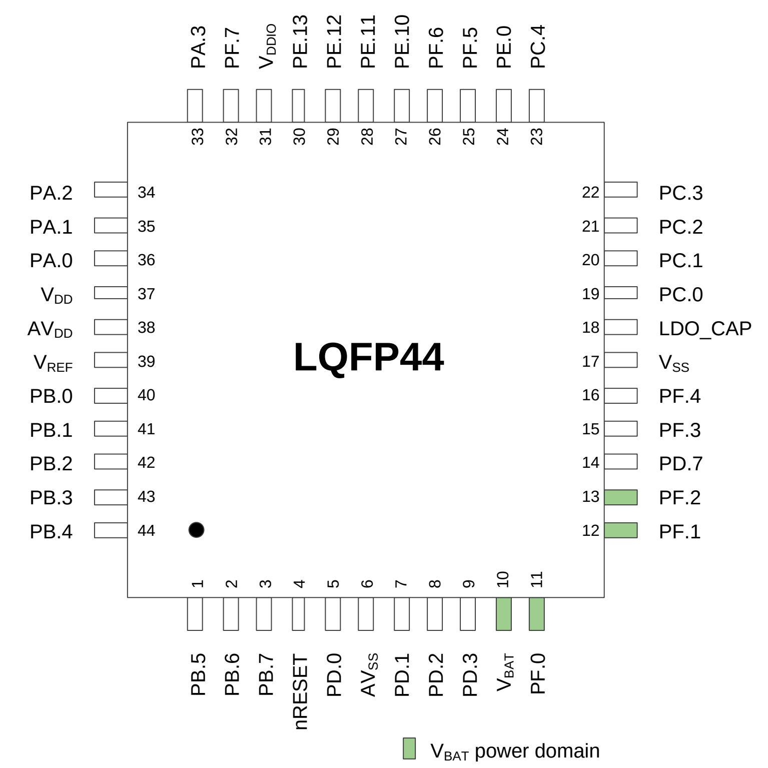



Figure 4.1-1 LQFP 44 Pin Diagram

### *4.1.1.2 LQFP64 Pin Diagram*

Corresponding Part Number: M471R1E6AE, M471SE6AE

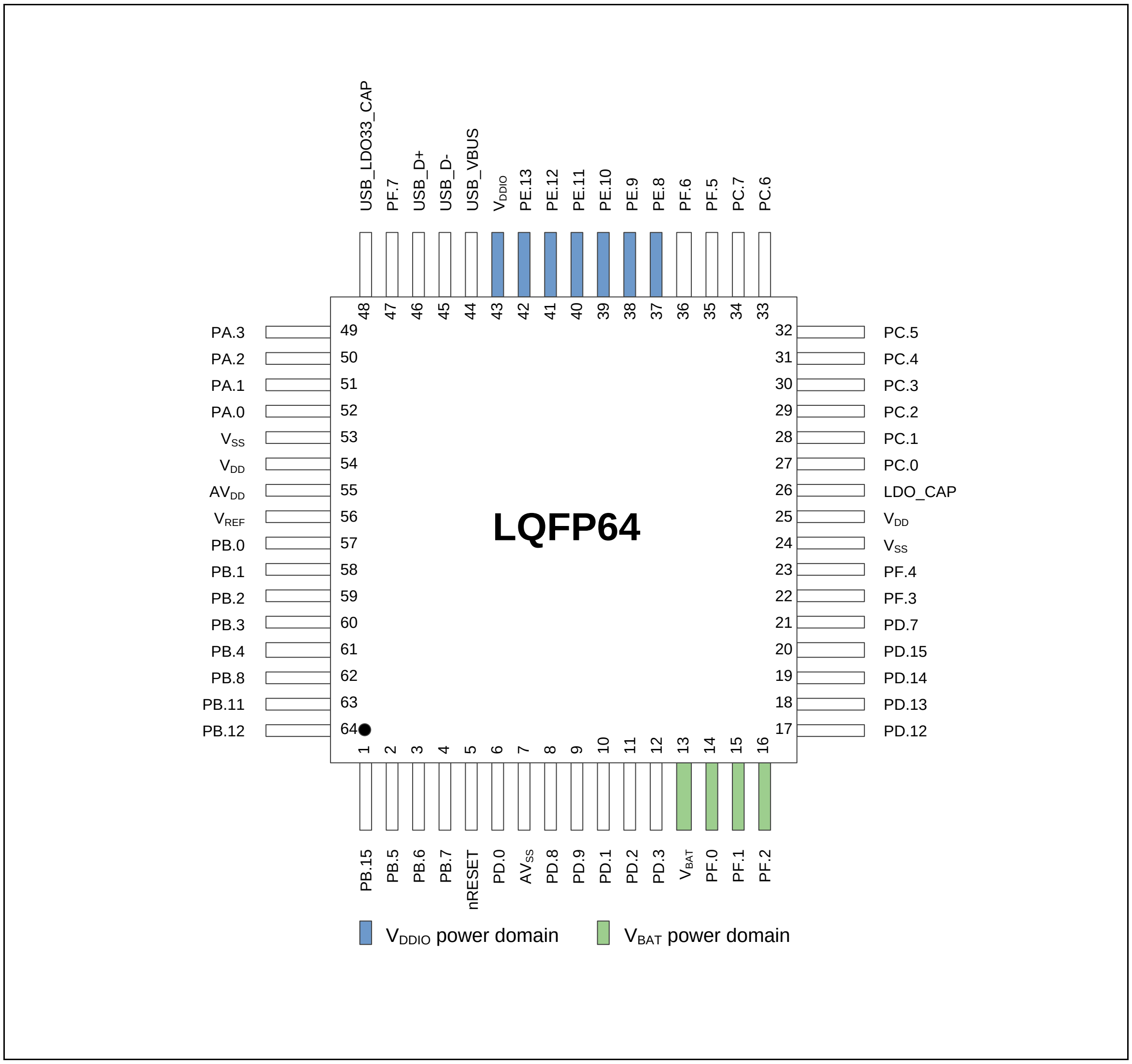



Figure 4.1-2 LQFP 64-pin Diagram

### 4.1.2 Multi-function Pin Diagram

#### *4.1.2.1 LQFP44 Multi-function Pin Diagram*

Corresponding Part Number: M471MD6AE

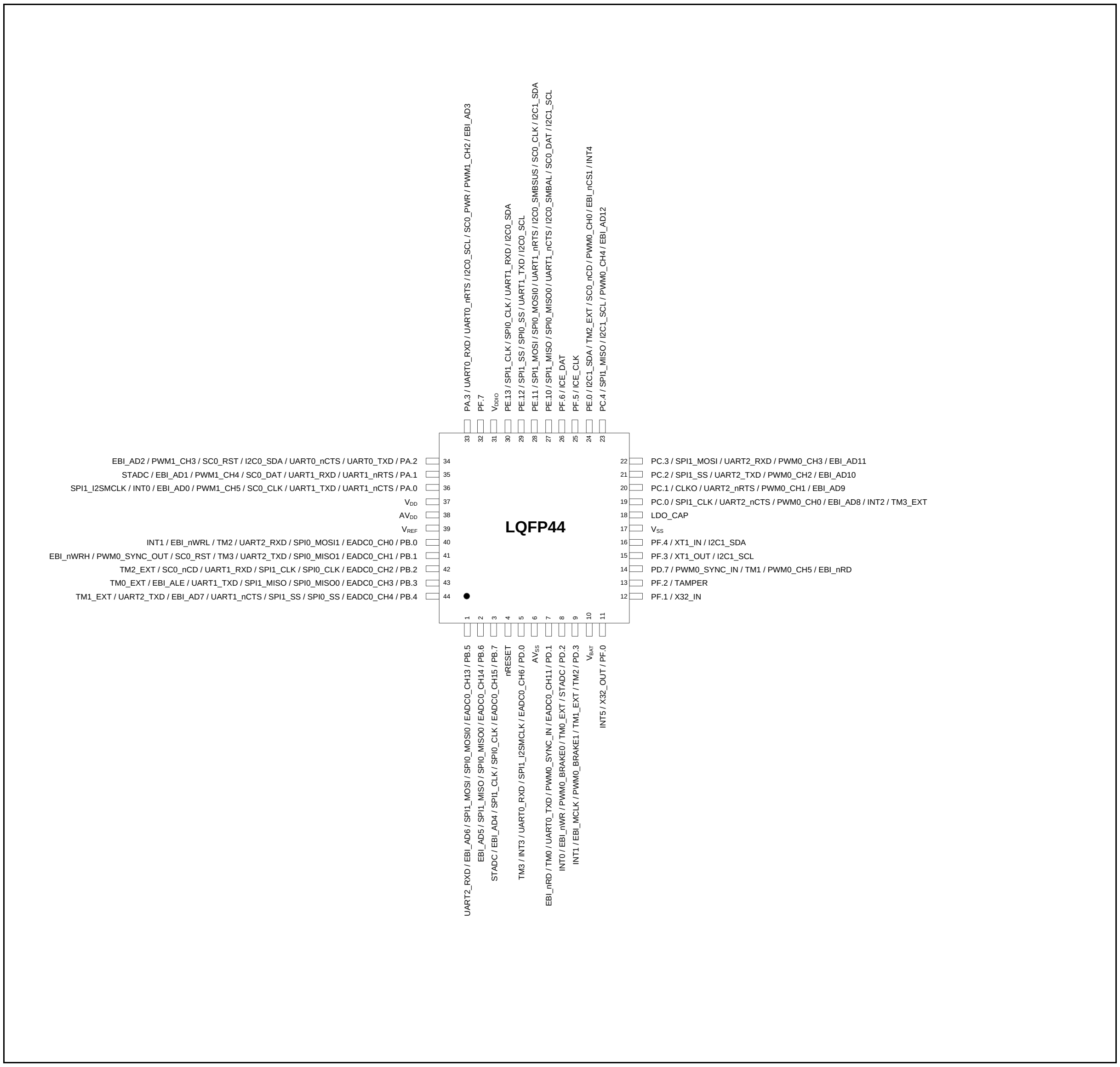


Figure 4.1-3 LQFP 44 Multi-function Pin Diagram

#### *4.1.2.2 LQFP64 Multi-function Pin Diagram*

Corresponding Part Number: M471R1E6AE, M471SE6AE

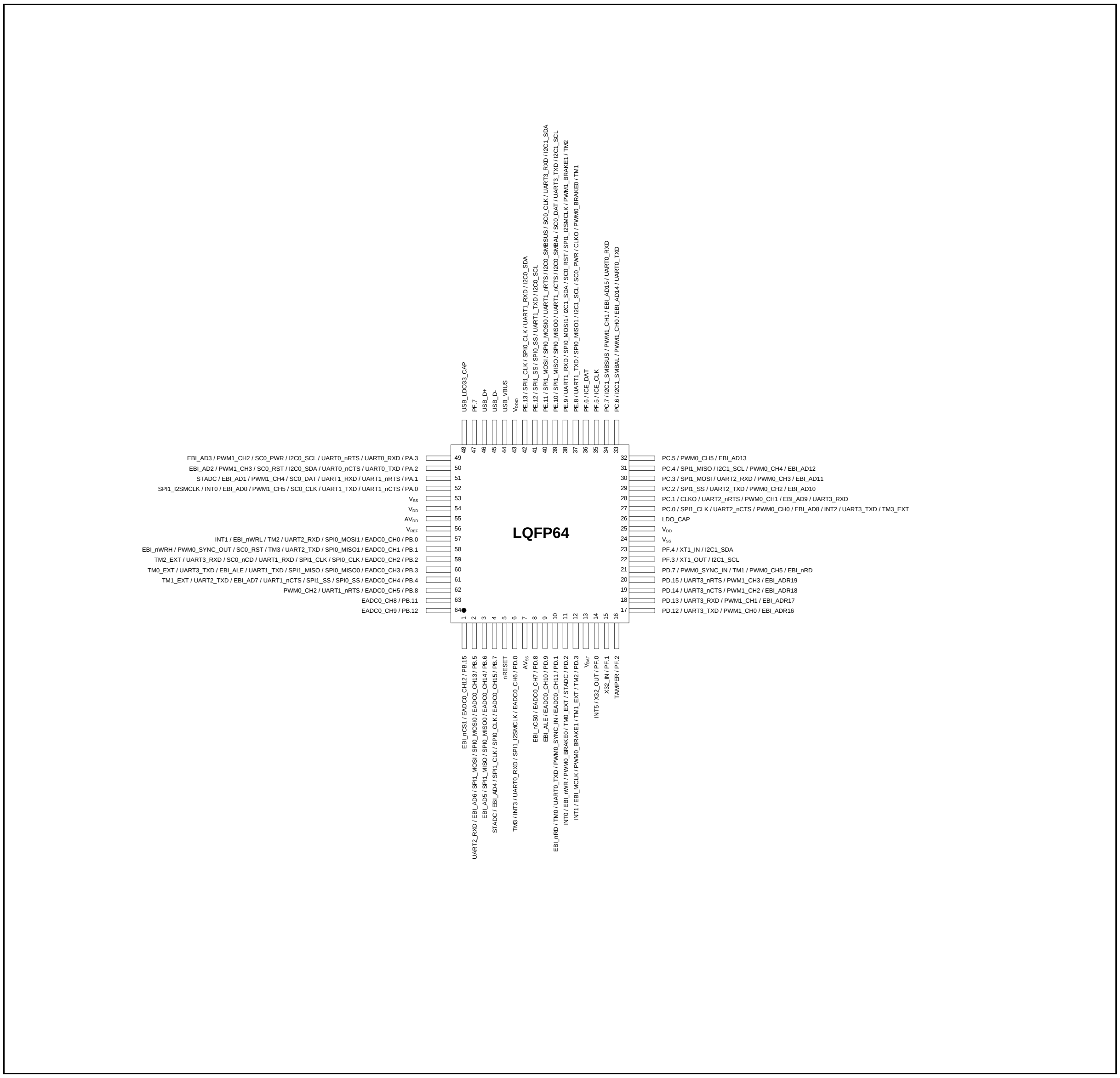


Figure 4.1-4 LQFP 64 Multi-function Pin Diagram

## 4.2 Pin Mapping

Different part number with the same package might have different function. Please refer to the selection guide in section 3.2, Pin Configuration in section 4.1 or NuTool - PinConfig.

**Corresponding Part Number: M471M/M471R1/M471S series.**

| | M471M/M471R1/M471S Series | |
|---|---|---|
| Pin Name | 64 Pin | 44 Pin |
| PB.15 | 1 | |
| PB.5 | 2 | 1 |
| PB.6 | 3 | 2 |
| PB.7 | 4 | 3 |
| nRESET | 5 | 4 |
| PD.0 | 6 | 5 |
| $AV_{SS}$ | 7 | 6 |
| $V_{DD}$ | | |
| PD.8 | 8 | |
| PD.9 | 9 | |
| PD.1 | 10 | 7 |
| PD.2 | 11 | 8 |
| PD.3 | 12 | 9 |
| $V_{RTC18}$ | | |
| $V_{BAT}$ | 13 | 10 |
| PF.0 | 14 | 11 |
| PF.1 | 15 | 12 |
| PF.2 | 16 | 13 |
| PD.12 | 17 | |
| PD.13 | 18 | |
| PD.14 | 19 | |
| PD.15 | 20 | |
| PD.7 | 21 | 14 |
| PF.3 | 22 | 15 |
| PF.4 | 23 | 16 |
| $V_{SS}$ | 24 | 17 |
| $V_{DD}$ | 25 | |
| LDO_CAP | 26 | 18 |
| PC.0 | 27 | 19 |

| | | |
|---|---|---|
| PC.1 | 28 | 20 |
| PC.2 | 29 | 21 |
| PC.3 | 30 | 22 |
| PC.4 | 31 | 23 |
| PE.0 | | 24 |
| PC.5 | 32 | |
| PC.6 | 33 | |
| PC.7 | 34 | |
| PF.5 | 35 | 25 |
| PF.6 | 36 | 26 |
| PE.8 | 37 | |
| PE.9 | 38 | |
| PE.10 | 39 | 27 |
| PE.11 | 40 | 28 |
| PE.12 | 41 | 29 |
| PE.13 | 42 | 30 |
| $V_{DDIO}$ | 43 | 31 |
| USB_$V_{BUS}$ | 44 | |
| USB_D- | 45 | |
| USB_D+ | 46 | |
| PF.7 | 47 | 32 |
| USB_LDO33_CAP | 48 | |
| PA.3 | 49 | 33 |
| PA.2 | 50 | 34 |
| PA.1 | 51 | 35 |
| PA.0 | 52 | 36 |
| $V_{SS}$ | 53 | |
| $V_{DD}$ | 54 | 37 |
| $AV_{DD}$ | 55 | 38 |
| $V_{REF}$ | 56 | 39 |
| PB.0 | 57 | 40 |
| PB.1 | 58 | 41 |
| PB.2 | 59 | 42 |
| PB.3 | 60 | 43 |
| PB.4 | 61 | 44 |

| | | |
|---|---|---|
| PB.8 | 62 | |
| PB.11 | 63 | |
| PB.12 | 64 | |

## 4.3 Pin Function Description

Corresponding Part Number: M471MD6AE, M471R1E6AE, M471SE6AE

### 4.3.1 Multi-function Summary Table

| Group | Pin Name | Type | Description |
|---|---|---|---|
| CLKO | CLKO | O | Clock Out |
| | | O | |
| EADC0 | EADC0_CH0 | A | EADC0 channel 0 analog input. |
| | EADC0_CH1 | A | EADC0 channel 1 analog input. |
| | EADC0_CH2 | A | EADC0 channel 2 analog input. |
| | EADC0_CH3 | A | EADC0 channel 3 analog input. |
| | EADC0_CH4 | A | EADC0 channel 4 analog input. |
| | EADC0_CH5 | A | EADC0 channel 5 analog input. |
| | EADC0_CH6 | A | EADC0 channel 6 analog input. |
| | EADC0_CH7 | A | EADC0 channel 7 analog input. |
| | EADC0_CH8 | A | EADC0 channel 8 analog input. |
| | EADC0_CH9 | A | EADC0 channel 9 analog input. |
| | EADC0_CH10 | A | EADC0 channel 10 analog input. |
| | EADC0_CH11 | A | EADC0 channel 11 analog input. |
| | EADC0_CH12 | A | EADC0 channel 12 analog input. |
| | EADC0_CH13 | A | EADC0 channel 13 analog input. |
| | EADC0_CH14 | A | EADC0 channel 14 analog input. |
| | EADC0_CH15 | A | EADC0 channel 15 analog input. |
| EBI | EBI_AD0 | I/O | EBI address/data bus bit 0. |
| | EBI_AD1 | I/O | EBI address/data bus bit 1. |
| | EBI_AD2 | I/O | EBI address/data bus bit 2. |
| | EBI_AD3 | I/O | EBI address/data bus bit 3. |
| | EBI_AD4 | I/O | EBI address/data bus bit 4. |
| | EBI_AD5 | I/O | EBI address/data bus bit 5. |
| | EBI_AD6 | I/O | EBI address/data bus bit 6. |
| | EBI_AD7 | I/O | EBI address/data bus bit 7. |
| | EBI_AD8 | I/O | EBI address/data bus bit 8. |
| | EBI_AD9 | I/O | EBI address/data bus bit 9. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | EBI_AD10 | I/O | EBI address/data bus bit 10. |
| | EBI_AD11 | I/O | EBI address/data bus bit 11. |
| | EBI_AD12 | I/O | EBI address/data bus bit 12. |
| | EBI_AD13 | I/O | EBI address/data bus bit 13. |
| | EBI_AD14 | I/O | EBI address/data bus bit 14. |
| | EBI_AD15 | I/O | EBI address/data bus bit 15. |
| | EBI_ADR16 | O | EBI address bus bit 16. |
| | EBI_ADR17 | O | EBI address bus bit 17. |
| | EBI_ADR18 | O | EBI address bus bit 18. |
| | EBI_ADR19 | O | EBI address bus bit 19. |
| | EBI_ALE | O | EBI address latch enable output pin. |
| | | O | |
| | EBI_MCLK | O | EBI external clock output pin. |
| | EBI_nCS0 | O | EBI chip select 0 output pin. |
| | EBI_nCS1 | O | EBI chip select 1 output pin. |
| | | O | |
| | EBI_nRD | O | EBI read enable output pin. |
| | | O | |
| | EBI_nWR | O | EBI write enable output pin. |
| | EBI_nWRH | O | EBI high byte write enable output pin |
| | EBI_nWRL | O | EBI low byte write enable output pin. |
| I2C0 | I2C0_SCL | I/O | $I^2C0$ clock pin. |
| | | I/O | |
| | I2C0_SDA | I/O | $I^2C0$ data input/output pin. |
| | | I/O | |
| | I2C0_SMBAL | O | $I^2C0$ SMBus SMBALTER pin |
| | I2C0_SMBSUS | O | $I^2C0$ SMBus SMBSUS pin (PMBus CONTROL pin) |
| I2C1 | I2C1_SCL | I/O | $I^2C1$ clock pin. |
| | | I/O | |
| | | I/O | |
| | | I/O | |
| | I2C1_SDA | I/O | $I^2C1$ data input/output pin. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | | I/O | |
| | | I/O | |
| | | I/O | |
| | I2C1_SMBAL | O | I²C1 SMBus SMBALTER pin |
| | I2C1_SMBSUS | O | I²C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| ICE | ICE_CLK | I | Serial wired debugger clock pin.<br>Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin. |
| | ICE_DAT | I/O | Serial wired debugger data pin.<br>Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin. |
| INT0 | INT0 | I | External interrupt 0 input pin. |
| | | I | |
| INT1 | INT1 | I | External interrupt 1 input pin. |
| | | I | |
| INT2 | INT2 | I | External interrupt 2 input pin. |
| INT3 | INT3 | I | External interrupt 3 input pin. |
| INT4 | INT4 | I | External interrupt 4 input pin. |
| INT5 | INT5 | I | External interrupt 5 input pin. |
| PWM0 | PWM0_BRAKE0 | I | PWM0 Brake 0 input pin. |
| | | I | |
| | PWM0_BRAKE1 | I | PWM0 Brake 1 input pin. |
| | PWM0_CH0 | I/O | PWM0 channel 0 output/capture input. |
| | | I/O | |
| | PWM0_CH1 | I/O | PWM0 channel 1 output/capture input. |
| | PWM0_CH2 | I/O | PWM0 channel 2 output/capture input. |
| | | I/O | |
| | PWM0_CH3 | I/O | PWM0 channel 3 output/capture input. |
| | PWM0_CH4 | I/O | PWM0 channel 4 output/capture input. |
| | PWM0_CH5 | I/O | PWM0 channel 5 output/capture input. |
| | | I/O | |
| | PWM0_SYNC_IN | I | PWM0 counter synchronous trigger input pin. |
| | | I | |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | PWM0_SYNC_OUT | O | PWM0 counter synchronous trigger output pin. |
| PWM1 | PWM1_BRAKE1 | I | PWM1 Brake 1 input pin. |
| | PWM1_CH0 | I/O | PWM1 channel 0 output/capture input. |
| | | I/O | |
| | PWM1_CH1 | I/O | PWM1 channel 1 output/capture input. |
| | | I/O | |
| | PWM1_CH2 | I/O | PWM1 channel 2 output/capture input. |
| | | I/O | |
| | PWM1_CH3 | I/O | PWM1 channel 3 output/capture input. |
| | | I/O | |
| | PWM1_CH4 | I/O | PWM1 channel 4 output/capture input. |
| | PWM1_CH5 | I/O | PWM1 channel 5 output/capture input. |
| SC0 | SC0_CLK | O | Smart Card 0 clock pin. |
| | | O | |
| | SC0_DAT | I/O | Smart Card 0 data pin. |
| | | I/O | |
| | SC0_PWR | O | Smart Card 0 power pin. |
| | | O | |
| | SC0_RST | O | Smart Card 0 reset pin. |
| | | O | |
| | | O | |
| | SC0_nCD | I | Smart Card 0 card detect pin. |
| | | I | |
| SPI0 | SPI0_CLK | I/O | SPI0 serial clock pin. |
| | | I/O | |
| | | I/O | |
| | SPI0_MISO0 | I/O | SPI0 MISO0 (Master In, Slave Out) pin. |
| | | I/O | |
| | | I/O | |
| | SPI0_MISO1 | I/O | SPI0 MISO1 (Master In, Slave Out) pin. |
| | | I/O | |
| | SPI0_MOSI0 | I/O | SPI0 MOSI0 (Master Out, Slave In) pin. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | | I/O | |
| | SPI0_MOSI1 | I/O | SPI0 MOSI1 (Master Out, Slave In) pin. |
| | | I/O | |
| | SPI0_SS | I/O | SPI0 slave select pin. |
| | | I/O | |
| SPI1 | SPI1_CLK | I/O | SPI1 serial clock pin. |
| | | I/O | |
| | | I/O | |
| | | I/O | |
| | SPI1_I2SMCLK | I/O | SPI1 I2S master clock output pin |
| | | I/O | |
| | | I/O | |
| | SPI1_MISO | I/O | SPI1 MISO (Master In, Slave Out) pin. |
| | | I/O | |
| | | I/O | |
| | | I/O | |
| | SPI1_MOSI | I/O | SPI1 MOSI (Master Out, Slave In) pin. |
| | | I/O | |
| | | I/O | |
| | SPI1_SS | I/O | SPI1 slave select pin. |
| | | I/O | |
| | | I/O | |
| STADC | STADC | I | ADC external trigger input. |
| | | I | |
| | | I | |
| TAMPER | TAMPER | I/O | TAMPER detector loop pin . |
| TM0 | TM0 | I/O | Timer0 event counter input/toggle output pin. |
| | TM0_EXT | I/O | Timer0 external capture input/toggle output pin. |
| | | I/O | |
| TM1 | TM1 | I/O | Timer1 event counter input/toggle output pin. |
| | | I/O | |
| | TM1_EXT | I/O | Timer1 external capture input/toggle output pin. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | | I/O | |
| TM2 | TM2 | I/O | Timer2 event counter input/toggle output pin. |
| | | I/O | |
| | | I/O | |
| | TM2_EXT | I/O | Timer2 external capture input/toggle output pin. |
| | | I/O | |
| TM3 | TM3 | I/O | Timer3 event counter input/toggle output pin. |
| | | I/O | |
| | TM3_EXT | I/O | Timer3 external capture input/toggle output pin. |
| UART0 | UART0_RXD | I | UART0 data receiver input pin. |
| | | I | |
| | | I | |
| | UART0_TXD | O | UART0 data transmitter output pin. |
| | | O | |
| | | O | |
| | UART0_nCTS | I | UART0 clear to Send input pin. |
| | UART0_nRTS | O | UART0 request to Send output pin. |
| UART1 | UART1_RXD | I | UART1 data receiver input pin. |
| | | I | |
| | | I | |
| | | I | |
| | UART1_TXD | O | UART1 data transmitter output pin. |
| | | O | |
| | | O | |
| | | O | |
| | UART1_nCTS | I | UART1 clear to Send input pin. |
| | | I | |
| | | I | |
| | UART1_nRTS | O | UART1 request to Send output pin. |
| | | O | |
| | | O | |
| UART2 | UART2_RXD | I | UART2 data receiver input pin. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | | I | |
| | | I | |
| | UART2_TXD | O | UART2 data transmitter output pin. |
| | | O | |
| | | O | |
| | UART2_nCTS | I | UART2 clear to Send input pin. |
| | UART2_nRTS | O | UART2 request to Send output pin. |
| UART3 | UART3_RXD | I | UART3 data receiver input pin. |
| | | I | |
| | | I | |
| | | I | |
| | UART3_TXD | O | UART3 data transmitter output pin. |
| | | O | |
| | | O | |
| | | O | |
| | UART3_nCTS | I | UART3 clear to Send input pin. |
| | UART3_nRTS | O | UART3 request to Send output pin. |
| X32 | X32_IN | I | External 32.768 kHz crystal input pin. |
| | X32_OUT | O | External 32.768 kHz crystal output pin. |
| XT1 | XT1_IN | I | External 4~20 MHz (high speed) crystal input pin. |
| | XT1_OUT | O | External 4~20 MHz (high speed) crystal output pin. |

# 5 BLOCK DIAGRAM

## 5.1 M471M/M471R1/M471S Series Block Diagram

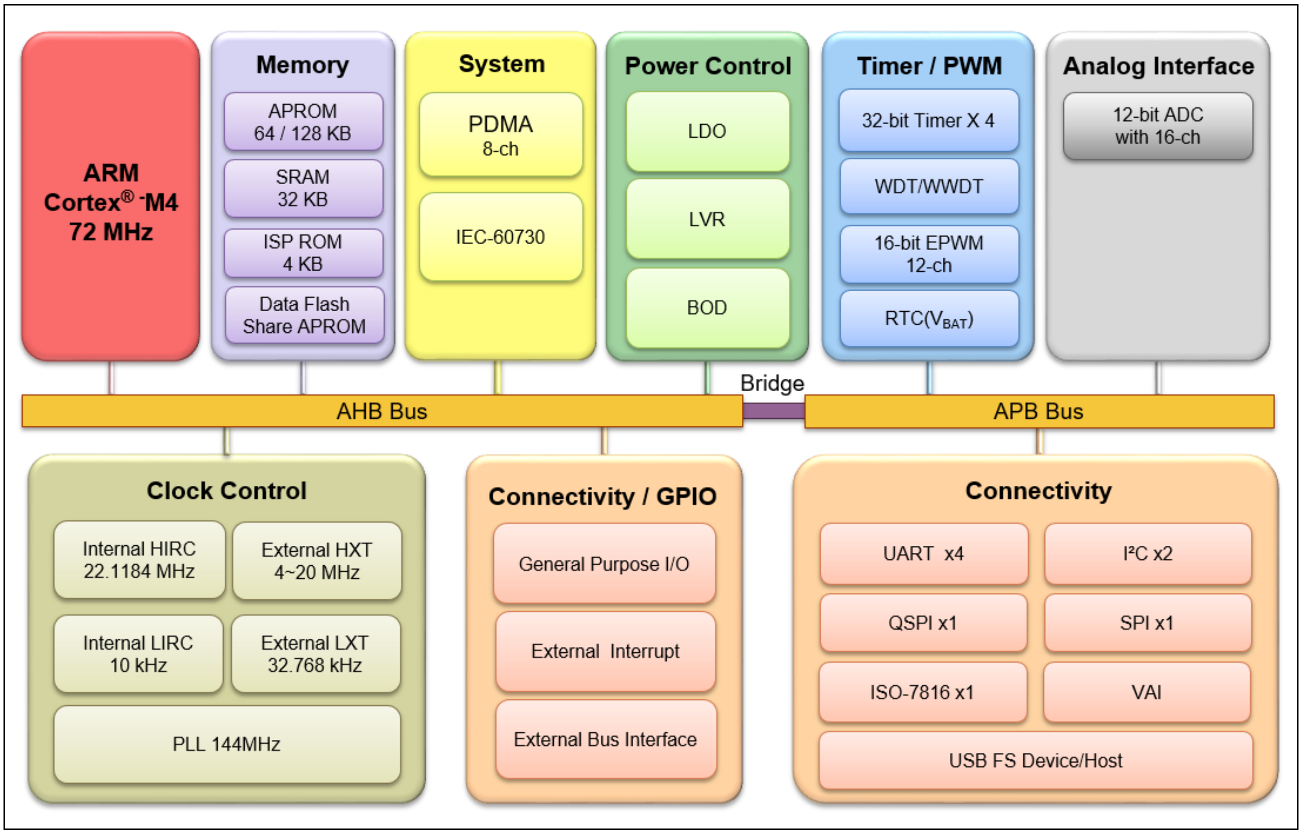



Figure 5.1-1 NuMicro® M471M/M471R1/M471S Block Diagram

# 6 FUNCTIONAL DESCRIPTION

## 6.1 Arm® Cortex®-M4 Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The NuMicro® M471M/M471R1/M471S family is embedded with Cortex®-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. Figure 6.1-1 shows the functional controller of the processor.

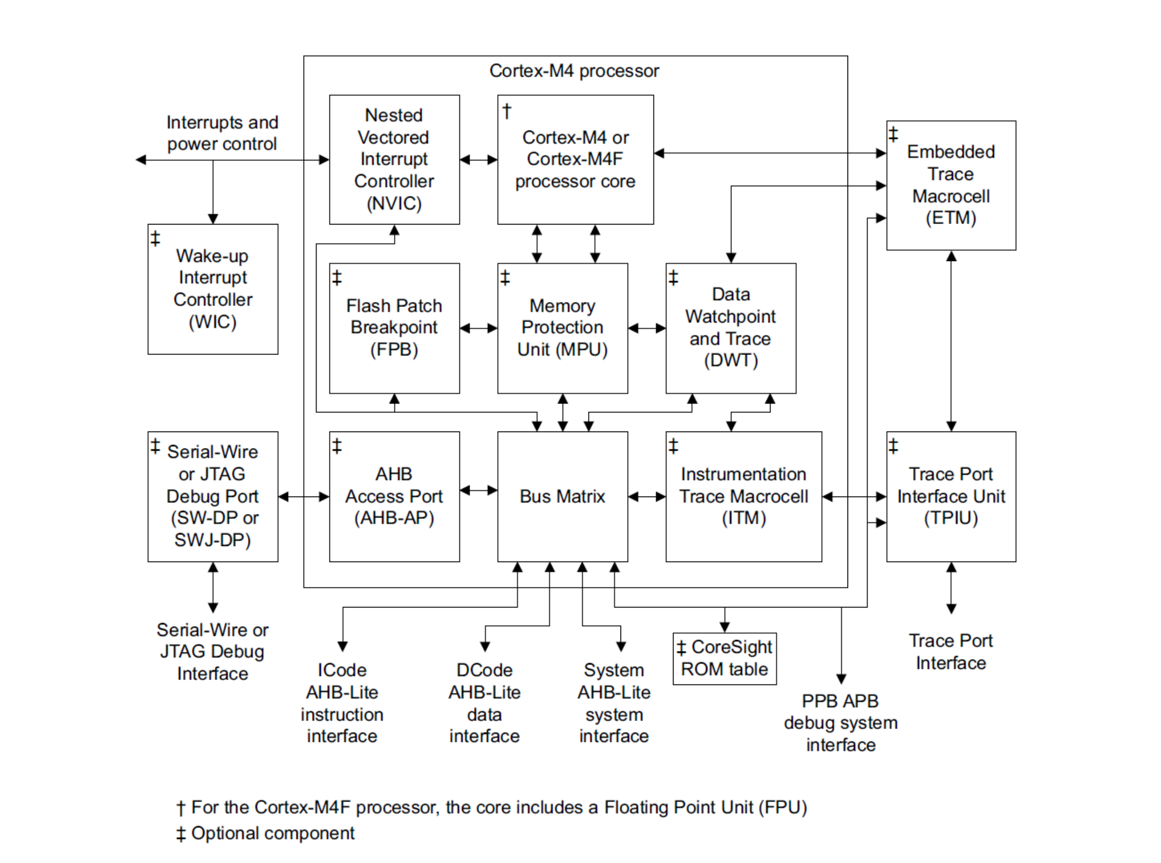



Figure 6.1-1 Cortex®-M4 Block Diagram

Cortex®-M4 processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *ARMv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)

- Hardware integer divide instructions, SDIV and UDIV
- Handler and Thread modes
- Thumb and Debug states
- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
- Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
- Support for ARMv6 big-endian byte-invariant or little-endian accesses
- Support for ARMv6 unaligned accesses

- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the NuMicro® M471M/M471R1/M471S family configured with 64 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tril-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is

halted, and access to debug control registers even while SYSRESETn is asserted.

- Serial Wire Debug Port(SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
- Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
- Optional Embedded Trace Macrocell (ETM) for instruction trace.

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

## 6.2 System Manager

### 6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for

- System Reset
- Power Modes and Wake-up Sources
- System Power Distribution
- SRAM Memory Organization
- System Control Register for Part Number ID, Chip Reset and Multi-function Pin Control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

### 6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset can reset chip through peripheral reset signals. Software reset can trigger reset through control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M4 core Only by writing 1 to CPURST (SYS_IPRST0[1])

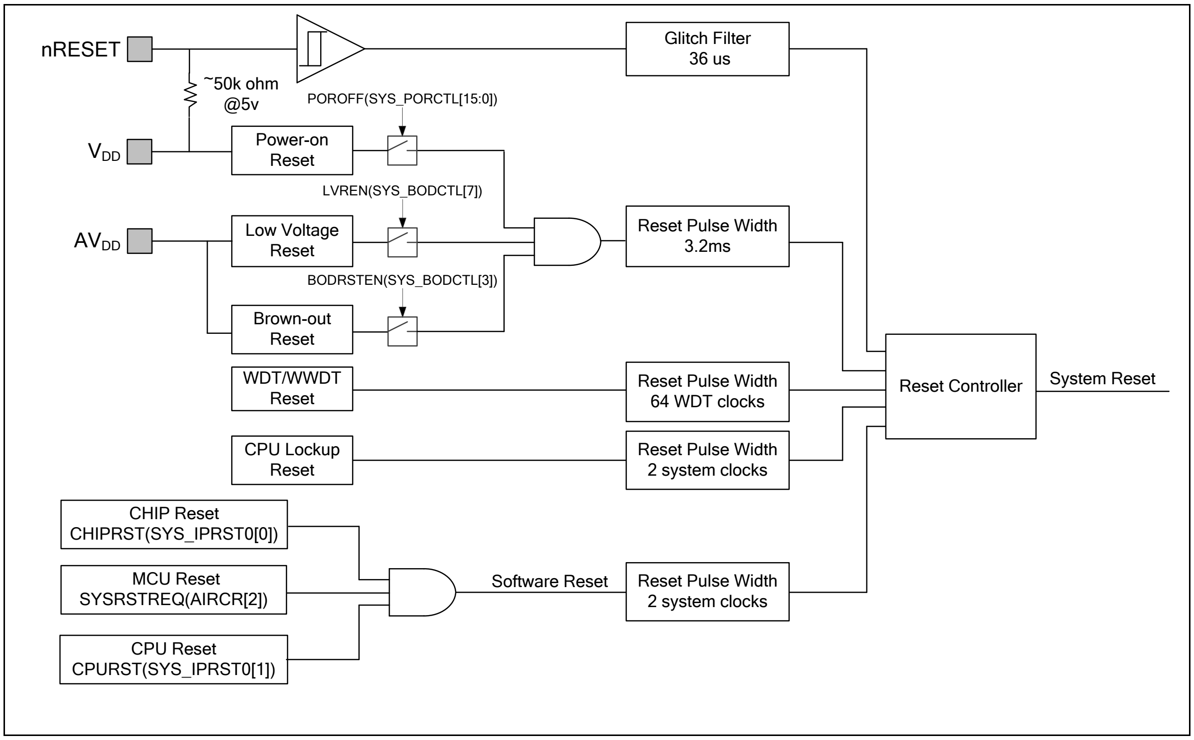



Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M4 only; the other reset sources will reset Cortex®-M4 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

| Reset Sources<br>Register | POR | nRESET | WDT | LVR | BOD | Lockup | CHIP | MCU | CPU |
|---|---|---|---|---|---|---|---|---|---|
| **SYS_RSTSTS** | 0x001 | Bit 1 = 1 | Bit 2 = 1 | Bit 3 = 1 | Bit 4 = 1 | Bit 8 = 1 | Bit 0 = 1 | Bit 5 = 1 | Bit 7 = 1 |
| **CHIPRST**<br>**(SYS_IPRST0[0])** | 0x0 | - | - | - | - | - | - | - | - |
| **BODEN**<br>**(SYS_BODCTL[0])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - |
| **BODVL**<br>**(SYS_BODCTL[2:1])** | | | | | | | | | |
| **BODRSTEN**<br>**(SYS_BODCTL[3])** | | | | | | | | | |
| **HXTEN**<br>**(CLK_PWRCTL[0])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | |
| **LXTEN**<br>**(CLK_PWRCTL[1])** | 0x0 | - | - | - | - | - | - | - | - |
| **WDTCKEN**<br>**(CLK_APBCLK0[0])** | 0x1 | - | 0x1 | - | - | - | 0x1 | - | - |
| **HCLKSEL**<br>**(CLK_CLKSEL0[2:0])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - |
| **WDTSEL**<br>**(CLK_CLKSEL1[1:0])** | 0x3 | 0x3 | - | - | - | - | - | - | - |
| **HXTSTB**<br>**(CLK_STATUS[0])** | 0x0 | - | - | - | - | - | - | - | - |
| **LXTSTB**<br>**(CLK_STATUS[1])** | 0x0 | - | - | - | - | - | - | - | - |
| **PLLSTB**<br>**(CLK_STATUS[2])** | 0x0 | - | - | - | - | - | - | - | - |
| **HIRCSTB**<br>**(CLK_STATUS[4])** | 0x0 | - | - | - | - | - | - | - | - |
| **CLKSFAIL**<br>**(CLK_STATUS[7])** | 0x0 | 0x0 | - | - | - | - | - | - | - |
| **RSTEN**<br>**(WDT_CTL[1])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| **WDTEN**<br>**(WDT_CTL[7])** | | | | | | | | | |
| **WDT_CTL**<br>**except bit 1 and bit 7.** | 0x0700 | 0x0700 | 0x0700 | 0x0700 | 0x0700 | - | 0x0700 | - | - |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **WDT_ALTCTL** | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| **WWDT_RLDCNT** | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| **WWDT_CTL** | 0x3F0800 | 0x3F0800 | 0x3F0800 | 0x3F0800 | 0x3F0800 | - | 0x3F0800 | - | - |
| **WWDT_STATUS** | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| **WWDT_CNT** | 0x3F | 0x3F | 0x3F | 0x3F | 0x3F | - | 0x3F | - | - |
| **BS (FMC_ISPCTL[1])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| **FMC_DFBA** | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | - | Reload from CONFIG1 | - | - |
| **CBS (FMC_ISPSTS[2:1])** | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| **PGFF (FMC_ISPSTS[5])** | 0x0 | - | 0x0 | - | - | - | 0x0 | - | - |
| **VECMAP (FMC_ISPSTS[23:9])** | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | - | Reload base on CONFIG0 | - | - |
| **Other Peripheral Registers** | Reset Value | | | | | | | | - |
| **FMC Registers** | Reset Value | | | | | | | | |
| **Note:** '-' means that the value of register keeps original setting. | | | | | | | | | |

Table 6.2-1 Reset Value of Registers

#### *6.2.2.1 nRESET Reset*

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 $V_{DD}$ and the state keeps longer than 36 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 $V_{DD}$ and the state keeps longer than 36 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

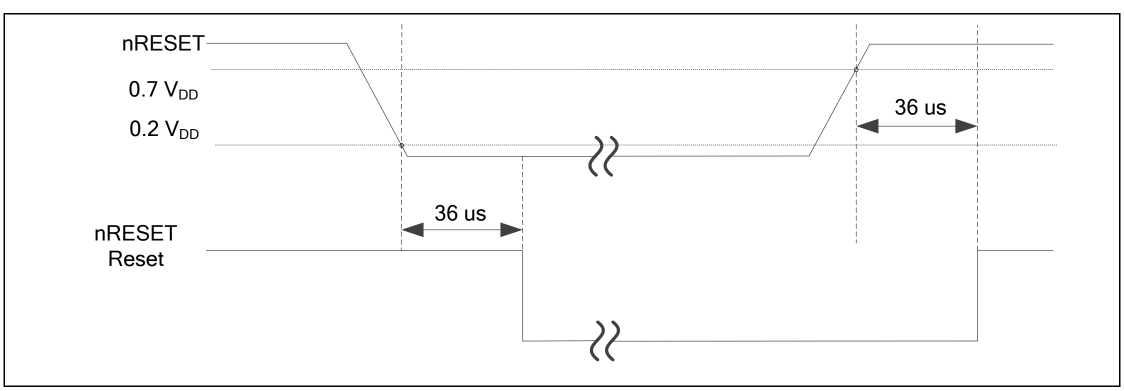


Figure 6.2-2 nRESET Reset Waveform

#### 6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

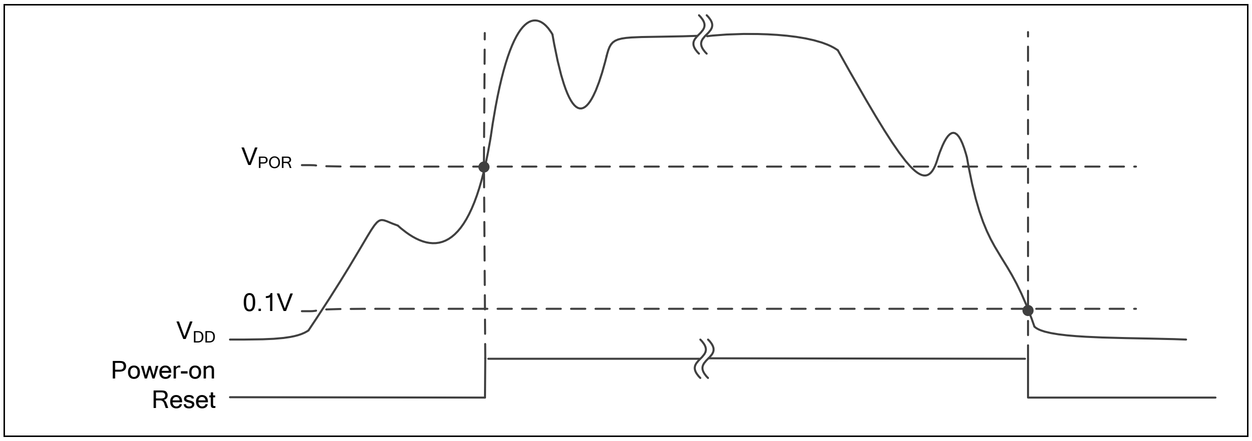



Figure 6.2-3 Power-on Reset (POR) Waveform

#### 6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect $AV_{DD}$ during system operation. When the $AV_{DD}$ voltage is lower than $V_{LVR}$ and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the $AV_{DD}$ voltage rises above $V_{LVR}$ and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The LVRF(SYS_RSTSTS[3]) will be set to 1 if the previous reset source is LVR. The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

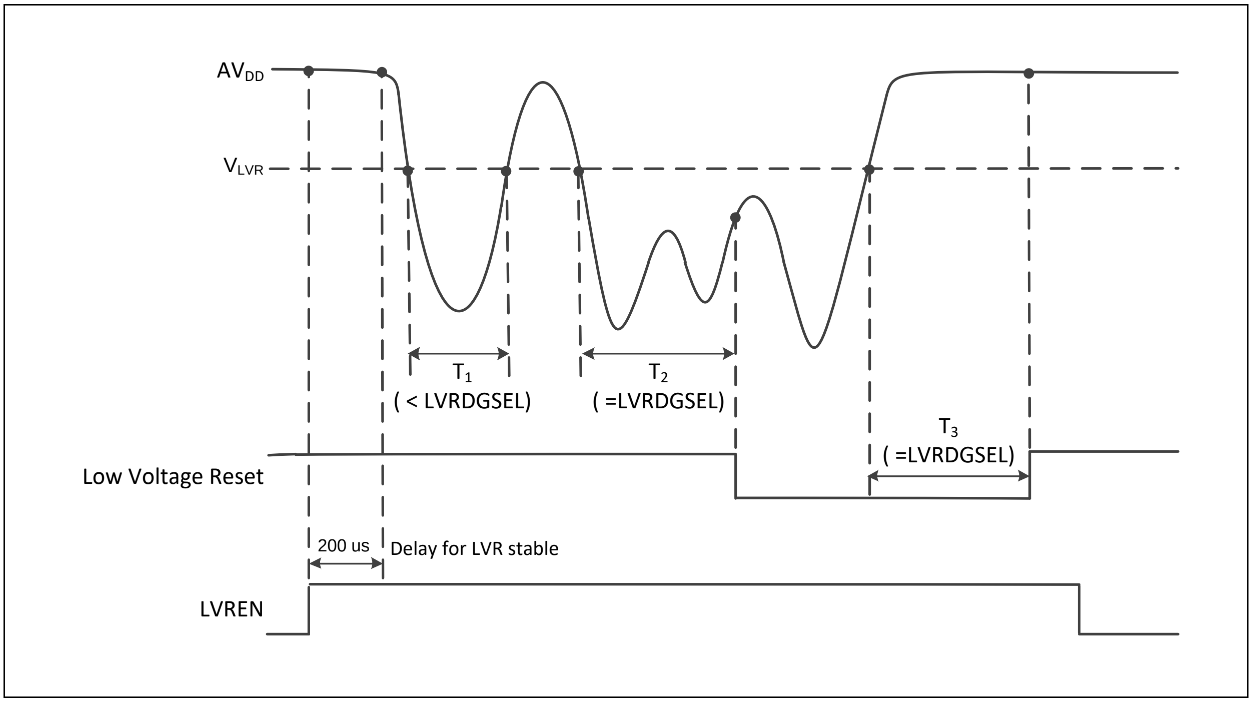



Figure 6.2-4 Low Voltage Reset (LVR) Waveform

#### *6.2.2.4 Brown-out Detector Reset (BOD Reset)*

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-Out Detector function will detect $AV_{DD}$ during system operation. When the $AV_{DD}$ voltage is lower than $V_{BOD}$ and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the $AV_{DD}$ voltage rises above $V_{BOD}$ and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]). The default value of BODEN, BODVL and BODRSTEN is set by Flash controller user configuration register CBODEN (CONFIG0 [23]), CBOV (CONFIG0 [22:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-Out Detector waveform.

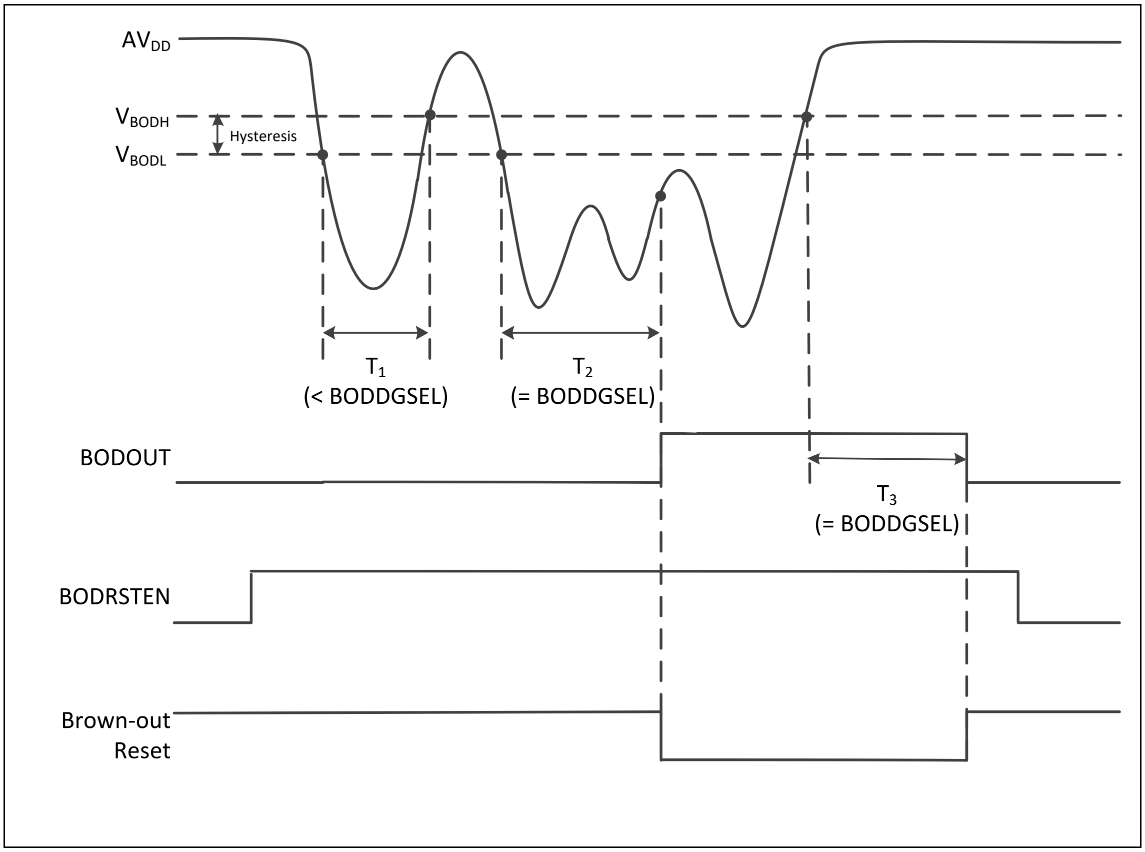



Figure 6.2-5 Brown-out Detector (BOD) Waveform

#### *6.2.2.5 Watchdog Timer Reset (WDT)*

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

#### *6.2.2.6 CPU Lockup Reset*

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

#### *6.2.2.7 CPU Reset, CHIP Reset and MCU Reset*

The CPU Reset means only Cortex®-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-On Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG setting. User can set the

CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

### 6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

| Power Mode | Normal Mode | Idle Mode | Power-Down Mode |
|---|---|---|---|
| **Definition** | CPU is in active state | CPU is in sleep state | CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended. |
| **Entry Condition** | Chip is in normal mode after system reset released | CPU executes WFI instruction. | CPU sets sleep mode enable and power down enable and executes WFI instruction. |
| **Wake-up Sources** | N/A | All interrupts | RTC, WDT, I²C, Timer, UART, BOD, GPIO and USBD |
| **Available Clocks** | All | All except CPU clock | LXT and LIRC |
| **After Wake-up** | N/A | CPU back to normal mode | CPU back to normal mode |

Table 6.2-2 Power Mode Difference Table

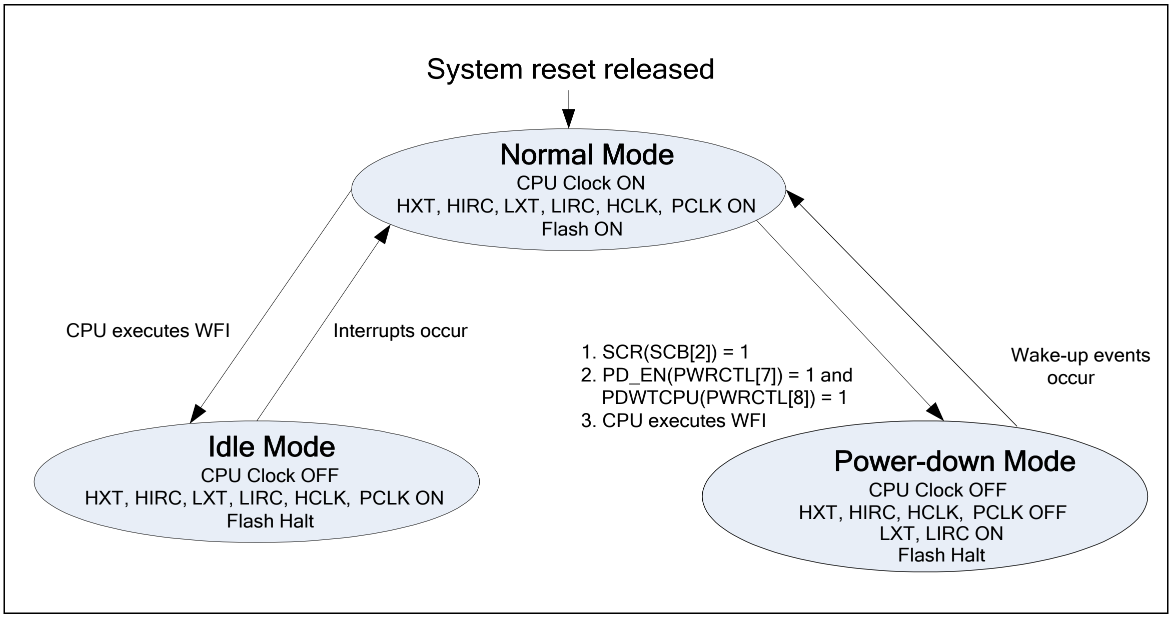



Figure 6.2-6 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in run mode.
2. LIRC (10 kHz OSC) ON or OFF depends on S/W setting in run mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.

| | Normal Mode | Idle Mode | Power-Down Mode |
|---|---|---|---|
| HXT (4~20 MHz XTL) | ON | ON | Halt |
| HIRC (12/16 MHz OSC) | ON | ON | Halt |
| LXT (32768 Hz XTL) | ON | ON | ON/OFF[1] |
| LIRC (10 kHz OSC) | ON | ON | ON/OFF[2] |
| PLL | ON | ON | Halt |
| LDO | ON | ON | ON |
| CPU | ON | Halt | Halt |
| HCLK/PCLK | ON | ON | Halt |
| SRAM retention | ON | ON | ON |
| FLASH | ON | ON | Halt |
| EBI | ON | ON | Halt |
| GPIO | ON | ON | Halt |
| PDMA | ON | ON | Halt |
| TIMER | ON | ON | ON/OFF[3] |
| PWM | ON | ON | Halt |
| WDT | ON | ON | ON/OFF[4] |
| WWDT | ON | ON | Halt |
| RTC | ON | ON | ON/OFF[5] |
| UART | ON | ON | Halt |
| SC | ON | ON | Halt |
| $I^2C$ | ON | ON | Halt |
| SPI | ON | ON | Halt |
| USBD | ON | ON | Halt |
| EADC | ON | ON | Halt |

Table 6.2-3 Clocks in Power Modes

**Wake-up sources in Power-down mode:**

RTC, WDT, $I^2C$, Timer, UART, BOD, GPIO and USBD

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

| Wake-Up Source | Wake-Up Condition | System Can Enter Power-Down Mode Again Condition* |
|---|---|---|
| BOD | Brown-Out Detector Interrupt | After software writes 1 to clear SYS_BODCTL[BODIF]. |
| GPIO | GPIO Interrupt | After software write 1 to clear the INTSRC[n] bit. |
| TIMER | Timer Interrupt | After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]). |
| WDT | WDT Interrupt | After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect). |
| RTC | Alarm Interrupt | After software writes 1 to clear ALMIF (RTC_INTSTS[0]). |
| | Time Tick Interrupt | After software writes 1 to clear TICKIF (RTC_INTSTS[1]). |
| | Snoop Detection Interrupt | After software writes 1 to clear SNPDIF (RTC_INTSTS[2]). |
| UART | RX Data wake-up | After software writes 1 to clear DATWKIF (UARTx_INTSTS[17]). |
| | nCTS wake-up | After software writes 1 to clear CTSWKIF (UARTx_INTSTS[16]). |
| $I^2C$ | Falling edge in the I2C_SDA or I2C_CLK | After software writes 1 to clear WKIF( I2C_WKSTS[0]). |
| USBD | Remote Wake-up | After software writes 1 to clear BUSIF (USBD_INTSTS[0]). |

Table 6.2-4 Condition of Entering Power-down Mode Again

### 6.2.4 System Power Distribution

In this chip, power distribution is divided into five segments:

- Analog power from $AV_{DD}$ and $AV_{SS}$ provides the power for analog components operation. The $V_{REF}$ should be connected with an external 1uF capacitor that should be located close to the $V_{REF}$ pin to avoid power noise for analog applications.
- Digital power from $V_{DD}$ and $V_{SS}$ supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from $V_{BUS}$ offers the power for operating the USB transceiver.
- RTC power from $V_{BAT}$ provides the power for PF.0~PF.2, RTC and 80 bytes backup registers.
- A dedicated power from $V_{DDIO}$ supplies the power for PE.8~PE.13.

The outputs of internal voltage regulators, LDO_CAP and USB_VDD33_CAP, require an external capacitor which should be located close to the corresponding pin. Analog power ($AV_{DD}$) should be the same voltage level of the digital power ($V_{DD}$). Figure 6.2-7 shows the NuMicro® M471M/M471R1/M471S series power distribution.

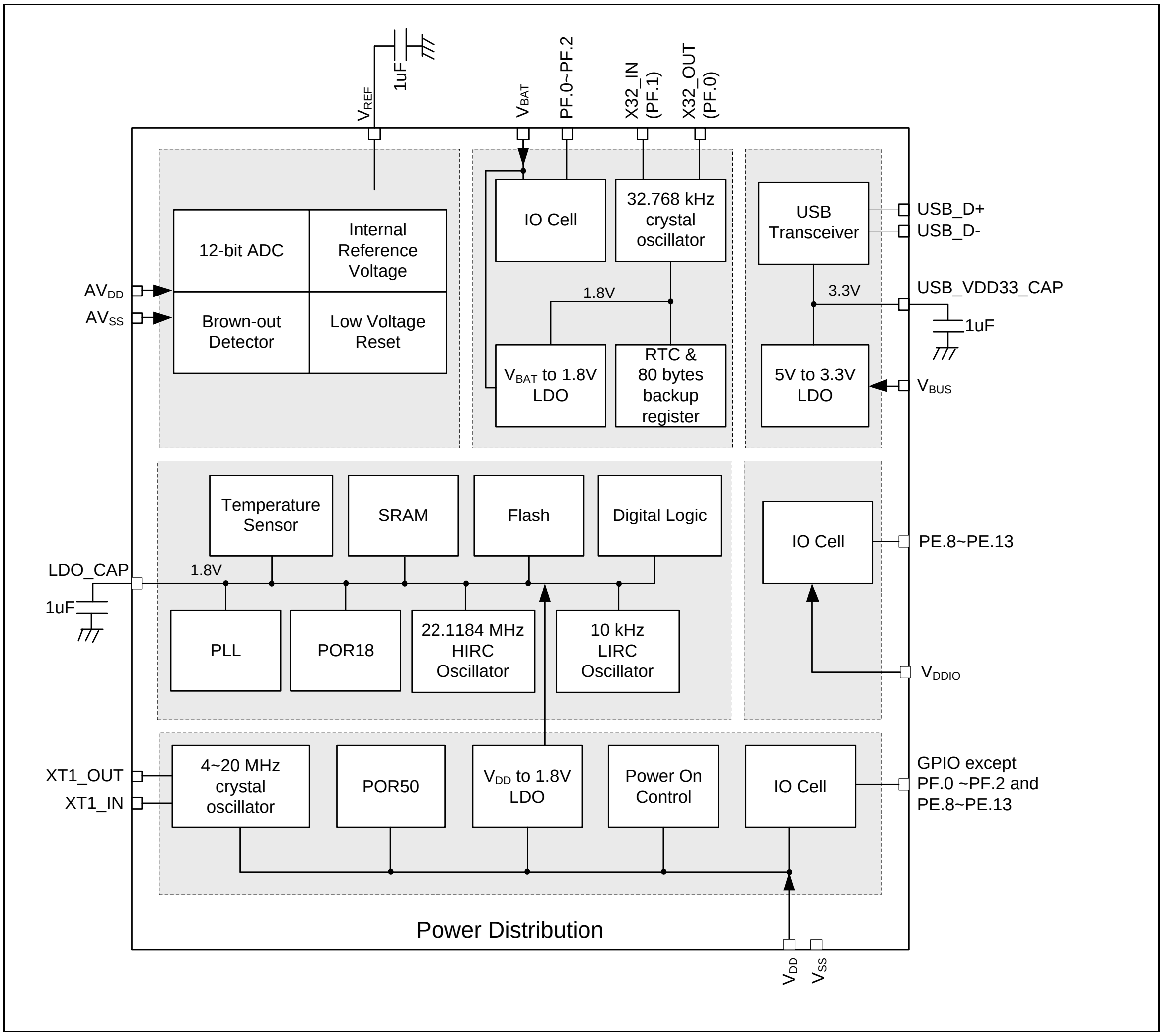



Figure 6.2-7 NuMicro® M471M/M471R1/M471S Series Power Distribution Diagram

### 6.2.5 System Memory Map

The NuMicro® M471M/M471R1/M471S series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-5. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M471M/M471R1/M471S series only supports little-endian data format.

| Address Space | Token | Controllers |
|---|---|---|
| **Flash and SRAM Memory Space** | | |
| 0x0000_0000 – 0x0001_FFFF | FLASH_BA | FLASH Memory Space (128KB) |
| 0x0004_0000 – 0x0005_FFFF | Reserved | Reserved |
| 0x0006_0000 – 0x0007_FFFF | Reserved | Reserved |
| 0x2000_4000 – 0x2000_7FFF | SRAM1_BA | SRAM Memory Space |
| 0x2000_8000 – 0x2000_BFFF | Reserved | Reserved |
| 0x2000_C000 – 0x2000_FFFF | Reserved | Reserved |
| 0x6000_0000 – 0x6FFF_FFFF | EXTMEM_BA | External Memory Space for EBI Interface (256 MB) |
| **Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)** | | |
| 0x4000_0000 – 0x4000_01FF | SYS_BA | System Control Registers |
| 0x4000_0200 – 0x4000_02FF | CLK_BA | Clock Control Registers |
| 0x4000_0300 – 0x4000_03FF | NMI_BA | NMI Control Registers |
| 0x4000_4000 – 0x4000_4FFF | GPIO_BA | GPIO Control Registers |
| 0x4000_8000 – 0x4000_8FFF | PDMA_BA | Peripheral DMA Control Registers |
| 0x4000_9000 – 0x4000_9FFF | UHC_BA | USB Host Control Registers |
| 0x4000_B000 – 0x4000_BFFF | Reserved | Reserved |
| 0x4000_C000 – 0x4000_CFFF | FMC_BA | Flash Memory Control Registers |
| 0x4000_D000 – 0x4000_DFFF | Reserved | Reserved |
| 0x4001_0000 – 0x4001_0FFF | EBI_BA | External Bus Interface Control Registers |
| 0x4001_9000 – 0x4001_9FFF | Reserved | Reserved |
| 0x4003_0000 – 0x4003_0FFF | Reserved | Reserved |
| 0x4003_1000 – 0x4003_1FFF | CRC_BA | CRC Generator Registers |
| 0x5000_8000 – 0x5000_FFFF | Reserved | Reserved |
| **APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)** | | |
| 0x4004_0000 – 0x4004_0FFF | WDT_BA | Watchdog Timer Control Registers |
| 0x4004_1000 – 0x4004_1FFF | RTC_BA | Real Time Clock (RTC) Control Register |
| 0x4004_3000 – 0x4004_3FFF | EADC_BA | Enhanced Analog-Digital-Converter (EADC) Control Registers |
| 0x4004_4000 – 0x4004_4FFF | Reserved | Reserved |
| 0x4004_5000 – 0x4004_5FFF | Reserved | Reserved |
| 0x4004_6000 – 0x4004_6FFF | Reserved | Reserved |
| 0x4004_7000 – 0x4004_7FFF | Reserved | Reserved |

| | | |
|---|---|---|
| 0x4004_8000 – 0x4004_8FFF | Reserved | Reserved |
| 0x4004_9000 – 0x4004_9FFF | Reserved | Reserved |
| 0x4004_D000 – 0x4004_DFFF | Reserved | Reserved |
| 0x4005_0000 – 0x4005_0FFF | TMR01_BA | Timer0/Timer1 Control Registers |
| 0x4005_1000 – 0x4005_1FFF | TMR23_BA | Timer2/Timer3 Control Registers |
| 0x4005_8000 – 0x4005_8FFF | PWM0_BA | PWM0 Control Registers |
| 0x4005_9000 – 0x4005_9FFF | PWM1_BA | PWM1 Control Registers |
| 0x4005_C000 – 0x4005_CFFF | Reserved | Reserved |
| 0x4005_D000 – 0x4005_DFFF | Reserved | Reserved |
| 0x4006_0000 – 0x4006_0FFF | SPI0_BA | SPI0 Control Registers |
| 0x4006_1000 – 0x4006_1FFF | SPI1_BA | SPI1 Control Registers |
| 0x4006_2000 – 0x4006_2FFF | Reserved | Reserved |
| 0x4006_3000 – 0x4006_3FFF | Reserved | Reserved |
| 0x4007_0000 – 0x4007_0FFF | UART0_BA | UART0 Control Registers |
| 0x4007_1000 – 0x4007_1FFF | UART1_BA | UART1 Control Registers |
| 0x4007_2000 – 0x4007_2FFF | UART2_BA | UART2 Control Registers |
| 0x4007_3000 – 0x4007_3FFF | UART3_BA | UART3 Control Registers |
| 0x4007_4000 – 0x4007_4FFF | Reserved | Reserved |
| 0x4007_5000 – 0x4007_5FFF | Reserved | Reserved |
| 0x4008_0000 – 0x4008_0FFF | I2C0_BA | $I^2C0$ Control Registers |
| 0x4008_1000 – 0x4008_1FFF | I2C1_BA | $I^2C1$ Control Registers |
| 0x4008_2000 – 0x4008_2FFF | Reserved | Reserved |
| 0x4008_3000 – 0x4008_3FFF | Reserved | Reserved |
| 0x4008_4000 – 0x4008_4FFF | Reserved | Reserved |
| 0x4009_0000 – 0x4009_0FFF | SC0_BA | Smartcard Host 0 Control Registers |
| 0x4009_1000 – 0x4009_1FFF | Reserved | Reserved |
| 0x4009_2000 – 0x4009_2FFF | Reserved | Reserved |
| 0x4009_3000 – 0x4009_3FFF | Reserved | Reserved |
| 0x4009_4000 – 0x4009_4FFF | Reserved | Reserved |
| 0x4009_5000 – 0x4009_5FFF | Reserved | Reserved |
| 0x400A_0000 – 0x400A_0FFF | Reserved | Reserved |
| 0x400A_1000 – 0x400A_1FFF | Reserved | Reserved |
| 0x400B_0000 – 0x400B_0FFF | Reserved | Reserved |
| 0x400B_1000 – 0x400B_1FFF | Reserved | Reserved |
| 0x400B_0000 – 0x400B_0FFF | Reserved | Reserved |

| | | |
|---|---|---|
| 0x400B_1000 – 0x400B_1FFF | Reserved | Reserved |
| 0x400C_0000 – 0x400C_0FFF | USBD_BA | USB Device Control Register |
| 0x400E_0000 – 0x400E_0FFF | Reserved | Reserved |
| 0x400E_2000 – 0x400E_2FFF | Reserved | Reserved |
| 0x5008_0000 – 0x5008_0FFF | Reserved | Reserved |
| **System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)** | | |
| 0xE000_E010 – 0xE000_E0FF | SCS_BA | System Timer Control Registers |
| 0xE000_E100 – 0xE000_ECFF | SCS_BA | External Interrupt Controller Control Registers |
| 0xE000_ED00 – 0xE000_ED8F | SCS_BA | System Control Registers |

Table 6.2-5 Address Space Assignments for On-Chip Controllers

### 6.2.6 SRAM Memory Organization

The M471M/M471R1/M471S series supports embedded SRAM with total 32 KB size and the SRAM organization is separated to two banks: SRAM bank0 and SRAM bank1. Each of these two banks has 16 KB address space and can be accessed simultaneously.

- Supports total 32 KB SRAM
- Supports byte / half word / word write
- Supports fixed 16 KB SRAM bank for independent access
- Supports oversize response error
- Supports remap address to 0x1000_0000

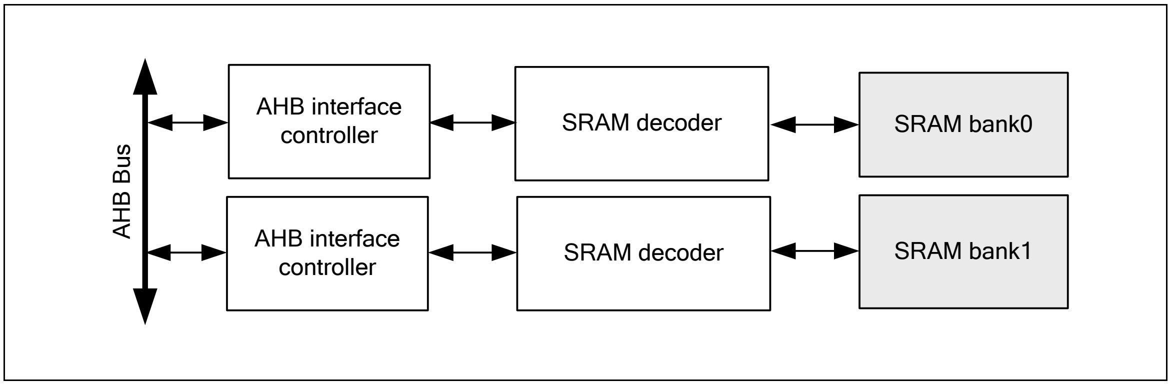



Figure 6.2-8 SRAM Block Diagram

Figure 6.2-9 shows the M471M/M471R1/M471S series SRAM organization. There are two SRAM banks in M471M/M471R1/M471S and each bank is addressed to 16 KB. The bank0 address space is from 0x2000_0000 to 0x2000_3FFF. The bank1 address space is from 0x2000_4000 to 0x2000_7FFF. The address between 0x2000_8000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

The address of each bank is remapping from 0x2000_0000 to 0x1000_0000. CPU can read SRAM bank0 through 0x2000_0000 to 0x2000_3FFF or 0x1000_0000 to 0x1000_3FFF, and read SRAM bank1 through 0x2000_4000 to 0x2000_7FFF or 0x1000_4000 to 0x1000_7FFF.

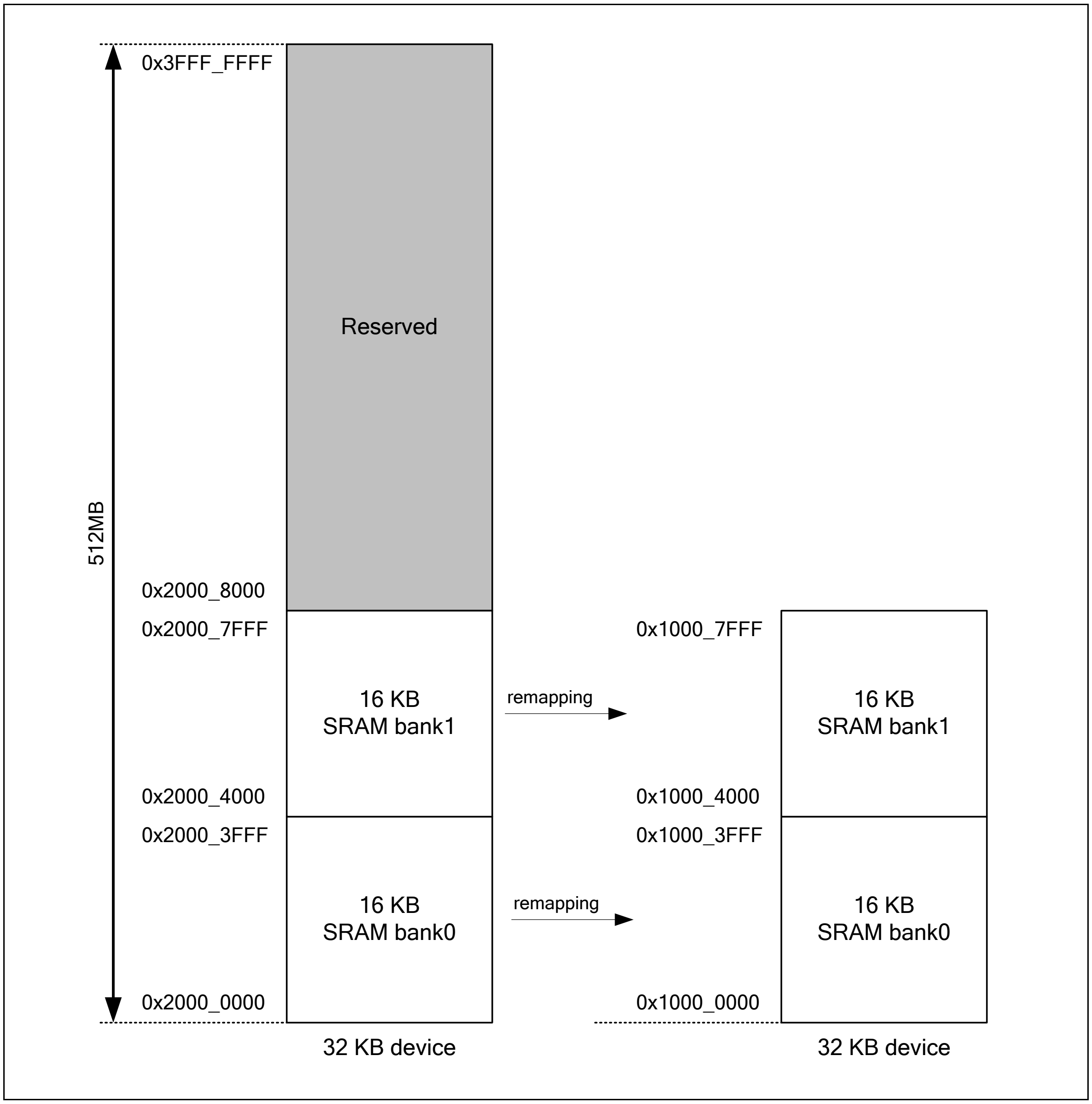



Figure 6.2-9 SRAM Memory Organization

### 6.2.7 System Timer (SysTick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “*Arm® Cortex®-M4 Technical Reference Manual*” and “*Arm® v6-M Architecture Reference Manual*”.

### 6.2.8 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

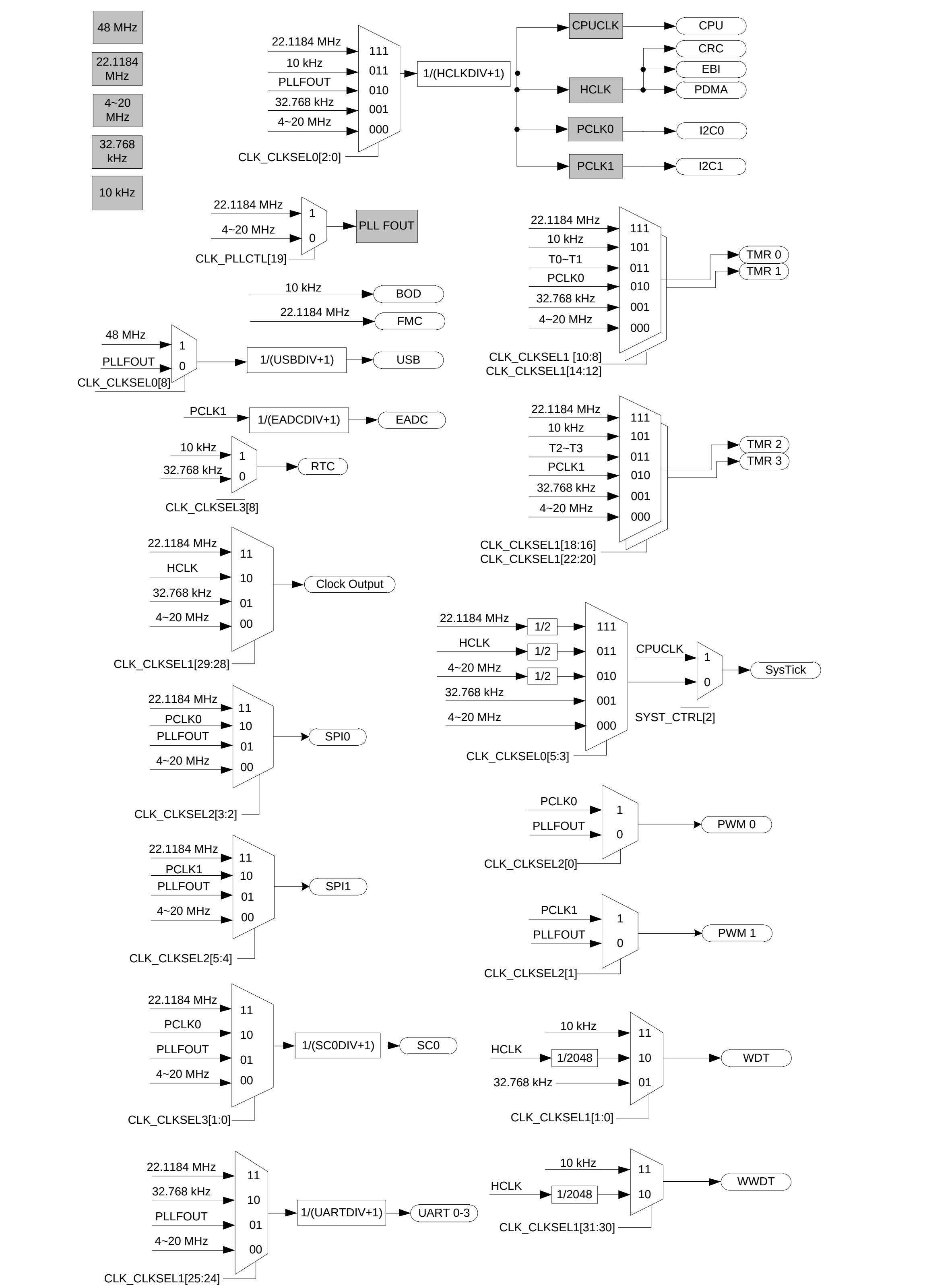
- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-15 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

## 6.3 Clock Controller

### 6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M4 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~20 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.




**Note:** Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-1 Clock Generator Global View Diagram

### 6.3.2 Clock Generator

The clock generator consists of 6 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~20 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~20 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)
- 48 MHz internal high speed RC oscillator (HIRC48M)

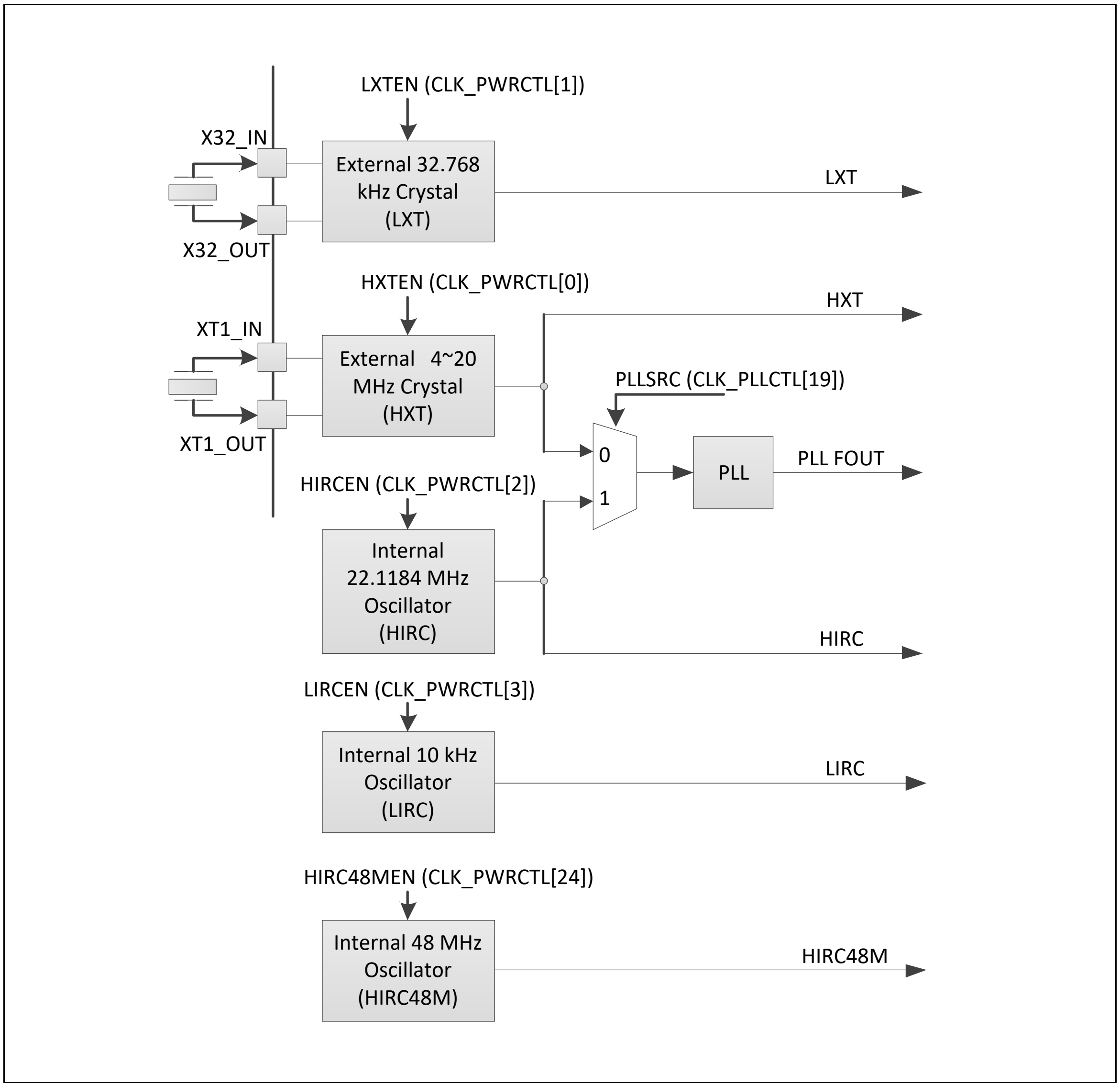
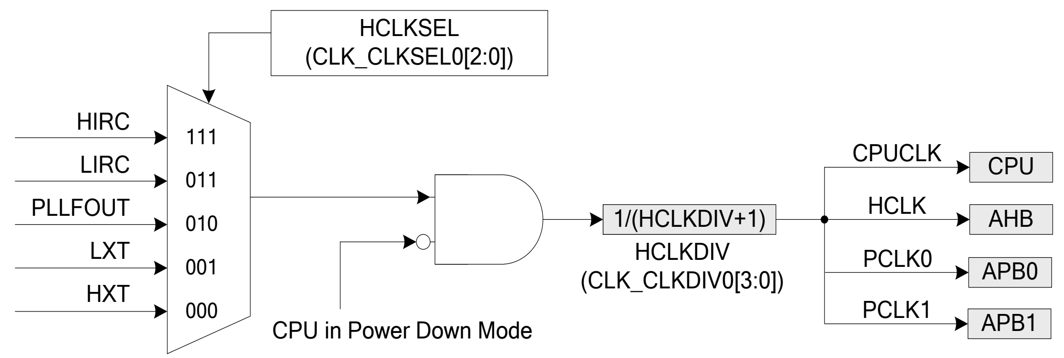



Figure 6.3-2 Clock Generator Block Diagram

### 6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.




**Note:** Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.3-4.

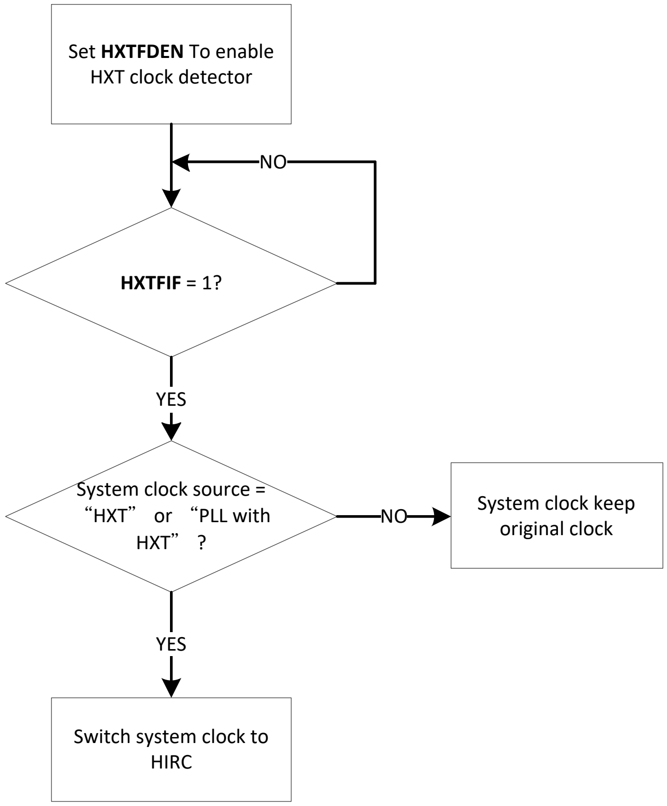
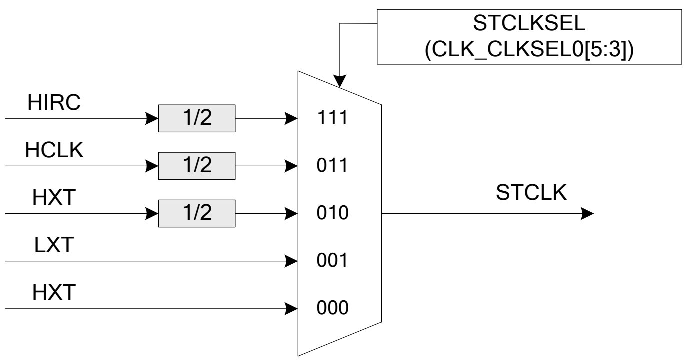



Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M4 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.




**Note:** Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-5 SysTick Clock Control Block Diagram

### 6.3.4 Peripherals Clock

The peripherals clock has different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSEL1 and CLK_CLKSEL2 register description in 6.3.8.

### 6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

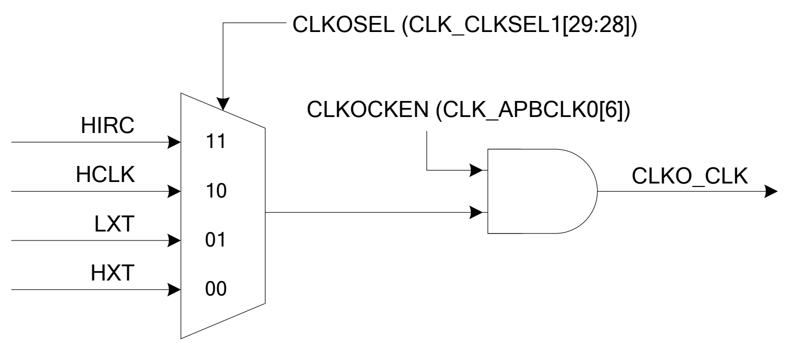
- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

### 6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where $F_{in}$ is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$**,** where $F_{in}$ is the input clock frequency, $F_{out}$ is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.




**Note:** Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-6 Clock Source of Clock Output

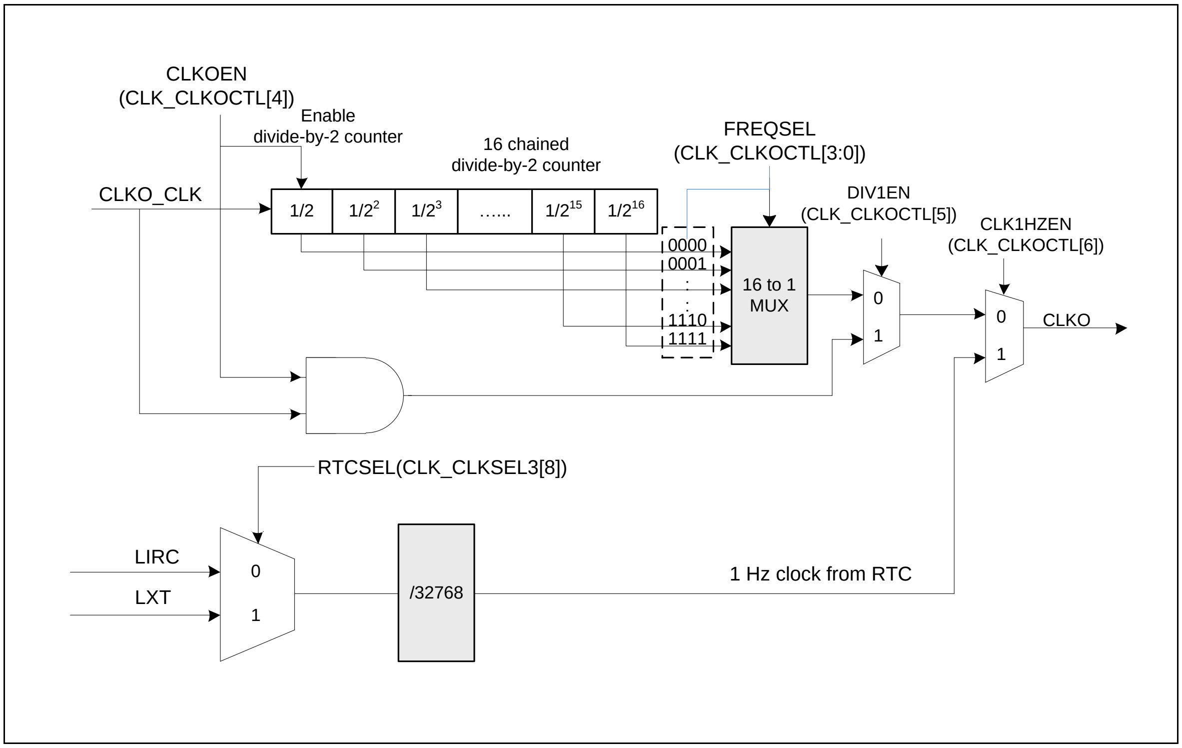



Figure 6.3-7 Clock Output Block Diagram

## 6.4 Flash Memeory Controller (FMC)

### 6.4.1 Overview

The M471M/M471R1/M471S series is equipped with 128/64 KB on-chip embedded Flash for application and configurable Data Flash to store some application dependent data. A User Configuration block is provided for system initiation. A 4 KB loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 4KB cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded Flash updated.

### 6.4.2 Features

- Supports 128/64 KB application ROM (APROM).
- Supports 4 KB loader ROM (LDROM).
- Supports Data Flash with configurable memory size.
- Supports 8 bytes User Configuration block to control system initiation.
- Supports 2 KB page erase for all embedded Flash.
- Supports 32-bit/64-bit and multi-word Flash programming function.
- Supports fast Flash programming verification function.
- Supports checksum calculation function.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.
- Supports cache memory to improve Flash access performance and reduce power consumption.

## 6.5 External Bus Interface (EBI)

### 6.5.1 Overview

The M471M/M471R1/M471S series is equipped with an external bus interface (EBI) for external device used. To save the connections between external device and the M471M/M471R1/M471S , the EBI operates in address bus and data bus multiplex mode. The EBI supports two chip selects that can connect two external devices with different timing setting requirement.

### 6.5.2 Features

- Supports address bus and data bus multiplex mode to save the address pins
- Supports two chip selects with polarity control for each bank
- Supports external accessible space up to 1 Mbytes (need 20-bit address width) for each bank. Real addressable space size is dependent on package pin out
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports 8-bit or 16-bit data width for each chip select
- Supports LCD interface i80 mode
- Supports variable address latch enable time (tALE)
- Supports variable data access time (tACC) and data access hold time (tAHD) for each chip select
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

## 6.6 General Purpose I/O (GPIO)

### 6.6.1 Overview

The M471M/M471R1/M471S series has up to 49 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 49 pins are arranged in 6 ports named as PA, PB, PC, PD, PE and PF. Each of the 49 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOIN (CONFIG0[10]). Each I/O pin has a very weakly individual pull-up resistor which is about 110 kΩ ~ 300 kΩ for $V_{DD}$ is from 5.0 V to 2.5 V.

### 6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOIN = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOIN = 1, all GPIO pins in input mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function
- Supports 5V-tolerance function for following pins
  - PA.0 ~ PA.3, PC.0 ~ PC.7, PD.2 ~ PD.3, PD.7, PD.12 ~ PD.15, PE.0, PE.8 ~ PE.13, PF.2, PF.5 ~ PF.7

## 6.7 PDMA Controller (PDMA)

### 6.7.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 8 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

### 6.7.2 Features

- Supports 8 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, ADC and PWM request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function for each channel

## 6.8 Timer Controller (TMR)

### 6.8.1 Overview

The Timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

### 6.8.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM and EADC function

## 6.9 PWM Generator and Capture Timer (PWM)

### 6.9.1 Overview

The M471M/M471R1/M471S series provides two PWM generators – PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM using comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for EADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various PWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

### 6.9.2 Features

#### *6.9.2.1 PWM function features*

- Supports maximum clock frequency up to144MHz
- Supports up to two PWM modules, each module provides 6 output channels.
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin

- Edge detect brake source to control brake state until brake interrupt cleared
- Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - PWM counter match zero, period value or compared value
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM counter match zero, period value or compared value
  - PWM counter match free trigger comparator compared value (only for EADC)

#### *6.9.2.2 Capture Function Features*

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

## 6.10 Watchdog Timer (WDT)

### 6.10.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

### 6.10.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval ($2^4$ ~ $2^{18}$) and the time-out interval is 1.6 ms ~ 26.214s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT.

## 6.11 Window Watchdog Timer (WWDT)

### 6.11.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

### 6.11.2 Features

- 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter

## 6.12 Real Time Clock (RTC)

### 6.12.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

The RTC controller also offers 80 bytes spare registers to store user's important information. The spare registers content is cleared when specified event on tamper pin is detected.

### 6.12.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register
- Supports Leap Year indication in RTC_LEAPYEAR register
- Supports Day of the Week counter in RTC_WEEKDAY register
- Frequency of RTC clock source compensate by RTC_FREQADJ register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated
- Supports 80 bytes spare registers and a snoop pin detection to clear the content of these spare registers

## 6.13 UART Interface Controller (UART)

### 6.13.1 Overview

The M471M/M471R1/M471S series provides four channels of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, RS-485 and auto-baud rate measuring function.

### 6.13.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS and RX data wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction

| UART Feature | UART0 / UART1 | UART2 / UART3 | SC_UART |
|---|---|---|---|
| FIFO | 16 Bytes | 16 Bytes | 4 Bytes |
| Auto Flow Control (CTS/RTS) | √ | √ | - |
| IrDA | √ | √ | - |
| RS-485 Function Mode | √ | √ | - |
| Auto-Flow Control | √ | √ | - |

| | | | |
|---|---|---|---|
| nCTS Wake-up | √ | √ | - |
| RX Data Wake-up | √ | √ | - |
| Auto-Baud Rate Measurement | √ | √ | - |
| STOP Bit Length | 1, 1.5, 2 bit | 1, 1.5, 2 bit | 1, 2 bit |
| Word Length 5, 6,7, 8 bits | √ | √ | √ |
| Even / Odd Parity | √ | √ | √ |
| Stick Bit | √ | √ | - |
| √= Supported | | | |

Table 6.13-1 NuMicro® M471M/M471R1/M471S Series UART Feature

## 6.14 Smart Card Host Interface (SC)

### 6.14.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/INTENC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

### 6.14.2 Features

- ISO-7816-3 T = 0, T = 1 compliant.
- EMV2000 compliant
- One ISO-7816-3 port
- Separates receive/transmit 4 byte entry FIFO for data payloads.
- Programmable transmission clock frequency.
- Programmable receiver buffer trigger level.
- Programmable guard time selection (11 ETU ~ 267 ETU).
- A 24-bit and two 8-bit timers for Answer to Request (ATR) and waiting times processing.
- Supports auto inverse convention function.
- Supports transmitter and receiver error retry and error number limiting function.
- Supports hardware activation sequence, hardware warm reset sequence and hardware
- deactivation sequence process.
- Supports hardware auto deactivation sequence when detected the card removal.
- Supports UART mode
  - Full duplex, asynchronous communications.
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads.
  - Supports programmable baud rate generator.
  - Supports programmable receiver buffer trigger level.
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SC_EGT[7:0]).
  - Programmable even, odd or no parity bit generation and detection.
  - Programmable stop bit, 1- or 2- stop bit generation

## 6.15 I²C Serial Interface Controller (I²C)

### 6.15.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controller which supports Bus Management (System Management (SM)/Power Management (PM) bus compatible) and Power-down wake-up function.

### 6.15.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition ( four slave address with mask option)
- Supports Bus Management (SM/PM compatible) function
- Supports Power-down wake-up function

## 6.16 Serial Peripheral Interface (SPI)

### 6.16.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The M471M/M471R1/M471S series contains up to three sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device.

SPI0 controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode.

### 6.16.2 Features

- Up to two sets of SPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode for SPI0
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 4-/8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface

## 6.17 USB Device Controller (USBD)

### 6.17.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports Control/Bulk/Interrupt/ Isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 8 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of "Endpoint Control" is also used to manage the data sequential synchronization, endpoint state, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate this USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

### 6.17.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer types
- Supports suspend function when no bus activity existing for 3 ms
- Supports 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provides remote wake-up capability

## 6.18 USB 1.1 Host Controller (USBH)

### 6.18.1 Overview

This chip is equipped with a USB 1.1 Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

### 6.18.2 Features

- Supports Universal Serial Bus (USB) Specification Revision 1.1.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt and Isochronous transfers.
- Supports an integrated Root Hub.
- Supports a USB host port shared with USB device (OTG function).
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.

## 6.19 CRC Controller (CRC)

### 6.19.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with programmable polynomial settings.

### 6.19.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1’s complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

## 6.20 Enhanced 12-bit Analog-to-Digital Converter (EADC)

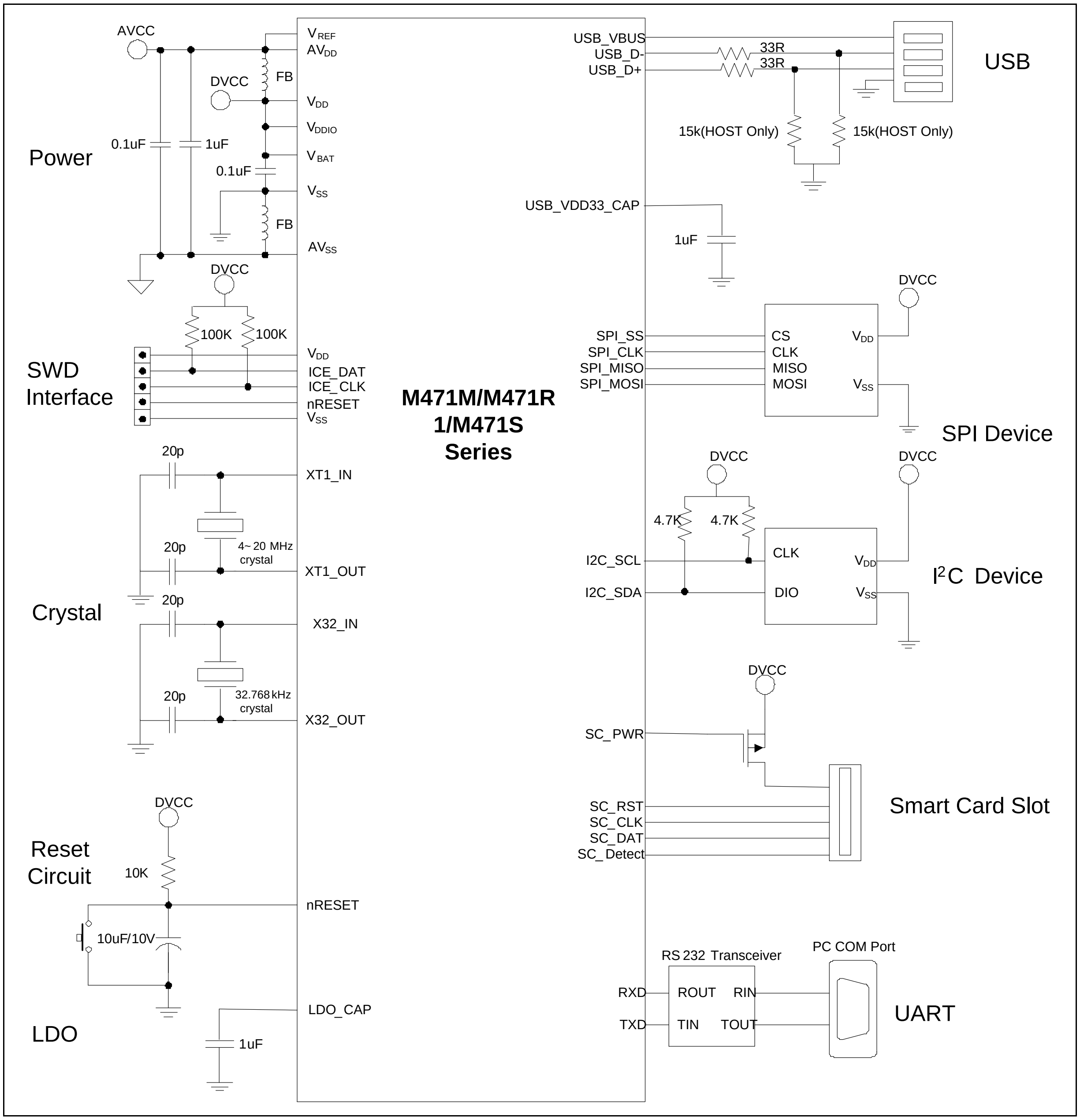
### 6.20.1 Overview

The M471M/M471R1/M471S series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 16 external input channels and 3 internal channels. The A/D converter can be started by software trigger, PWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (STADC) input signal.

### 6.20.2 Features

- Analog input voltage range: 0~$V_{REF}$ (Max to $AV_{DD}$).
- Reference voltage from $V_{REF}$ pin or $AV_{DD}$.
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels.
- 3 internal channels, they are band-gap voltage ($V_{BG}$), temperature sensor ($V_{TEMP}$), and Battery power ($V_{BAT}$)
- Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses.
- Maximum ADC clock frequency is 20 MHz.
- Up to 1 Msps conversion rate.
- Configurable ADC internal sampling time.
- Up to 19 sample modules
  - Each of sample module 0~15 which is configurable for ADC converter channel EADC_CH0~15 and trigger source.
  - Sample module 16~18 is fixed for ADC channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and battery power ($V_{BAT}$).
  - Double buffer for sample module 0~3
  - Configurable sampling time for each sample module.
  - Conversion results are held in 19 data registers with valid and overrun indicators.
- An A/D conversion can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18)
  - External pin STADC
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - PWM triggers
- Supports PDMA transfer

# 7 APPLICATION CIRCUIT




**Note 1:** It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

**Note 2:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

# 8 ELECTRICAL CHARACTERISTICS

## 8.1 Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD} - V_{SS}$ | DC Power Supply | -0.3 | +7.0 | V |
| $V_{IN}$ | Input Voltage | $V_{SS}$ - 0.3 | $V_{DD}$ + 0.3 | V |
| $1/t_{CLCL}$ | Oscillator Frequency | 4 | 20 | MHz |
| $T_A$ | Operating Temperature | -40 | +105 | ℃ |
| $T_{ST}$ | Storage Temperature | -55 | +150 | ℃ |
| $I_{DD}$ | Maximum Current into $V_{DD}$ | - | 120 | mA |
| $I_{SS}$ | Maximum Current out of $V_{SS}$ | | 120 | mA |
| $I_{IO}$ | Maximum Current sunk by a I/O pin | | 35 | mA |
| | Maximum Current sourced by a I/O pin | | 35 | mA |
| | Maximum Current sunk by total I/O pins | | 100 | mA |
| | Maximum Current sourced by total I/O pins | | 100 | mA |

**Note:** Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

## 8.2 DC Electrical Characteristics

($V_{DD}$ - $V_{SS}$ = 2.5 ~ 5.5 V, $T_A$ = 25°C)

| Parameter | Symbol | SPECIFICATION | | | | Test Conditions | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | | | | | |
| Operation voltage | $V_{DD}$ | 2.5 | - | 5.5 | V | $V_{DD}$ = 2.5 V ~ 5.5 V up to 72 MHz | | | | |
| Power supply for PE.8~PE.13 | $V_{DDIO}$ | 1.8 | - | 5.5 | V | | | | | |
| RTC Operation voltage for PF.0~PF.2 | $V_{BAT}$ | 2.5 | - | 5.5 | V | | | | | |
| Power Ground | $V_{SS}$ / $AV_{SS}$ | -0.3 | 0 | 0.3 | V | | | | | |
| LDO Output Voltage | $V_{LDO}$ | | 1.8 | | V | $V_{DD}$ ≥ 2.5 V | | | | |
| Band-gap Voltage | $V_{BG}$ | 1.175 | 1.21 | 1.225 | V | $V_{DD}$ = 2.5 V ~ 5.5 V, $T_A$ = 25°C | | | | |
| Allowed voltage difference for $V_{DD}$ and $AV_{DD}$ | $V_{DD}$-$AV_{DD}$ | -0.3 | 0 | 0.3 | V | | | | | |
| Operating Current Normal Run Mode HCLK = 72 MHz while(1){} executed from flash | | | | | | $V_{DD}$ | HXT | HIRC | PLL | All digital modules |
| | $I_{DD1}$ | - | 50 | - | mA | 5.5V | 12 MHz | X | V | V |
| | $I_{DD2}$ | - | 25 | - | mA | 5.5V | 12 MHz | X | V | X |
| | $I_{DD3}$ | - | 48 | - | mA | 3.3V | 12 MHz | X | V | V |
| | $I_{DD4}$ | - | 22 | - | mA | 3.3V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK = 50 MHz while(1){} executed from flash | $I_{DD5}$ | - | 43 | - | mA | 5.5V | 12 MHz | X | V | V |
| | $I_{DD6}$ | - | 25 | - | mA | 5.5V | 12 MHz | X | V | X |
| | $I_{DD7}$ | - | 41 | - | mA | 3.3V | 12 MHz | X | V | V |
| | $I_{DD8}$ | - | 22 | - | mA | 3.3V | 12 MHz | X | V | X |
| Operating Current Normal Run Mode HCLK =22.1184 MHz while(1){} executed from flash | $I_{DD9}$ | - | 17 | - | mA | 5.5V | X | V | X | V |
| | $I_{DD10}$ | - | 8 | - | mA | 5.5V | X | V | X | X |
| | $I_{DD11}$ | - | 17 | - | mA | 3.3V | X | V | X | V |
| | $I_{DD12}$ | - | 8 | - | mA | 3.3V | X | V | X | X |
| Operating Current Normal Run Mode HCLK = 12 MHz while(1){} executed from flash | $I_{DD13}$ | - | 10 | - | mA | 5.5V | 12 MHz | X | X | V |
| | $I_{DD14}$ | - | 6 | - | mA | 5.5V | 12 MHz | X | X | X |
| | $I_{DD15}$ | - | 8 | - | mA | 3.3V | 12 MHz | X | X | V |
| | $I_{DD16}$ | - | 4 | - | mA | 3.3V | 12 MHz | X | X | X |
| Operating Current | $I_{DD17}$ | - | 3 | - | mA | 5.5V | 12 MHz | X | X | V |

| Parameter | Symbol | SPECIFICATION | | | | Test Conditions | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | | | | | |
| Normal Run Mode<br>HCLK =4 MHz<br>while(1){}<br>executed from flash | $I_{DD18}$ | - | 2 | - | mA | 5.5V | 12 MHz | X | X | X |
| | $I_{DD19}$ | - | 3 | - | mA | 3.3V | 12 MHz | X | X | V |
| | $I_{DD20}$ | - | 2 | - | mA | 3.3V | 12 MHz | X | X | X |
| Operating Current<br>HCLK = 32.768 kHz<br>while(1){}<br>executed from flash | $I_{DD21}$ | - | 146 | - | uA | $V_{DD}$ | LXT (kHz) | HIRC | PLL | All digital modules |
| | | | | | | 5.5V | 32.768 | X | X | V |
| | $I_{DD22}$ | | 134 | | uA | 5.5V | 32.768 | X | X | X |
| | $I_{DD23}$ | | 133 | | uA | 3.3V | 32.768 | X | X | V |
| | $I_{DD24}$ | - | 121 | - | uA | 3.3V | 32.768 | X | X | X |
| Operating Current<br>Normal Run Mode<br>HCLK = 10 kHz<br>while(1){}<br>Executed from Flash | $I_{DD25}$ | - | 131 | - | μA | $V_{DD}$ | HXT /LXT | LIRC (kHz) | PLL | All digital modules |
| | | | | | | 5.5V | X | 10 | X | V |
| | $I_{DD26}$ | - | 128 | - | μA | 5.5V | X | 10 | X | X |
| | $I_{DD27}$ | - | 118 | - | μA | 3.3V | X | 10 | X | V |
| | $I_{DD28}$ | - | 115 | - | μA | 3.3V | X | 10 | X | X |
| Operating Current<br>Idle Mode<br>HCLK = 72 MHz | $I_{IDLE1}$ | - | 30 | - | mA | $V_{DD}$ | HXT | HIRC | PLL | All digital modules |
| | | | | | | 5.5V | 12 MHz | X | V | V |
| | $I_{IDLE2}$ | - | 10 | - | mA | 5.5V | 12 MHz | X | V | X |
| | $I_{IDLE3}$ | - | 28 | - | mA | 3.3V | 12 MHz | X | V | V |
| | $I_{IDLE4}$ | - | 7 | - | mA | 3.3V | 12 MHz | X | V | X |
| Operating Current<br>Idle Mode<br>HCLK = 50 MHz | $I_{IDLE5}$ | - | 32 | - | mA | 5.5V | 12 MHz | X | V | V |
| | $I_{IDLE6}$ | - | 10 | - | mA | 5.5V | 12 MHz | X | V | X |
| | $I_{IDLE7}$ | - | 29 | - | mA | 3.3V | 12 MHz | X | V | V |
| | $I_{IDLE8}$ | - | 8 | - | mA | 3.3V | 12 MHz | X | V | X |
| Operating Current<br>Idle Mode<br>HCLK =22.1184 MHz | $I_{IDLE9}$ | - | 11 | - | mA | 5.5V | X | V | X | V |
| | $I_{IDLE10}$ | - | 2 | - | mA | 5.5V | X | V | X | X |
| | $I_{IDLE11}$ | - | 10 | - | mA | 3.3V | X | V | X | V |
| | $I_{IDLE12}$ | - | 2 | - | mA | 3.3V | X | V | X | X |
| Operating Current<br>Idle Mode<br>HCLK =12 MHz | $I_{IDLE13}$ | - | 7 | - | mA | 5.5V | 12 MHz | X | X | V |
| | $I_{IDLE14}$ | | 3 | | mA | 5.5V | 12 MHz | X | X | X |
| | $I_{IDLE15}$ | - | 5 | - | mA | 3.3V | 12 MHz | X | X | V |
| | $I_{IDLE16}$ | - | 2 | - | mA | 3.3V | 12 MHz | X | X | X |

| Parameter | Symbol | SPECIFICATION | | | | Test Conditions | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | | | | | |
| Operating Current<br>Idle Mode<br>HCLK =4 MHz | $I_{IDLE17}$ | - | 2.2 | - | mA | 5.5V | 12 MHz | X | X | V |
| | $I_{IDLE18}$ | - | 1.1 | - | mA | 5.5V | 12 MHz | X | X | X |
| | $I_{IDLE19}$ | - | 1.8 | - | mA | 3.3V | 12 MHz | X | X | V |
| | $I_{IDLE20}$ | - | 0.6 | - | mA | 3.3V | 12 MHz | X | X | X |
| Operating Current<br>Idle Mode<br>32.768 kHz | $I_{IDLE21}$ | - | 136 | - | uA | $V_{DD}$ | LXT (kHz) | HIRC | PLL | All digital modules |
| | | | | | | 5.5V | 32.768 | X | X | V |
| | $I_{IDLE22}$ | - | 126 | - | uA | 5.5V | 32.768 | X | X | X |
| | $I_{IDLE23}$ | | 123 | | uA | 3.3V | 32.768 | X | X | V |
| | $I_{IDLE24}$ | | 114 | | uA | 3.3V | 32.768 | X | X | X |
| Operating Current<br>Idle Mode<br>at 10 kHz | $I_{IDLE25}$ | - | 128 | - | uA | $V_{DD}$ | HXT /LXT | LIRC (kHz) | PLL | All digital modules |
| | | | | | | 5.5V | X | 10 | X | V |
| | $I_{IDLE26}$ | - | 125 | - | µA | 5.5V | X | 10 | X | X |
| | $I_{IDLE27}$ | - | 115 | - | µA | 3.3V | X | 10 | X | V |
| | $I_{IDLE28}$ | - | 112 | - | µA | 3.3V | X | 10 | X | X |
| Standby Current<br>Power-down Mode<br>(Deep Sleep Mode) | $I_{PWD1}$ | | 21.08 | | µA | $V_{DD}$ | HXT/HIRC/PLL | LXT (kHz) | RTC | RAM retension |
| | | | | | | 5.5V | X | X | X | V |
| | $I_{PWD2}$ | | 22.18 | | µA | 5.5V | X | 10 | V | V |
| | $I_{PWD3}$ | | 23.21 | | µA | 5.5V | X | 32.768 | V | V |
| | $I_{PWD4}$ | | 23.23 | | µA | 5.5V | X | 10 & 32.768 | V | V |
| | $I_{PWD5}$ | | 19.38 | | µA | 3.3V | X | X | X | V |
| | $I_{PWD6}$ | | 20.44 | | µA | 3.3V | X | 10 | V | V |
| | $I_{PWD7}$ | | 21.50 | | µA | 3.3V | X | 32.768 | V | V |
| | $I_{PWD8}$ | | 21.55 | | µA | 3.3V | X | 10 & 32.768 | V | V |
| RTC Operating Current | $I_{VBAT}$ | | 2.01 | | uA | $V_{BAT}$ = 5.0 V, 32.768 kHz external low speed crystal oscillator (LXT), RTC ON and $V_{DD}/AV_{DD}$ power domain OFF. | | | | |
| | | | 1.91 | | uA | $V_{BAT}$ = 3.0 V, 32.768 kHz external low speed crystal oscillator (LXT), RTC ON and $V_{DD}/AV_{DD}$ power domain OFF. | | | | |
| Input Current at /RESET[1] | $I_{IN}$ | -55 | -45 | -30 | µA | $V_{DD}$ = 3.3V, $V_{IN}$ = 0.45V | | | | |

| Parameter | Symbol | SPECIFICATION | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| Logic 0 Input Current (Quasi-bidirectional mode) | $I_{IL}$ | - | -67 | -75 | μA | $V_{DD} = V_{DDIO} = V_{BAT}$ = 5.5 V, $V_{IN}$ = 0V |
| Logic 1 to 0 Transition Current (Quasi-bidirectional mode) [*3] | $I_{TL}$ | - | -610 | -650 | μA | $V_{DD} = V_{DDIO} = V_{BAT}$ =5.5 V, $V_{IN}$ = 2.0V |
| Input Leakage Current | $I_{LK}$ | -1 | - | +1 | μA | $V_{DD} = V_{DDIO} = V_{BAT}$ =5.5 V, 0 < $V_{IN}$ < $V_{DD}$<br>Open-drain or input only mode |
| Input Low Voltage (TTL input) | $V_{IL1}$ | -0.3 | - | 0.8 | V | $V_{DD} = V_{DDIO} = V_{BAT}$ = 4.5 V |
| | | -0.3 | - | 0.6 | | $V_{DD} = V_{DDIO} = V_{BAT}$ = 2.5 V |
| Input Low Voltage (TTL input for PE8 ~ PE13) | $V_{IL2}$ | -0.3 | - | 0.3 | V | $V_{DD} = V_{BAT}$ = 2.5 ~ 5.5 V<br>$V_{DDIO}$ = 1.8 V |
| Input High Voltage (TTL input) | $V_{IH1}$ | 2.0 | - | $V_{DD}$ + 0.3 | V | $V_{DD} = V_{DDIO} = V_{BAT}$ = 5.5 V |
| | | 1.5 | - | $V_{DD}$ + 0.3 | | $V_{DD} = V_{DDIO} = V_{BAT}$ = 3.0 V |
| Input High Voltage (TTL input for PE8 ~ PE13) | $V_{IH2}$ | 1.0 | - | $V_{DDIO}$ + 0.3 | V | $V_{DD} = V_{BAT}$ = 2.5 ~ 5.5 V<br>$V_{DDIO}$ = 1.8 V |
| Hysteresis voltage of PA, PB, PC, PD,PE, PF (Schmitt input) | $V_{HY}$ | | 0.2$V_{DD}$ | | V | |
| Input Low Voltage XT1[*2] | $V_{IL3}$ | 0 | - | 0.8 | V | $V_{DD}$ = 4.5 V |
| | | 0 | - | 0.4 | | $V_{DD}$ = 2.5 V |
| Input High Voltage XT1[*2] | $V_{IH3}$ | 3.5 | - | $V_{DD}$ + 0.3 | V | $V_{DD}$ = 5.5 V |
| | | 2.4 | - | $V_{DD}$ + 0.3 | | $V_{DD}$ = 3.0 V |
| X32 Output Pin | $V_{XOUT}$ | 0.6 | | 0.9 | V | |
| Input Low Voltage X32I[*4] | $V_{IL4}$ | 0 | - | $V_{XOUT}$ - 0.3 | V | |
| Input High Voltage X32I[*4] | $V_{IH4}$ | $V_{XOUT}$ +0.3 | | 1.8 | V | |
| Negative going threshold (Schmitt input), nRST | $V_{IL5}$ | -0.3 | - | 0.2 $V_{DD}$ | V | |
| Positive going threshold (Schmitt input), nRST | $V_{IH5}$ | 0.7 $V_{DD}$ | - | $V_{DD}$ + 0.3 | V | |
| Internal nRESET pin pull up resistor | $R_{RST}$ | 40 | | 150 | kΩ | |

| Parameter | Symbol | SPECIFICATION | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| Input Low Voltage (Schmitt input) | $V_{IL6}$ | -0.3 | - | 0.3 $V_{DD}$ | V | $V_{DD} = V_{DDIO} = V_{BAT} = 2.5 \sim 5.5$ V |
| Input Low Voltage (Schmitt input for PE8~ PE13) | $V_{IL7}$ | -0.3 | - | 0.3 $V_{DDIO}$ | V | $V_{DDIO} = 1.8$ V ~ 5.5V |
| Input High Voltage (Schmitt input) | $V_{IH6}$ | 0.7 $V_{DD}$ | - | $V_{DD}$ + 0.3 | V | $V_{DD} = V_{DDIO} = V_{BAT} = 2.5 \sim 5.5$ V |
| Input High Voltage (Schmitt input for PE8~ PE13) | $V_{IH7}$ | 0.7 $V_{DDIO}$ | - | $V_{DDIO}$ + 0.3 | V | $V_{DDIO} = 1.8$ V ~ 5.5V |
| Source Current (Quasi-bidirectional Mode) | $I_{SR11}$ | -300 | -400 | - | µA | $V_{DD} = V_{DDIO} = V_{BAT} = 4.5$ V, $V_S = 2.4$ V |
| | $I_{SR12}$ | -50 | -80 | - | µA | $V_{DD} = V_{DDIO} = V_{BAT} = 2.7$ V, $V_S = 2.2$ V |
| | $I_{SR13}$ | -40 | -73 | - | µA | $V_{DD} = V_{DDIO} = V_{BAT} = 2.5$ V, $V_S = 2.0$ V |
| Source Current (Quasi-bidirectional Mode for PE8~ PE13) | $I_{SR14}$ | -11 | -19 | | µA | $V_{DD} = V_{BAT} = 2.5 \sim 5.5$ V<br>$V_{DDIO} = 1.8$ V, $V_S = 1.6$ V |
| Source Current (Push-pull Mode) | $I_{SR21}$ | -20 | -26 | - | mA | $V_{DD} = V_{DDIO} = V_{BAT} = 4.5$ V, $V_S = 2.4$ V |
| | $I_{SR22}$ | -3 | -5.2 | - | mA | $V_{DD} = V_{DDIO} = V_{BAT} = 2.7$ V, $V_S = 2.2$ V |
| | $I_{SR23}$ | -2.5 | -5 | - | mA | $V_{DD} = V_{DDIO} = V_{BAT} = 2.5$ V, $V_S = 2.0$ V |
| Source Current<br>(Set IO as Push-pull Mode and basic driving strength<br>Only for PE8~PE13) | $I_{SR24}$ | -1 | -1.5 | | mA | $V_{DD} = V_{BAT} = 2.5 \sim 5.5$ V<br>$V_{DDIO} = 1.8$ V, $V_S = 1.6$ V |
| Source Current<br>(Set IO as Push-pull Mode and high driving strength<br>Only for PE8~PE13) | $I_{SR31}$ | -28 | -47 | - | mA | $V_{DD} = V_{BAT} = 2.5 \sim 5.5$ V<br>$V_{DDIO} = 4.5$ V, $V_S = 2.4$ V |
| | $I_{SR32}$ | -5.3 | -8.8 | - | mA | $V_{DD} = V_{BAT} = 2.5 \sim 5.5$ V<br>$V_{DDIO} = 2.7$ V, $V_S = 2.2$ V |
| | $I_{SR33}$ | -4.9 | -8.1 | - | mA | $V_{DD} = V_{BAT} = 2.5 \sim 5.5$ V<br>$V_{DDIO} = 2.5$ V, $V_S = 2.0$ V |
| | $I_{SR34}$ | -1.5 | -2.5 | | mA | $V_{DD} = V_{BAT} = 2.5 \sim 5.5$ V<br>$V_{DDIO} = 1.8$ V, $V_S = 1.6$ V |
| Sink Current (Quasi-bidirectional, Open-Drain and Push-pull Mode) | $I_{SK11}$ | 10 | 17 | - | mA | $V_{DD} = V_{DDIO} = V_{BAT} = 4.5$ V, $V_S = 0.45$ V |
| | $I_{SK12}$ | 6 | 11 | - | mA | $V_{DD} = V_{DDIO} = V_{BAT} = 2.7$ V, $V_S = 0.45$ V |
| | $I_{SK13}$ | 5 | 10 | - | mA | $V_{DD} = V_{DDIO} = V_{BAT} = 2.5$ V, $V_S = 0.45$ V |
| Sink Current<br>(Only for PE8~PE13) | $I_{SK14}$ | 3.6 | 6 | | mA | $V_{DD} = V_{BAT} = 2.5 \sim 5.5$ V<br>$V_{DDIO} = 1.8$ V, $V_S = 0.45$ V |

| Parameter | Symbol | SPECIFICATION | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| Sink Current (Set IO as high driving strength Only for PE8~PE13) | $I_{SK21}$ | 14.7 | 24.5 | | mA | $V_{DD} = V_{BAT}$ = 2.5 ~ 5.5 V<br>$V_{DDIO}$ = 4.5 V, $V_S$ = 0.45 V |
| | $I_{SK22}$ | 9.2 | 15.3 | | mA | $V_{DD} = V_{BAT}$ = 2.5 ~ 5.5 V<br>$V_{DDIO}$ = 2.7 V, $V_S$ = 0.45 V |
| | $I_{SK23}$ | 8.5 | 14.1 | | mA | $V_{DD} = V_{BAT}$ = 2.5 ~ 5.5 V<br>$V_{DDIO}$ = 2.5 V, $V_S$ = 0.45 V |
| | $I_{SK24}$ | 5.4 | 9 | | mA | $V_{DD} = V_{BAT}$ = 2.5 ~ 5.5 V<br>$V_{DDIO}$ = 1.8 V, $V_S$ = 0.45 V |

**Notes:**

1. nRESET pin is a Schmitt trigger input.
2. XT1_IN is a CMOS input.
3. All pins can source a transition current when they are being externally driven from 1 to 0. In the condition of $V_{DD}$=5.5V, the transition current reaches its maximum value when $V_{IN}$ approximates to 2V.
4. If X32I is as external clock input, the input high voltage should be lower than 1.8V to avoid chip damage.

### 8.2.1 On-chip peripheral current consumption

- ALL GPIO pins are in push pull mode, output high.
- LDO = 1.8V
- The typical values for TA= 25 ˚C and $V_{DD} = AV_{DD}$ = 3.3 V unless otherwise specified.
- When the peripherals are enabled HCLK is the system clock, $f_{HCLK}$ = 72 MHz, $f_{PCLK0, 1} = f_{HCLK}/2$.

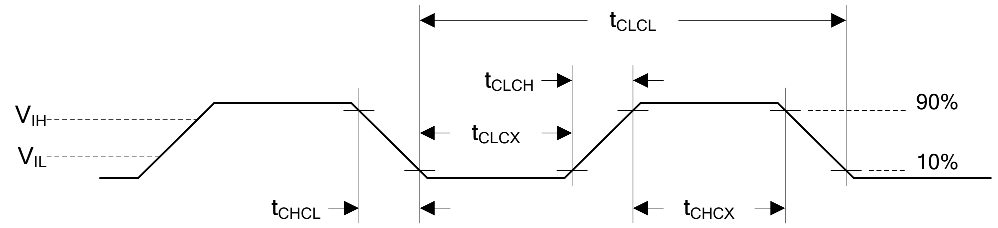
| Peripheral | $I_{DD}$ | Unit |
|---|---|---|
| PDMA0 ON | 1.026 | uA |
| ISP ON | 0.000 | |
| EBI ON | 0.343 | |
| USBH ON | 1.488 | |
| CRC ON | 0.220 | |
| FMC ON | 0.745 | |
| WDT ON | 0.433 | |
| RTC ON | 0.417 | |
| TMR0 ON | 0.568 | |
| TMR1 ON | 0.578 | |
| TMR2 ON | 0.486 | |
| TMR3 ON | 0.507 | |
| CLKO ON | 0.086 | |
| I2C0 ON | 0.428 | |
| I2C1 ON | 0.357 | |
| SPI0 ON | 1.154 | |
| SPI1 ON | 0.924 | |
| UART0 ON | 1.556 | |
| UART1 ON | 1.527 | |
| UART2 ON | 1.634 | |
| UART3 ON | 1.549 | |
| USBDC ON | 1.634 | |
| EADC ON | 0.964 | |

| | | |
|---|---|---|
| SC0 ON | 1.243 | |
| PWM0 ON | 1.850 | |
| PWM1 ON | 1.640 | |

**Note:** Guaranteed by characterization results, not tested in production

## 8.3 AC Electrical Characteristics

### 8.3.1 External 4~20 MHz High Speed Crystal (HXT) Input Clock




| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{CHCX}$ | Clock High Time | 10 | - | - | ns | - |
| $t_{CLCX}$ | Clock Low Time | 10 | - | - | ns | - |
| $t_{CLCH}$ | Clock Rise Time | 2 | - | 15 | ns | - |
| $t_{CHCL}$ | Clock Fall Time | 2 | - | 15 | ns | - |
| $V_{IH}$ | Input High Voltage | $0.7V_{DD}$ | | $V_{DD}$ | V | - |
| $V_{IL}$ | Input Low Voltage | 0 | | $0.3V_{DD}$ | V | - |

### 8.3.2 External 4~20 MHz High Speed Crystal (HXT) Oscillator

| Symbol | Parameter | Min. | Typ. | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{HXT}$ | Operation Voltage | 2.5 | - | 5.5 | V | - |
| $T_A$ | Temperature | -40 | - | 105 | ℃ | - |
| $I_{HXT}$ | Operating Current | - | 2 | - | mA | 12 MHz, $V_{DD}$ = 5.5V |
| | | - | 0.8 | - | mA | 12 MHz, $V_{DD}$ = 3.3V |
| $f_{HXT}$ | Clock Frequency | 4 | - | 20 | MHz | - |

#### *8.3.2.1 Typical Crystal Application Circuits*

| Crystal | C1 | C2 |
|---|---|---|
| 4 MHz ~ 20 MHz | 10~20 pF | 10~20 pF |

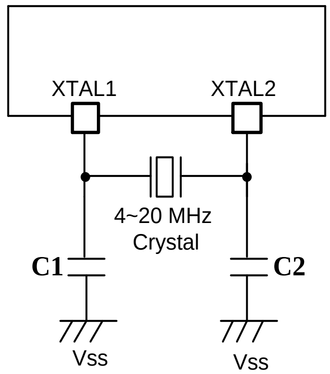
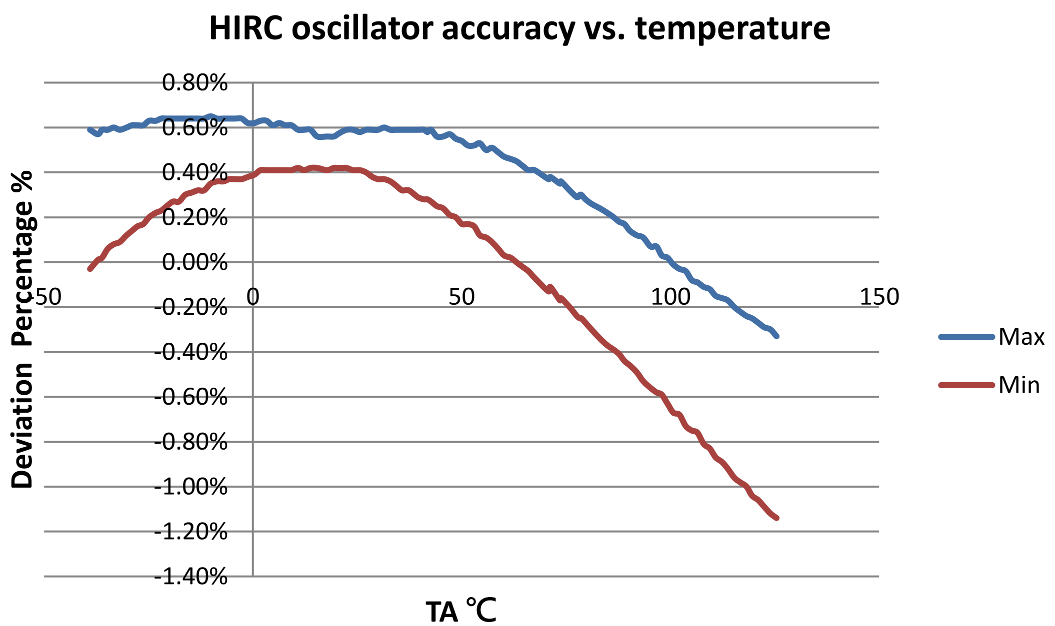



Figure 8.3-1 Typical Crystal Application Circuit

### 8.3.3 22.1184 MHz Internal High Speed RC Oscillator (HIRC)

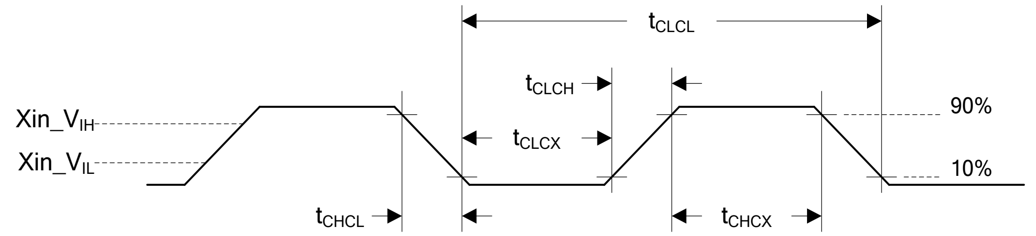
| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{HRC}$ | Supply Voltage | 1.62 | 1.8 | 1.98 | V | - |
| $f_{HRC}$ | Center Frequency | - | 22.1184 | | MHz | - |
| | Calibrated Internal Oscillator Frequency | -1 | - | +1 | % | $T_A$ = 25 ℃, $V_{DD}$ = 5 V |
| | | -2 | - | +2 | % | $T_A$ = -40 ℃ ~ 105 ℃<br>$V_{DD}$ = 2.5 V ~ 5 .5 V |
| $I_{HRC}$ | Operating Current | - | 790 | - | μA | $T_A$ = 25 ℃, $V_{DD}$ = 5 V |
| $T_S$ | Stable time | | | 20 | us | |




**Note:** Number of test samples: 10.

Figure 8.3-2 HIRC Accuracy vs. Temperature

### 8.3.4 32.768 kHz External Low Speed Crystal (LXT) Input Clock




*Note: Duty cycle is 50%.*

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{CHCX}$ | Clock High Time | TBD | - | - | ns | - |
| $t_{CLCX}$ | Clock Low Time | TBD | - | - | ns | - |
| $t_{CLCH}$ | Clock Rise Time | TBD | - | TBD | ns | - |
| $t_{CHCL}$ | Clock Fall Time | TBD | - | TBD | ns | - |
| Xin_$V_{IH}$ | LXT Input Pin Input High Voltage | Xout+0.3 | | 1.8 | V | - |
| Xin_$V_{IL}$ | LXT Input Pin Input Low Voltage | 0 | | Xout-0.3 | V | - |
| Xout | LXT Output Pin | 0.6 | | 0.9 | V | |

### 8.3.5 32.768 kHz External Low Speed Crystal (LXT) Oscillator

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operation Voltage $V_{BAT}$ | - | 2.5 | - | 5.5 | V |
| Operation Temperature | - | -40 | - | 105 | ℃ |
| Operation Current | 32.768KHz at $V_{BAT}$=5V | | 1.6 | | µA |
| Clock Frequency | External crystal | - | 32.768 | - | kHz |

#### *8.3.5.1 LXT Typical Crystal Application Circuits*

| CRYSTAL | $C_1$ | $C_2$ |
|---|---|---|
| 32.768 kHz | 10~20 pF | 10~20 pF |

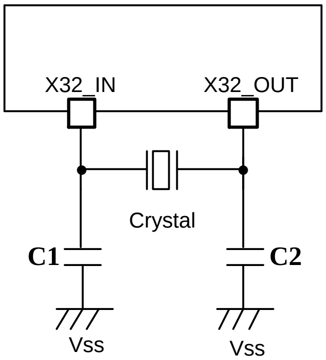



Figure 8.3-3 Typical Crystal Application Circuit

### 8.3.6 10 kHz Internal Low Speed RC Oscillator (LIRC)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{LRC}$ | Supply Voltage | 2.5 | - | 5.5 | V | - |
| $f_{LRC}$ | Center Frequency | - | 10 | - | kHz | - |
| | Oscillator Frequency | -30 | - | +30 | % | $V_{DD}$ = 2.5 V ~ 5.5 V<br>$T_A$ = 25℃ |
| | | -50 | - | +50 | % | $V_{DD}$ = 2.5 V ~ 5.5 V<br>$T_A$ = -40℃ ~ +105℃ |

## 8.4 Analog Characteristics

### 8.4.1 PIN AC characteristics

- $C_L$ = 51 pF

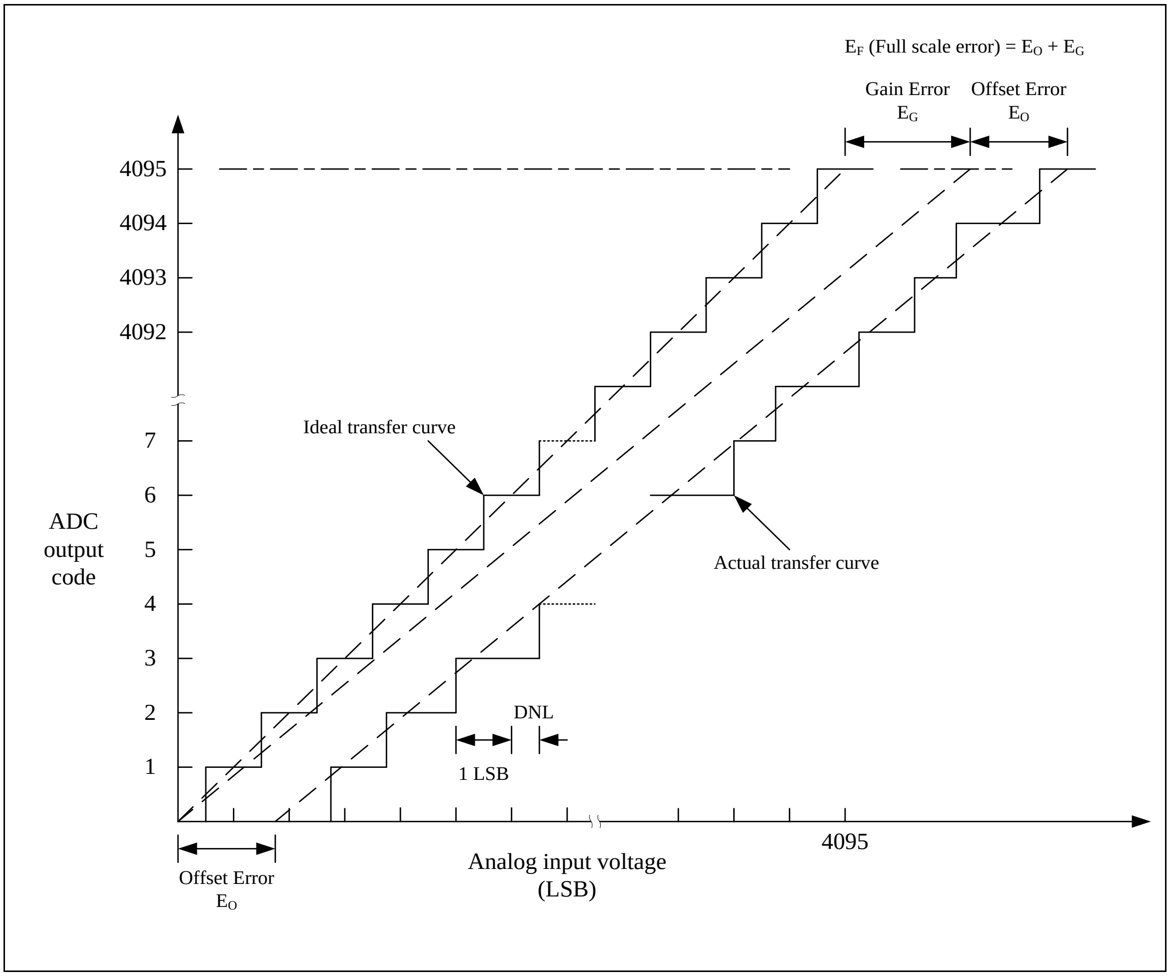
| Px_SLEWCTL | Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|---|
| Basic Slew Rate | $t_{f(IO)out}$ | Output high to low level fall time (90~10%) | $V_{DD}$ = 5.5 V | 6.87 | ns |
| | | | $V_{DD}$ = 3.3 V | 10.31 | |
| | $t_{r(IO)out}$ | output low to high level rise time (10~90%) | $V_{DD}$ = 5.5 V | 6.6 | |
| | | | $V_{DD}$ = 3.3 V | 10.4 | |
| Higher Slew Rate | $t_{f(IO)out}$ | Output high to low level fall time (90~10%) | $V_{DD}$ = 5.5 V | 4.67 | |
| | | | $V_{DD}$ = 3.3 V | 6.82 | |
| | $t_{r(IO)out}$ | output low to high level rise time (10~90%) | $V_{DD}$ = 5.5 V | 5.66 | |
| | | | $V_{DD}$ = 3.3 V | 8.46 | |

### 8.4.2 12-bit SAR ADC

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| - | Resolution | | 12 | | Bit | - |
| DNL | Differential Nonlinearity Error | - | - | ±2 | LSB | - |
| INL | Integral Nonlinearity Error | - | - | ±2 | LSB | - |
| $E_O$ | Offset Error | - | 3 | - | LSB | - |
| $E_G$ | Gain Error (Transfer Gain) | - | -3 | - | LSB | - |
| $E_A$ | Absolute Error | - | 4 | - | LSB | - |
| - | Monotonic | | Guaranteed | | - | - |
| $F_{ADC}$ | ADC Clock Frequency | - | - | 21 | MHz | $AV_{DD}$ = 4.5~5.5 V |
| | | - | - | 8.4 | | $AV_{DD}$ = 2.5~5.5 V |
| $F_S$ | Sample Rate ($F_{ADC}/T_{CONV}$) | - | - | 1000 | kSPS | $AV_{DD}$ = 4.5~5.5 V<br>$T_{CONV}$ = 21 clock<br>$F_{ADC}$ = 21 Mhz |
| | | - | - | 400 | kSPS | $AV_{DD}$ = 2.5~5.5 V<br>$T_{CONV}$ = 21 clock<br>$F_{ADC}$ = 8.4 Mhz |
| $T_{ACQ}$ | Acquisition Time (Sample Stage) | | 2~9 | | $1/F_{ADC}$ | Default: 6 ($1/F_{ADC}$)<br>EADC_SCTLx[31:24]=0 |
| $T_{CONV}$ | Total Conversion Time | | 16~23 | | $1/F_{ADC}$ | TCONV = TACQ+ 15<br>Default: 21 ($1/F_{ADC}$)<br>EADC_SCTLx[31:24]=0 |
| $AV_{DD}$[#1] | Supply Voltage | 2.5 | - | 5.5 | V | - |
| $I_{DDA}$[#1] | Supply Current (Avg.) | - | 2.8 | - | mA | $AV_{DD}$ = 5 V |
| $V_{IN}$[#1] | Analog Input Voltage | 0 | - | $V_{REF}$ | V | - |
| $V_{REF}$ | Reference Voltage | 2.5 | - | $AV_{DD}$ | V | $AV_{DD}$ = 5 V |
| $C_{IN}$[#1] | Input Capacitance | - | 6 | - | pF | - |
| $R_{IN}$[#1] | Input Load | - | 6.5 | - | kΩ | - |

**Note:**

**#1:** Design by guarantee, no test in production.




**Note:** The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

**Typical connection diagram using the ADC**

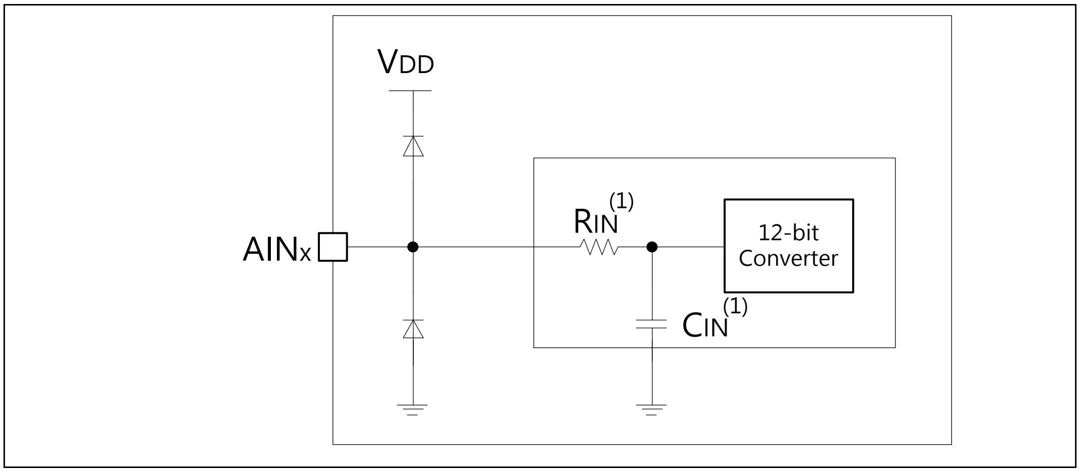



Figure 8.4-1 Typical connection diagram using the ADC

(1) Refer to ADC spec for the values of $R_{IN}$, $C_{IN}$

### 8.4.3 LDO

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{DD}$ | DC Power Supply | 2.5 | - | 5.5 | V | - |
| $V_{LDO}$ | Output Voltage | | 1.8 | | V | - |
| $T_A$ | Temperature | -40 | 25 | 105 | ℃ | |

**Notes:**

1. It is recommended a 0.1μF bypass capacitor is connected between $V_{DD}$ and the closest $V_{SS}$ pin of the device.
2. For ensuring power stability, a 1μF Capacitor must be connected between LDO_CAP pin and the closest $V_{SS}$ pin of the device.

### 8.4.4 Low Voltage Reset

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Supply Voltage | 0 | - | 5.5 | V | - |
| $T_A$ | Temperature | -40 | 25 | 105 | ℃ | - |
| $I_{LVR}$ | Quiescent Current | - | 1 | 5 | μA | $AV_{DD}$ = 5.5 V |
| $V_{LVR}$ | Threshold Voltage | 2.00 | 2.20 | 2.45 | V | $T_A$ = 105 ℃ |
| | | 1.90 | 2.00 | 2.10 | V | $T_A$ = 25 ℃ |
| | | 1.70 | 1.90 | 2.10 | V | $T_A$ = -40 ℃ |

### 8.4.5 Brown-out Detector

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Supply Voltage | 0 | - | 5.5 | V | - |
| $T_A$ | Temperature | -40 | 25 | 105 | ℃ | - |
| $I_{BOD}$ | Quiescent Current | - | - | 140 | μA | $AV_{DD}$ = 5.5 V |
| $V_{BOD}$ | Brown-out Voltage (Falling edge) | 4.2 | 4.4 | 4.6 | V | BOV_VL [1:0] = 11 |
| | | 3.5 | 3.7 | 3.9 | V | BOV_VL [1:0] = 10 |
| | | 2.55 | 2.7 | 2.85 | V | BOV_VL [1:0] = 01 |
| | | 2.05 | 2.2 | 2.35 | V | BOV_VL [1:0] = 00 |
| $V_{BOD}$ | Brown-out Voltage (Rising edge) | 4.3 | 4.5 | 4.7 | V | BOV_VL [1:0] = 11 |
| | | 3.6 | 3.8 | 4.0 | V | BOV_VL [1:0] = 10 |
| | | 2.6 | 2.75 | 2.9 | V | BOV_VL [1:0] = 01 |
| | | 2.1 | 2.25 | 2.4 | V | BOV_VL [1:0] = 00 |

### 8.4.6 Power-on Reset

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | 25 | 105 | ℃ | - |
| $V_{POR}$ | Reset Voltage | 1.6 | 2 | 2.4 | V | - |
| $V_{POR}$ | VDD Start Voltage to Ensure Power-on Reset | - | - | 100 | mV | |
| $RR_{VDD}$ | VDD Raising Rate to Ensure Power-on Reset | 0.025 | - | - | V/ms | |
| $t_{POR}$ | Minimum Time for VDD Stays at VPOR to Ensure Power-on Reset | 0.5 | - | - | ms | |

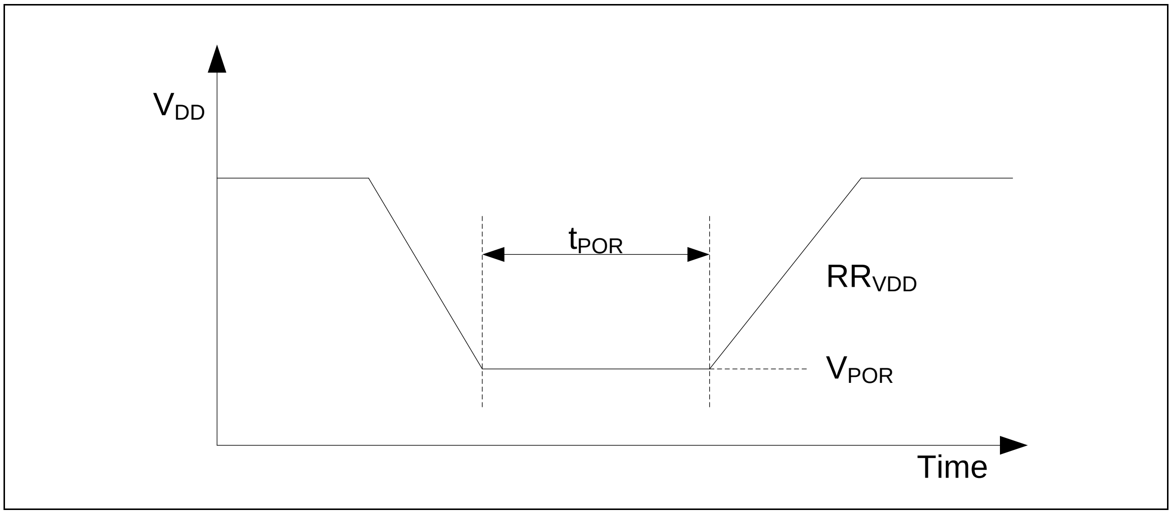


Figure 8.4-2 Power-up Ramp Condition

### 8.4.7 Temperature Sensor

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | - | 105 | ℃ | |
| $I_{TEMP}$ | Current Consumption | - | 16 | - | μA | |
| - | Gain | -1.55 | -1.672 | -1.75 | mV/℃ | |
| - | Offset | 735 | 748 | 755 | mV | $T_A$ = 0 ℃ |

**Note:**

1. The temperature sensor formula for the output voltage (Vtemp) is as below equation.
2. Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)

### 8.4.8 Internal Voltage Reference

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{VREF}$ | $AV_{DD}$ | 2.5 | | 5.5 | V | - |
| $V_{ref1}$ | Vref(2.56V) | 2.483 | 2.560 | 2.637 | V | $AV_{DD}$ >= 2.9V |
| $V_{ref2}$ | Vref(2.048V) | 1.986 | 2.048 | 2.109 | V | $AV_{DD}$ >= 2.5V |
| $V_{ref3}$ | Vref(3.072V) | 2.98 | 3.072 | 3.164 | V | $AV_{DD}$ >= 3.4V |
| $V_{ref4}$ | Vref(4.096V) | 3.973 | 4.096 | 4.219 | V | $AV_{DD}$ >= 4.5V |

### 8.4.9 USB PHY

#### *8.4.9.1 Low-full-Speed DC Electrical Specifications*

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High (driven) | 2.0 | - | | V | - |
| $V_{IL}$ | Input Low | - | - | 0.8 | V | - |
| $V_{DI}$ | Differential Input Sensitivity | 0.2 | - | | V | \|PADP-PADM\| |
| $V_{CM}$ | Differential Common-mode Range | 0.8 | - | 2.5 | V | Includes $V_{DI}$ range |
| $V_{SE}$ | Single-ended Receiver Threshold | 0.8 | - | 2.0 | V | - |
| | Receiver Hysteresis | - | 200 | | mV | - |
| $V_{OL}$ | Output Low (driven) | 0 | - | 0.3 | V | - |
| $V_{OH}$ | Output High (driven) | 2.8 | - | 3.6 | V | - |
| $V_{CRS}$ | Output Signal Cross Voltage | 1.3 | - | 2.0 | V | - |
| $R_{PU}$ | Pull-up Resistor | 1.425 | - | 1.575 | kΩ | - |
| $Z_{DRV}$ | Driver Output Resistance | - | 10 | - | Ω | Steady state drive* |
| $C_{IN}$ | Transceiver Capacitance | - | - | 20 | pF | Pin to GND |

*Driver output resistance doesn't include series resistor resistance.

#### *8.4.9.2 USB Full-Speed Driver Electrical Characteristics*

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $T_{FR}$ | Rise Time | 4 | - | 20 | ns | $C_L$=50p |
| $T_{FF}$ | Fall Time | 4 | - | 20 | ns | $C_L$=50p |
| $T_{FRFF}$ | Rise and Fall Time Matching | 90 | - | 111.11 | % | $T_{FRFF}=T_{FR}/T_{FF}$ |

*8.4.9.3 USB LDO Specification*

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{BUS}$ | $V_{BUS}$ Pin Input Voltage | 4.0 | 5.0 | 5.5 | V | - |
| $V_{DD33}$ | LDO Output Voltage | - | 3.3 | - | V | - |
| $C_{bp}$ | External Bypass Capacitor | - | 1.0 | - | uF | - |

## 8.5 Flash DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $V_{FLA}$[2] | Supply Voltage | - | 1.8 | - | V | $T_A$ = 25℃ |
| $N_{ENDUR}$ | Endurance | 20,000 | - | - | cycles[1] | |
| $T_{RET}$ | Data Retention | 100 | - | - | year | |
| $T_{ERASE}$ | Page Erase Time | 20 | | - | ms | |
| $T_{PROG}$ | Program Time | 60 | | - | us | |
| $I_{DD1}$ | Read Current | - | - | 13.5 | mA | |
| $I_{DD2}$ | Program Current | - | 10 | - | mA | |
| $I_{DD3}$ | Erase Current | - | 12 | - | mA | |

**Notes:**

1. Number of program/erase cycles.
2. $V_{FLA}$ is source from chip LDO output voltage.

## 8.6 I²C Dynamic Characteristics

| Symbol | Parameter | Standard Mode[1][2] | | Fast Mode[1][2] | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{LOW}$ | SCL low period | 4.7 | - | 1.2 | - | uS |
| $t_{HIGH}$ | SCL high period | 4 | - | 0.6 | - | uS |
| $t_{SU; STA}$ | Repeated START condition setup time | 4.7 | - | 1.2 | - | uS |
| $t_{HD; STA}$ | START condition hold time | 4 | - | 0.6 | - | uS |
| $t_{SU; STO}$ | STOP condition setup time | 4 | - | 0.6 | - | uS |
| $t_{BUF}$ | Bus free time | 4.7[3] | - | 1.2[3] | - | uS |
| $t_{SU;DAT}$ | Data setup time | 250 | - | 100 | - | nS |
| $t_{HD;DAT}$ | Data hold time | 0[4] | 3.45[5] | 0[4] | 0.8[5] | uS |
| $t_r$ | SCL/SDA rise time | - | 1000 | 20+0.1Cb | 300 | nS |
| $t_f$ | SCL/SDA fall time | - | 300 | - | 300 | nS |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

**Notes:**

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

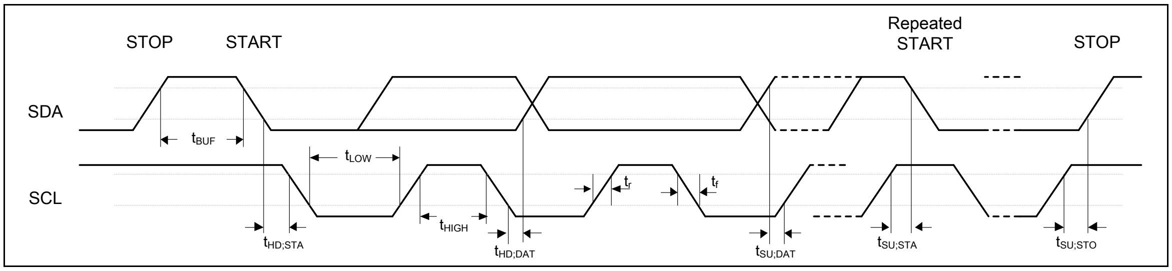



Figure 8.6-1 I²C Timing Diagram

## 8.7 SPI Dynamic Characteristics

### 8.7.1 Dynamic Characteristics of Data Input and Output Pin

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **SPI MASTER MODE (VDD = 4.5 V~5.5V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{W(SCKH)}$ $t_{W(SCKL)}$ | SPI high and low time, peripheral clock = 20MHz | 22.5 | - | 27.5 | ns |
| $t_{DS}$ | Data input setup time | 2 | - | - | ns |
| $t_{H(MI)}$ | Data input hold time | 4 | - | - | ns |
| $t_V$ | Data output valid time | - | - | 1 | ns |
| $t_{H(MO)}$ | Data output hold time | 0 | - | - | ns |
| **SPI MASTER MODE (VDD = 3.0~3.6 V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{W(SCKH)}$ $t_{W(SCKL)}$ | SPI high and low time, peripheral clock = 20MHz | 22.5 | - | 27.5 | ns |
| $t_{DS}$ | Data input setup time | 2 | | | ns |
| $t_{H(MI)}$ | Data input hold time | 4 | | | ns |
| $t_V$ | Data output valid time | | - | 1 | ns |
| $t_{H(MO)}$ | Data output hold time | 0 | - | - | ns |

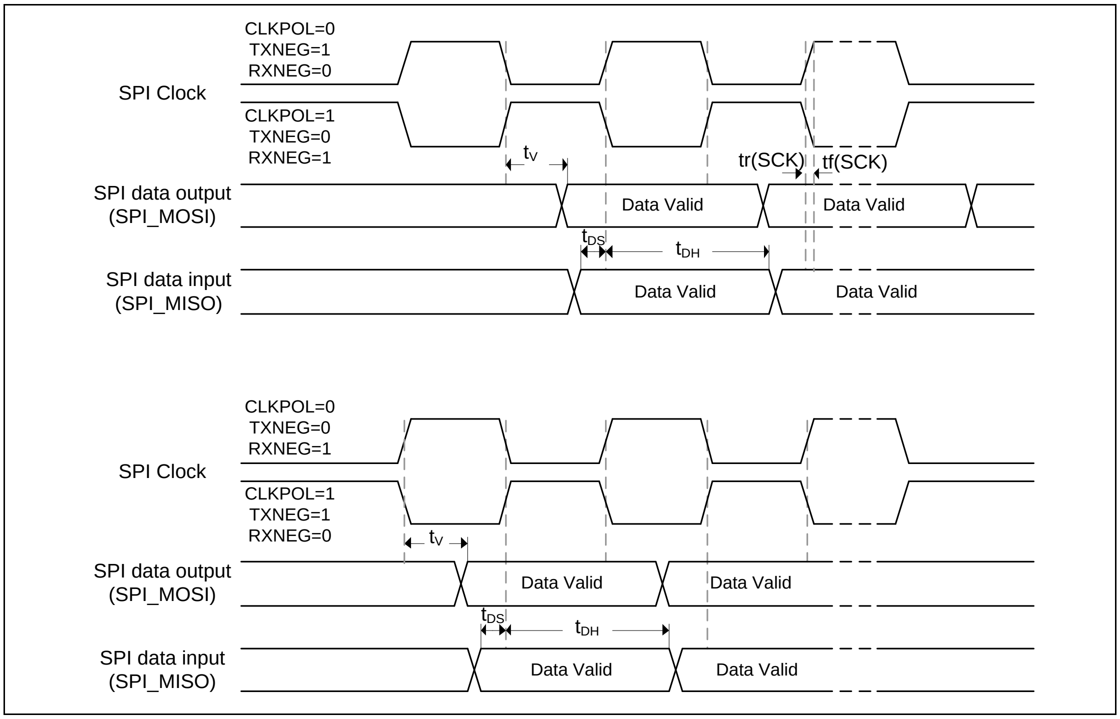



Figure 8.7-1 SPI Master Mode Timing Diagram

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **SPI SLAVE MODE (VDD = 4.5 V~5.5V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{SS}$ | Slave select setup time | 3 | - | - | Peripheral clock |
| $t_{SH}$ | Slave select hold time | 2 | - | - | Peripheral clock |
| $t_{DS}$ | Data input setup time | 2 | - | - | ns |
| $t_{H(SI)}$ | Data input hold time | 5.5 | - | - | ns |
| $t_{a(SO)}$ | Data output access time | - | - | 18 | ns |
| $t_V$ | Data output valid time | - | 18.5- | 24.5 | ns |
| $t_{H(SO)}$ | Data output hold time | 6 | - | - | ns |
| **SPI SLAVE MODE (VDD = 3.0 V ~ 3.6 V, 30 PF LOADING CAPACITOR)** | | | | | |
| $t_{SS}$ | Slave select setup time | 3 | - | - | Peripheral clock |
| $t_{SH}$ | Slave select hold time | 2 | - | - | Peripheral clock |
| $t_{DS}$ | Data input setup time | 2 | - | - | ns |
| $t_{H(SI)}$ | Data input hold time | 6 | - | - | ns |
| $t_{a(SO)}$ | Data output access time | - | - | 24 | ns |
| $t_V$ | Data output valid time | - | 23 | 30 | ns |
| $t_{H(SO)}$ | Data output hold time | 7 | - | - | ns |

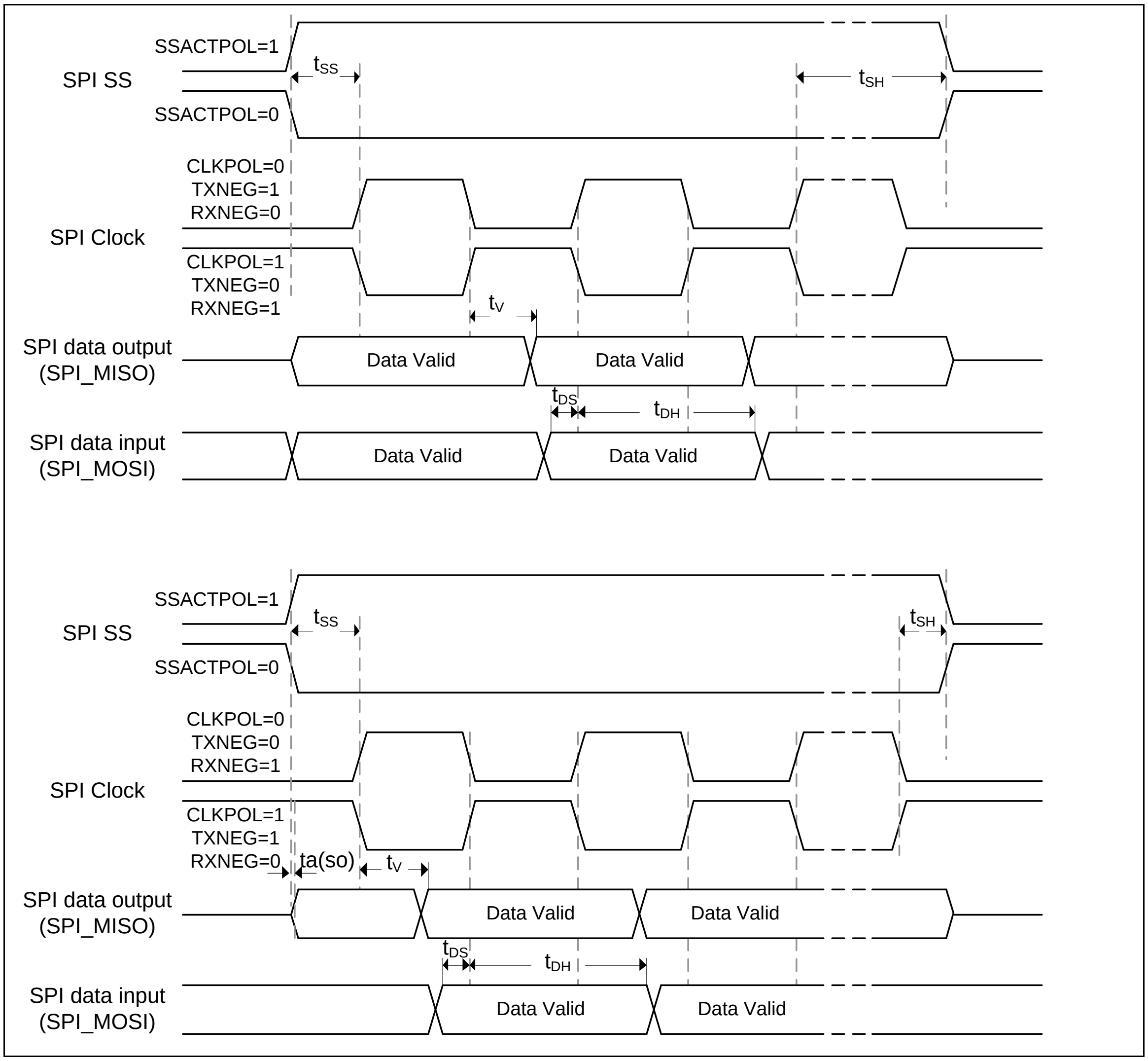
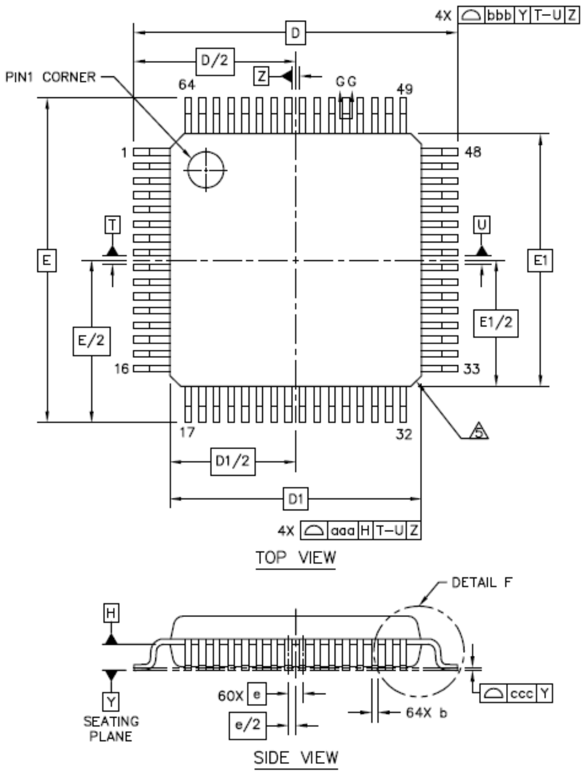


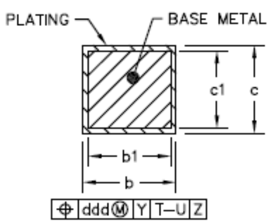

Figure 8.7-2 SPI Slave Mode Timing Diagram

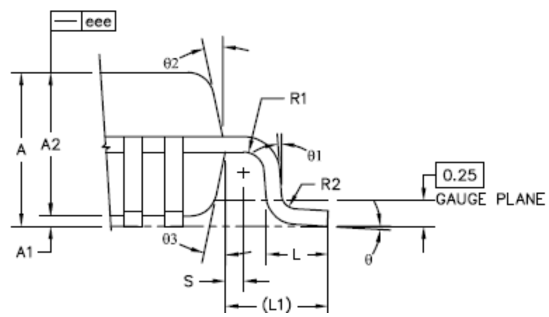
# 9 PACKAGE DIMENSIONS

## 9.1 LQFP 64L (7x7x1.4 mm, Footprint 2.0 mm)

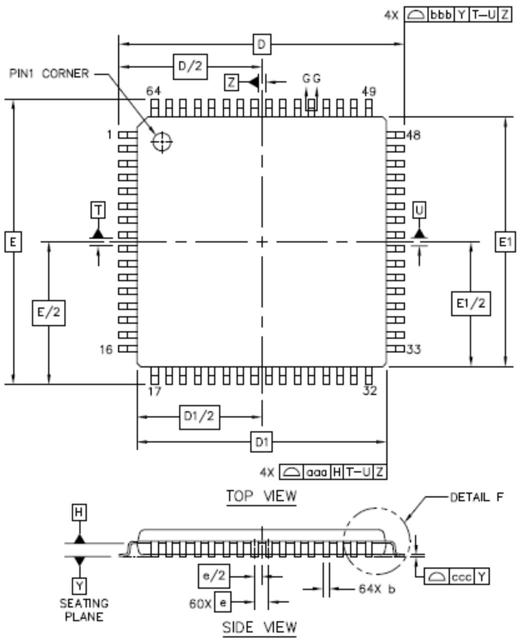



| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 1.6 |
| STAND OFF | | A1 | 0.05 | --- | 0.15 |
| MOLD THICKNESS | | A2 | 1.35 | 1.4 | 1.45 |
| LEAD WIDTH(PLATING) | | b | 0.13 | 0.18 | 0.23 |
| LEAD WIDTH | | b1 | 0.13 | 0.16 | 0.19 |
| L/F THICKNESS(PLATING) | | c | 0.09 | --- | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | --- | 0.16 |
| | X | D | 9 BSC | | |
| | Y | E | 9 BSC | | |
| BODY SIZE | X | D1 | 7 BSC | | |
| | Y | E1 | 7 BSC | | |
| LEAD PITCH | | e | 0.4 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| FOOTPRINT | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | --- | --- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | --- | --- |
| | | R2 | 0.08 | --- | 0.2 |
| | | S | 0.2 | --- | --- |
| PACKAGE EDGE TOLERANCE | | aaa | 0.2 | | |
| LEAD EDGE TOLERANCE | | bbb | 0.2 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.07 | | |
| MOLD FLATNESS | | eee | 0.05 | | |

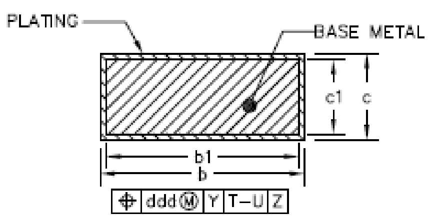


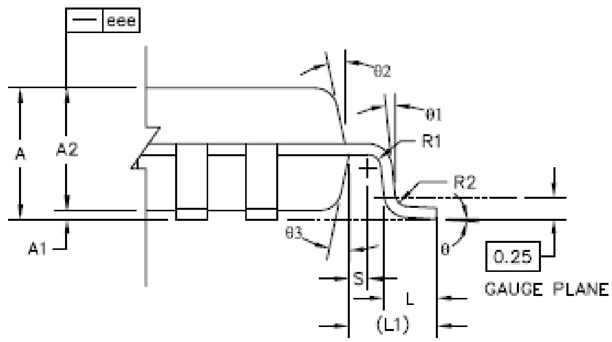
## 9.2 LQFP 64L (14x14x1.4mm, Footprint 2.0 mm)




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 1.6 |
| STAND OFF | | A1 | 0.05 | --- | 0.15 |
| MOLD THICKNESS | | A2 | 1.35 | 1.4 | 1.45 |
| LEAD WIDTH(PLATING) | | b | 0.3 | 0.35 | 0.45 |
| LEAD WIDTH | | b1 | 0.3 | --- | 0.41 |
| L/F THICKNESS(PLATING) | | c | 0.09 | --- | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | --- | 0.16 |
| | X | D | 16 BSC | | |
| | Y | E | 16 BSC | | |
| BODY SIZE | X | D1 | 14 BSC | | |
| | Y | E1 | 14 BSC | | |
| LEAD PITCH | | e | 0.8 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| FOOTPRINT | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | --- | --- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | --- | --- |
| | | R2 | 0.08 | --- | 0.2 |
| | | S | 0.2 | --- | --- |
| PACKAGE EDGE TOLERANCE | | aaa | 0.2 | | |
| LEAD EDGE TOLERANCE | | bbb | 0.2 | | |
| COPLANARITY | | ccc | 0.1 | | |
| LEAD OFFSET | | ddd | 0.2 | | |
| MOLD FLATNESS | | eee | 0.05 | | |

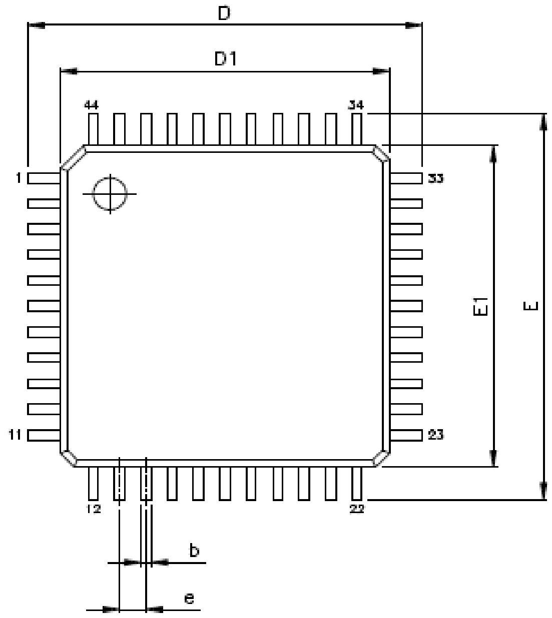



SECTION G–G
SCALE: 100/1



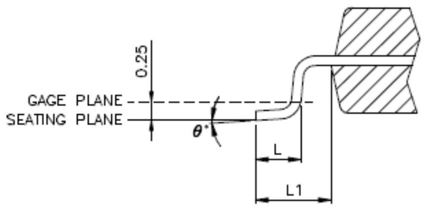

DETAIL F
SCALE: 15/1

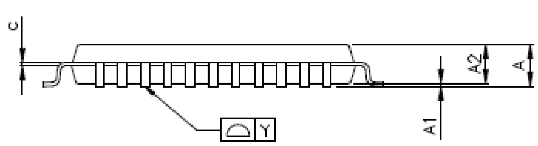
### 9.3 LQFP 44L (10x10x1.4mm, Footprint 2.0 mm)




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | – | – | 1.60 |
| A1 | 0.05 | – | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | – | 0.20 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| e | 0.80 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| θ | 0° | 3.5° | 7° |
| Y | 0.10 | | |



# 10 ABBREVIATIONS

## 10.1 Abbreviations

| Acronym | Description |
|---|---|
| ACMP | Analog Comparator Controller |
| ADC | Analog-to-Digital Converter |
| AES | Advanced Encryption Standard |
| APB | Advanced Peripheral Bus |
| AHB | Advanced High-Performance Bus |
| BOD | Brown-out Detection |
| CAN | Controller Area Network |
| DAP | Debug Access Port |
| DES | Data Encryption Standard |
| EADC | Enhanced Analog-to-Digital Converter |
| EBI | External Bus Interface |
| EMAC | Ethernet MAC Controller |
| EPWM | Enhanced Pulse Width Modulation |
| FIFO | First In, First Out |
| FMC | Flash Memory Controller |
| FPU | Floating-point Unit |
| GPIO | General-Purpose Input/Output |
| HCLK | The Clock of Advanced High-Performance Bus |
| HIRC | 12 MHz Internal High Speed RC Oscillator |
| HXT | 4~32 MHz External High Speed Crystal Oscillator |
| IAP | In Application Programming |
| ICP | In Circuit Programming |
| ISP | In System Programming |
| LDO | Low Dropout Regulator |
| LIN | Local Interconnect Network |
| LIRC | 10 kHz internal low speed RC oscillator (LIRC) |
| MPU | Memory Protection Unit |
| NVIC | Nested Vectored Interrupt Controller |
| PCLK | The Clock of Advanced Peripheral Bus |
| PDMA | Peripheral Direct Memory Access |
| PLL | Phase-Locked Loop |
| PWM | Pulse Width Modulation |

| | |
|---|---|
| QEI | Quadrature Encoder Interface |
| SD | Secure Digital |
| SPI | Serial Peripheral Interface |
| SPS | Samples per Second |
| TDES | Triple Data Encryption Standard |
| TK | Touch Key |
| TMR | Timer Controller |
| UART | Universal Asynchronous Receiver/Transmitter |
| UCID | Unique Customer ID |
| USB | Universal Serial Bus |
| WDT | Watchdog Timer |
| WWDT | Window Watchdog Timer |

Table 10.1-1 List of Abbreviations

# 11 REVISION HISTORY

| Date | Revision | Description |
|---|---|---|
| 2021.7.7 | 1.00 | Initial version. |

## Important Notice

**Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, “Insecure Usage”.**

**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

**All Insecure Usage shall be made at customer’s risk, and in the event that third parties lay claims to Nuvoton as a result of customer’s Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**