

$V_{DSM}$	=	1800 V
$I_{TAVM}$	=	730 A
$I_{TRMS}$	=	1150 A
$I_{TSM}$	=	9000 A
$V_{T0}$	=	0.80 V
$r_T$	=	0.540 mΩ

## Phase Control Thyristor

# 5STP 07D1800

Doc. No. 5SYA1027-05 Sep. 01

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability

### Blocking

Part Number	5STP 07D1800	5STP 07D1600	5STP 07D1200	Conditions
$V_{DRM}$ $V_{RRM}$	1800 V	1600 V	1200 V	$f = 50 \text{ Hz}$ , $t_p = 10 \text{ ms}$
$V_{RSM1}$	2000 V	1800 V	1400 V	$t_p = 5 \text{ ms}$ , single pulse
$I_{DRM}$	$\leq 100 \text{ mA}$			$V_{DRM}$
$I_{RRM}$	$\leq 100 \text{ mA}$			$V_{RRM}$
$dV/dt_{crit}$	1000 V/ $\mu\text{s}$			Exp. to $0.67 \times V_{DRM}$ , $T_j = 125^\circ\text{C}$

### Mechanical data

$F_M$	Mounting force	nom.	10 kN
		min.	8 kN
		max.	12 kN
a	Acceleration		
	Device unclamped		50 m/s <sup>2</sup>
	Device clamped		100 m/s <sup>2</sup>
m	Weight		0.3 kg
$D_S$	Surface creepage distance		25 mm
$D_a$	Air strike distance		14 mm

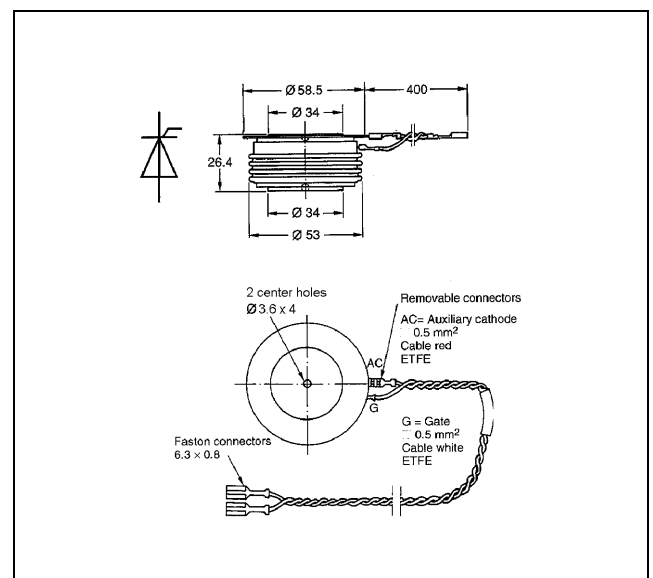


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## On-state

$I_{TAVM}$	Max. average on-state current	730 A	Half sine wave, $T_C = 70^\circ\text{C}$	
$I_{TRMS}$	Max. RMS on-state current	1150 A		
$I_{TSM}$	Max. peak non-repetitive	9000 A	$t_p = 10\text{ ms}$	$T_j = 125^\circ\text{C}$
	surge current	9500 A	$t_p = 8.3\text{ ms}$	After surge:
$I^2t$	Limiting load integral	405 $\text{kA}^2\text{s}$	$t_p = 10\text{ ms}$	$V_D = V_R = 0\text{V}$
		374 $\text{kA}^2\text{s}$	$t_p = 8.3\text{ ms}$	
$V_T$	On-state voltage	1.60 V	$I_T = 1500\text{ A}$	$T_j = 125^\circ\text{C}$
$V_{T0}$	Threshold voltage	0.80 V	$I_T = 500 - 1500\text{ A}$	
$r_T$	Slope resistance	0.540 $\text{m}\Omega$		
$I_H$	Holding current	20-70 mA	$T_j = 25^\circ\text{C}$	
		10-50 mA	$T_j = 125^\circ\text{C}$	
$I_L$	Latching current	80-500 mA	$T_j = 25^\circ\text{C}$	
		50-200 mA	$T_j = 125^\circ\text{C}$	

## Switching

$di/dt_{crit}$	Critical rate of rise of on-state current	150 $\text{A}/\mu\text{s}$	Cont. $f = 50\text{ Hz}$	$V_D \leq 0.67 \cdot V_{DRM}$ , $T_j = 125^\circ\text{C}$ $I_{TRM} = 1500\text{ A}$ $I_{FG} = 2\text{ A}$ , $t_r = 0.5\ \mu\text{s}$
		300 $\text{A}/\mu\text{s}$	60 sec. $f = 50\text{ Hz}$	
$t_d$	Delay time	$\leq 3.0\ \mu\text{s}$	$V_D = 0.4 \cdot V_{DRM}$	$I_{FG} = 2\text{ A}$ , $t_r = 0.5\ \mu\text{s}$
$t_q$	Turn-off time	$\leq 400\ \mu\text{s}$	$V_D \leq 0.67 \cdot V_{DRM}$ $dv_D/dt = 20\text{V}/\mu\text{s}$	$I_{TRM} = 1500\text{ A}$ , $T_j = 125^\circ\text{C}$ $V_R > 200\text{ V}$ , $di_T/dt = -20\text{ A}/\mu\text{s}$
$Q_{rr}$	Recovery charge	min	800 $\mu\text{As}$	
		max	1500 $\mu\text{As}$	

## Triggering

$V_{GT}$	Gate trigger voltage	2.6 V	$T_j = 25^\circ$
$I_{GT}$	Gate trigger current	400 mA	$T_j = 25^\circ$
$V_{GD}$	Gate non-trigger voltage	0.3 V	$V_D = 0.4 \times V_{DRM}$
$I_{GD}$	Gate non-trigger current	10 mA	$V_D = 0.4 \times V_{DRM}$
$V_{FGM}$	Peak forward gate voltage	12 V	
$I_{FGM}$	Peak forward gate current	10 A	
$V_{RGM}$	Peak reverse gate voltage	10 V	
$P_G$	Gate power loss	3 W	

### Thermal

$T_{jmax}$	Max. operating junction temperature range	125 °C	
$T_{stg}$	Storage temperature range	-40...140 °C	
$R_{thJC}$	Thermal resistance junction to case	70 K/kW	Anode side cooled
		74 K/kW	Cathode side cooled
		36 K/kW	Double side cooled
$R_{thCH}$	Thermal resistance case to heat sink	15 K/kW	Single side cooled
		7.5 K/kW	Double side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
$R_i(K/kW)$	19.18	9.82	5.45	1.44
$\tau_i(s)$	0.3862	0.0561	0.0058	0.0024

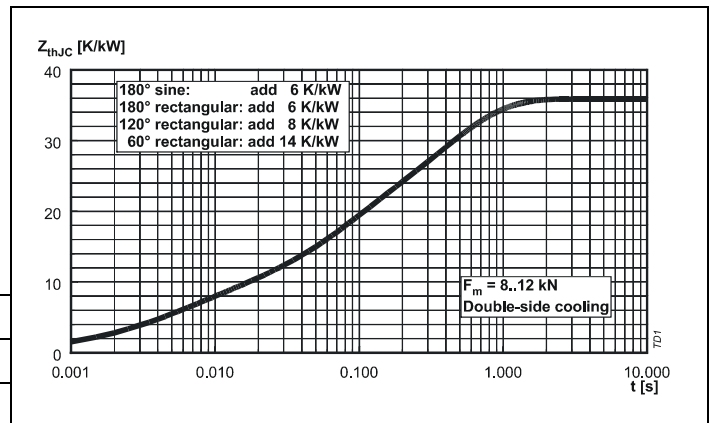


Fig. 1 Transient thermal impedance junction to case.

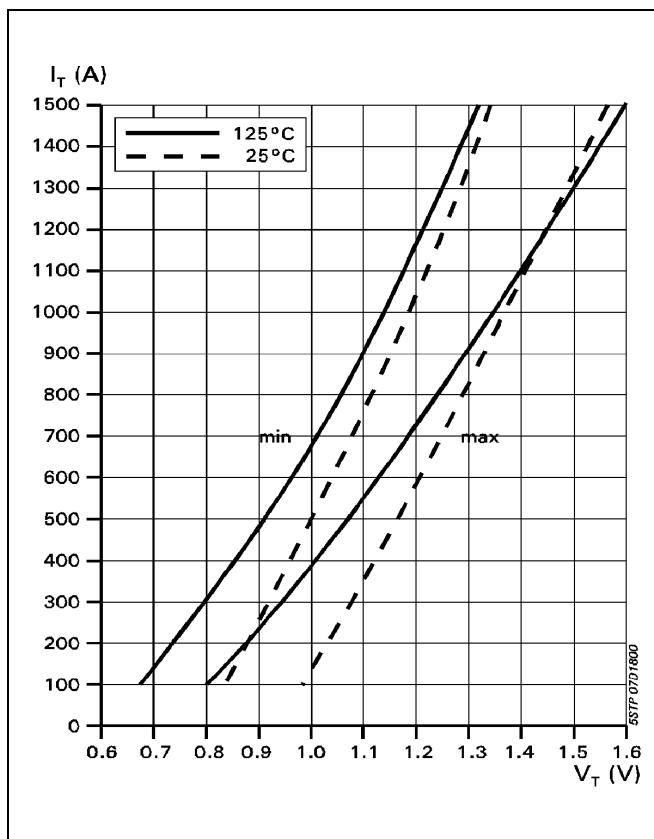


Fig. 2 On-state characteristics.

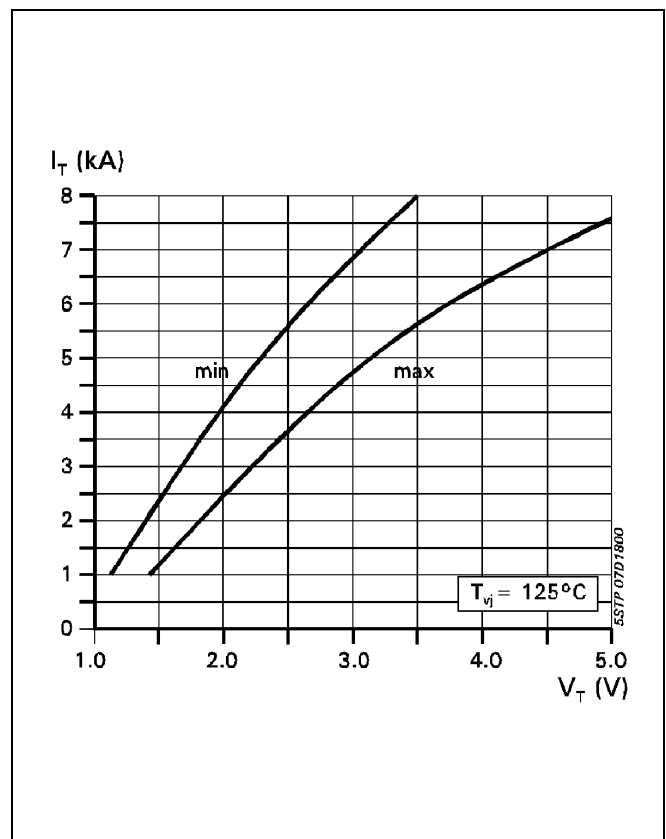


Fig. 3 On-state characteristics.  $T_{vj}=125^{\circ}C$ , 10ms half sine

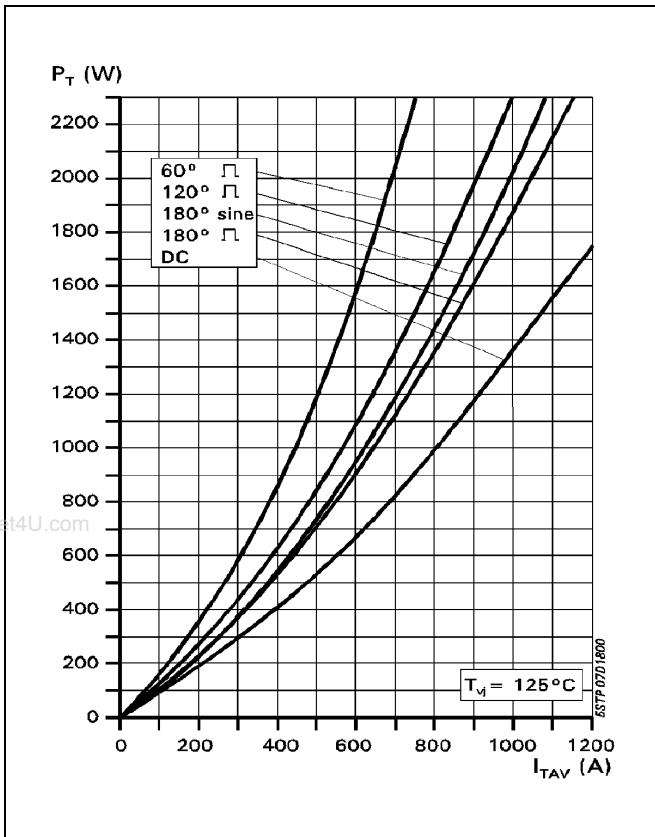


Fig. 4 On-state power dissipation vs. mean on-state current. Turn - on losses excluded.

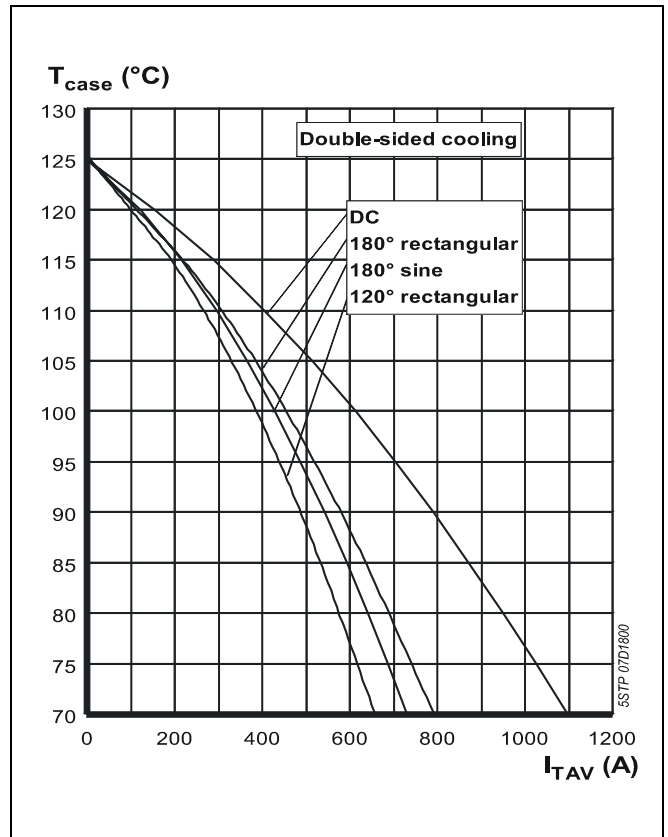


Fig. 5 Max. permissible case temperature vs. mean on-state current.

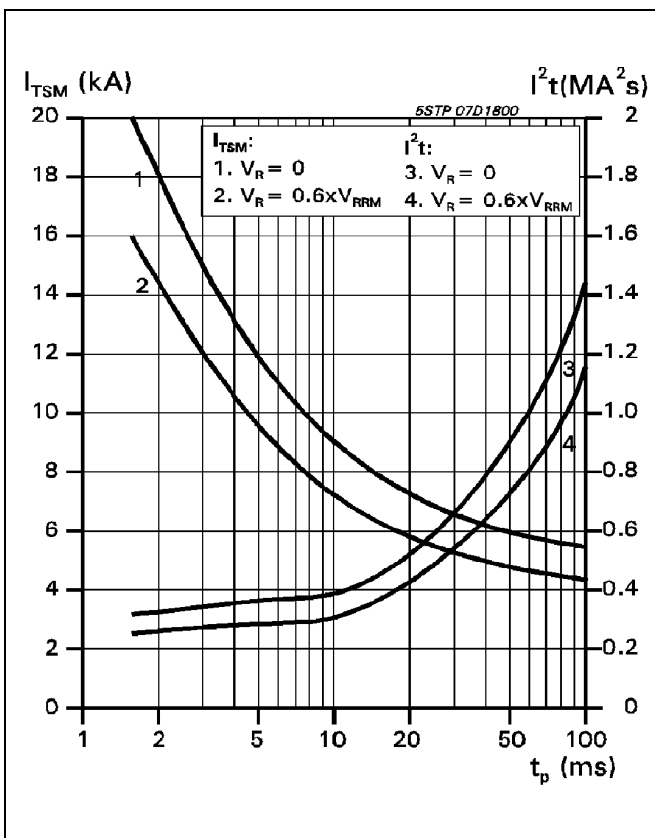


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

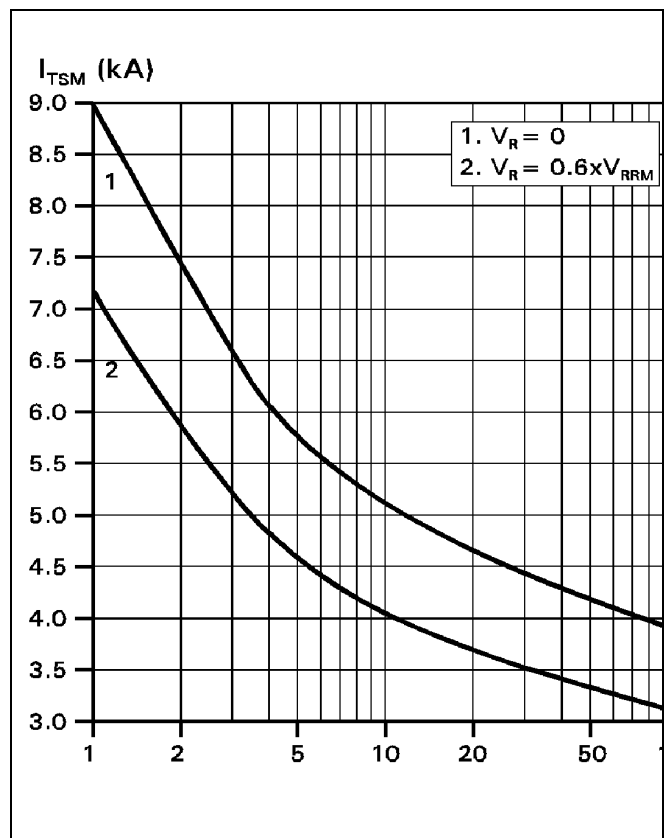


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

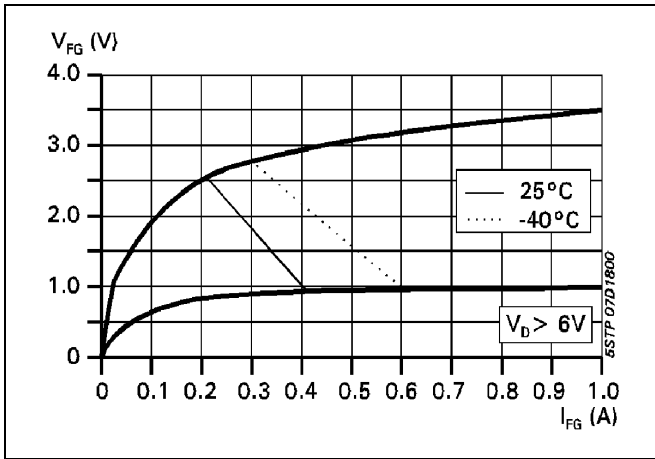


Fig. 8 Gate trigger characteristics.

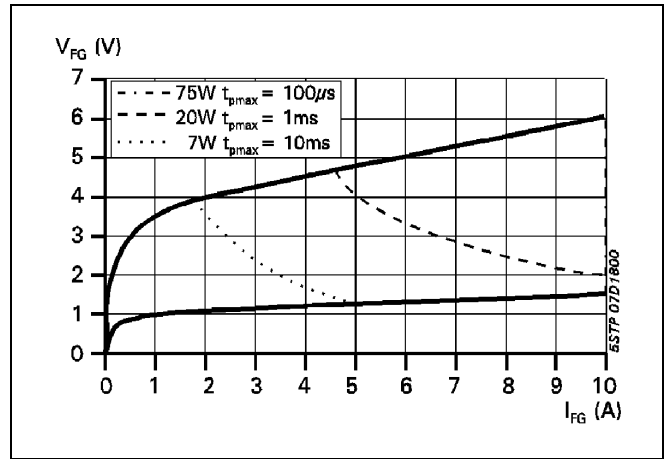


Fig. 9 Max. peak gate power loss.

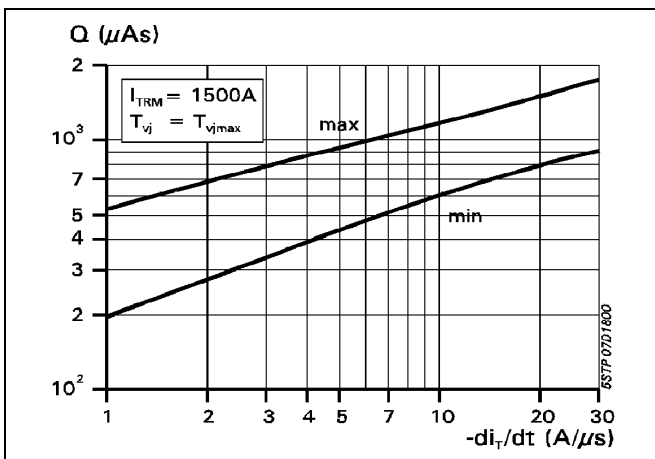


Fig. 10 Recovery charge vs. decay rate of on-state current.

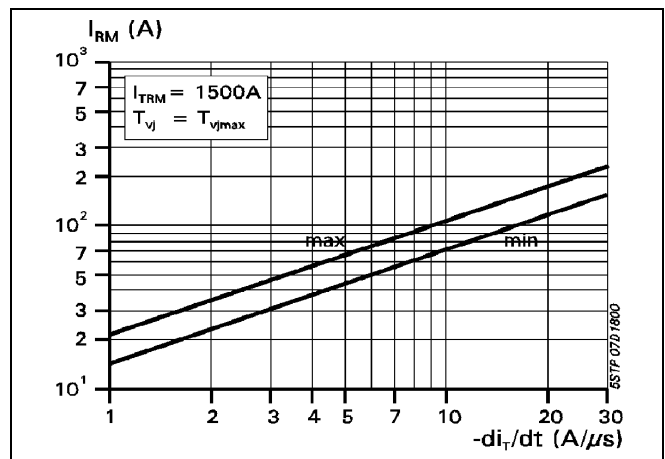


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

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