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16-CHANNEL ±100V 2A 3-LEVEL ULTRASOUND PULSER

Rev.1.1_00

S-UM5587P is a 16-channel, 3-level RTZ, high-voltage, high-speed ultrasound pulser.
The S-UM5587P comprises logic interfaces, level translators, MOSFET gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

■ Functions

- 16channel 3-level pulser with active T/R switch with 2-input per channel

■ Features

- 0 to ±100V output voltage
- ±2A source and sink peak current for pulsing (V_{PP}/V_{NN})
- ±1A source and sink peak current for active ground clamp
- 250Ω (±0.1A) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- Embedded floating voltage regulators
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- Up to 200MHz LVDS/LVCMOS clock (transparent mode available)
- 10Ω active T/R switch
- 20MHz output frequency at ±60V output, 220pF load
- 1.8V to 3.3V CMOS logic interface
- Noise-cut diodes at each high-voltage output
- Embedded high-voltage clamp diodes
- 4-mode output current control
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- BGA-330(1313)A: 13x13mm BGA package (RoHS compliant)

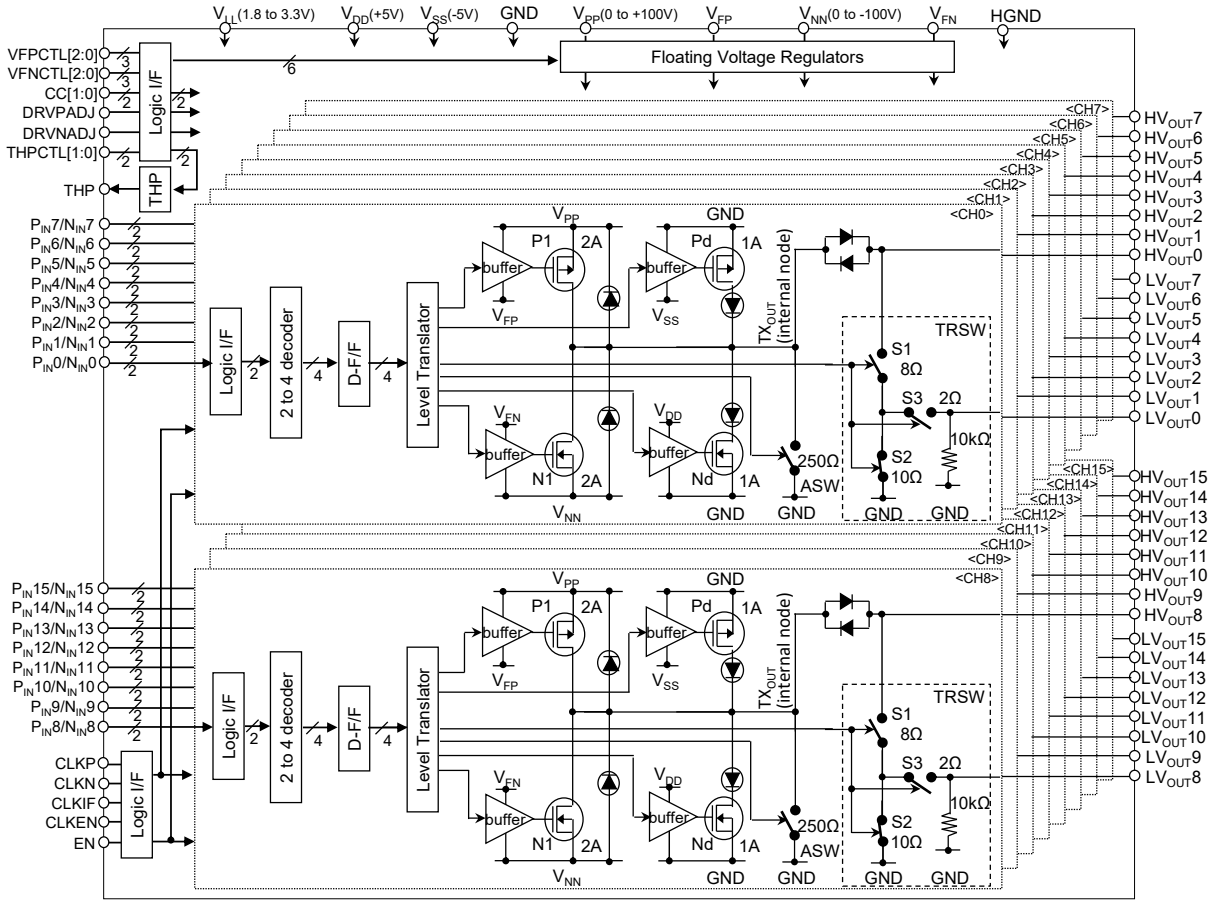

Figure 1 Block Diagram

■ Absolute Maximum Ratings

T_a=25˚C unless otherwise specified.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Negative supply voltage	V_{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	V_{PP}	-0.5 to +105	V	
5	Negative high-voltage supplies	V_{NN}	-105 to +0.5	V	
6	High-voltage outputs (x = 0 to 15)	$HV_{OUT}x$	-105 to +105	V	
7	Low-voltage outputs (x = 0 to 15)	$LV_{OUT}x$	-1 to +1	V	
8	Logic output voltage	SDOUT, FAULT	-0.4 to +7	V	
9	Logic input voltages	EN, CLKIF, CLKP, CLKN, CLKEN, CC[1:0], DRVPADJ, DRVNADJ, THPCTL<1:0>, VFPCTL<2:0>, VFNCTL<2:0>	-0.4 to +7	V	
10	Operating junction temperature	T_{Jop}	-20 to +125	°C	
11	Storage temperature	T_{STG}	-55 to +150	°C	
12	Maximum power dissipation	P_{Dmax}	4	W	

Remark Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

■ Operating Supply Voltages, Logic Inputs

1. Operating supply voltage and temperature

Table 2 Operating Supply Voltage and Temperature

No.	Items	Symbol	Min.	Typ.	Max.	Units	Condition
1	Logic supply voltage	V_{LL}	2.4	2.5 to 3.3	3.6	V	CMOS clock mode
			1.71	1.8 to 3.3	3.6	V	LVDS clock mode Transparent mode
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	V_{PP}	0	–	100	V	
5	Negative high-voltage supplies	V_{NN}	-100	–	0	V	
6	IC substrate voltage[*1]	V_{SUB}	–	0	–	V	
7	V_{PP}, $V_{NN\_}$ slew rate	SR_{MAX}	–	–	25	V/ms	
8	Operating free-air Temperature	T_A	0	–	75	°C	

***1.** The package exposed pad internally connected to the chip substrate must be soldered to the ground.

Clock Mode / Transparent Mode

Clock (CLK) mode synchronizes data inputs PINx, NINx (x=0 to 15) with a differential LVDS/CMOS clock.
Transparent (TP) mode without using clock is also available.

CLK mode:

Set CLKEN=0. PINx and NINx are decoded, clocked, level-translated, then sent to high-voltage output stage.
Differential clock input has two modes as shown below.

- LVDS CLK mode: set CLKIF=0. Connect 100Ω between CLKP and CLKN.
- CMOS CLK mode: set CLKIF=1.

TP mode:

Set CLKEN=CLKIF=1, CLKP/CLKN=0. PINx and NINx are decoded, level-translated, then sent to high-voltage output stage.

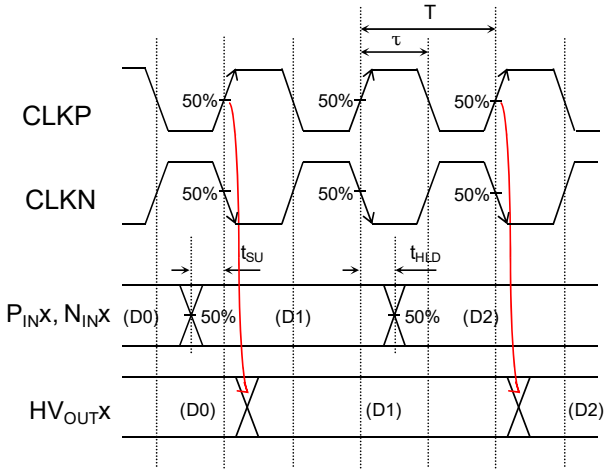

Figure 2 LVDS/CMOS CLK mode (CLKEN=0)

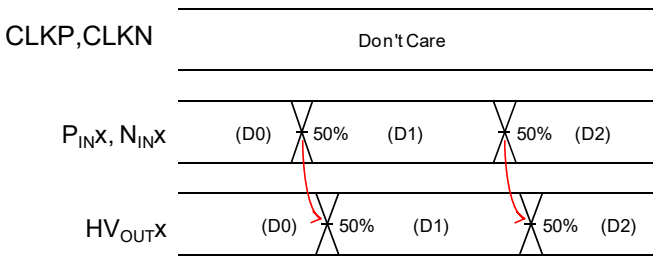

Figure 3 TP mode (CLKEN=1)

2. Logic inputs and outputs

2. 1 CMOS logic inputs

Table 3 CLKP/CLKN*3, PINx/NINx (x=0 to 15),CLKEN, CLKIF, EN, CC[1:0], DRVPADJ, DRVNADJ, VFPCT[2:0], VFNCTL[2:0], THPCTL[1:0]

No.	Items	Symbol	Min.	Typ.	Max.	Units	Condition	
1	High-level logic input voltage	V_{IH}	$0.8V_{LL}$	–	V_{LL}	V		
2	Low-level logic input voltage	V_{IL}	0	–	$0.2V_{LL}$	V		
3	Logic input capacitance	C_{IN}	–	3	–	pF		
4	Logic input high current *1	I_{IH}	-10	–	10	μA		
5	Logic input low current *2	I_{IL}	-10	–	10	μA		
6	Input rise/fall time	t_r, t_f	–	–	800	ps	CLK≥100MHz	CMOS CLK mode, 10 to 90% CLKP, CLKN, P_{INx}, N_{INx}
			–	–	2.0	ns	CLK<100MHz	
7	Input clock frequency	f_{CLK}	–	–	200	MHz	CMOS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ/T, See Fig.2	
8	Duty cycle	D_{CLK}	40	50	60	%		
9	Data setup time	t_{SU}	1.4	–	–	ns	CLK mode, P_{INx}, N_{INx} to CLK/CLKB See Fig.2	
10	Data hold time	t_{HLD}	1.4	–	–	ns		

***1.** DRVPADJ, DRVNADJ, VFPCT[2:0], VFNCTL[2:0], THPCTL[1:0] have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-down resistor.

***2.** EN, CC[1:0], CLKEN, and CLKIF have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

***3.** Differential CMOS or Single-ended CMOS is also available for CLKP/N, CSP/N, SCLKP/N and SDATAP/N. In case of single-ended CMOS, N-terminals (CLKN, CSPN, SCLKN and SDATAN) need to be connected to half of V_{LL} (V_{LL}/2).

2. 2 LVDS Differential Logic Inputs

Table 4 CLKP/CLKN

No.	Items	Symbol	Min.	Typ.	Max.	Units	Condition
1	High-level input voltage	V_{IH}	1.265	–	–	V	V_{IHCMR}(Typ)+V_{DIFF}(Min)/2
2	Low-level input voltage	V_{IL}	–	–	1.135	V	V_{IHCMR}(Typ)-V_{DIFF}(Min)/2
3	Differential input voltage range	$V_{DIFF(range)}$	0.13	0.35	0.49	±V	same as CLK,CLKB voltage swing
4	Differential input voltage peak to peak swing	$V_{DIFF(p-p)}$	0.26	0.7	0.98	V_{pp}	|CLK-CLKB| differential peak-to-peak voltage swing
5	Input voltage common mode range	V_{IHCMR}	0.84	1.2	1.56	V	
6	Differential input impedance	R_{IN}	85	100	115	Ω	External Resistor
7	High-level input current	I_{IH}	–	–	5.8	mA	
8	Low-level input current	I_{IL}	–	–	5.8	mA	
9	Input rise/fall time	t_r, t_f	–	–	600	ps	20% to 80% of V_{DIFF}
10	Input clock frequency	f_{CLK}	–	–	200	MHz	LVDS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ/T
11	Duty cycle	D_{CLK}	40	50	60	%	

NOTE: External termination Resister (100Ω) is necessary for LVDS I/F differential inputs.

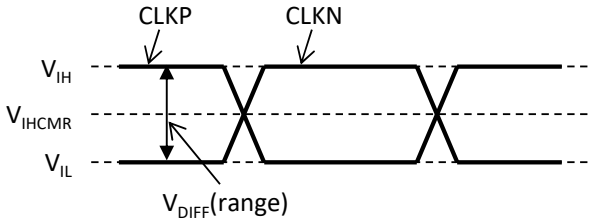

Figure 4 Differential input voltage range (V_{DIFF}(range))

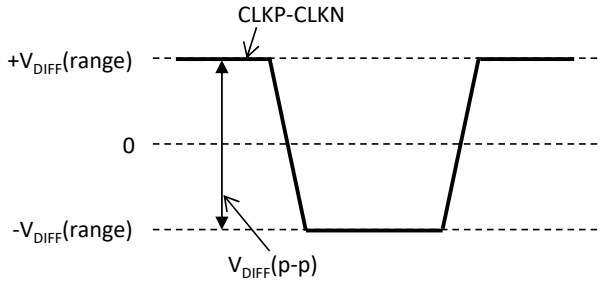

Figure 5 Differential input voltage peak to peak swing (V_{DIFF}(p-p))

2. 3 Open Drain Outputs

Table 5 THP

No.	Items	Symbol	Min.	Typ.	Max.	Units	Condition
1	Pull-up voltage	$V_{PUTXFLAG}$, $V_{PUFAULT}$	–	–	V_{LL}	V	Connected to V_{LL} with R1
2	Output low voltage	$V_{OLTXFLAG}$, $V_{OLFAULT}$	–	–	0.5	V	Active, V_{LL}=2.5V, R1=2.5kΩ
3	Output current	I_{TXFLAG}, I_{FAULT}	–	1.0	–	mA	V_{LL}=2.5V, R1=2.5kΩ
4	Off leak current	$I_{OFFLEAK}$	-10	–	10	μA	Disabled (Hi-Z)

■ Typical Application Circuit

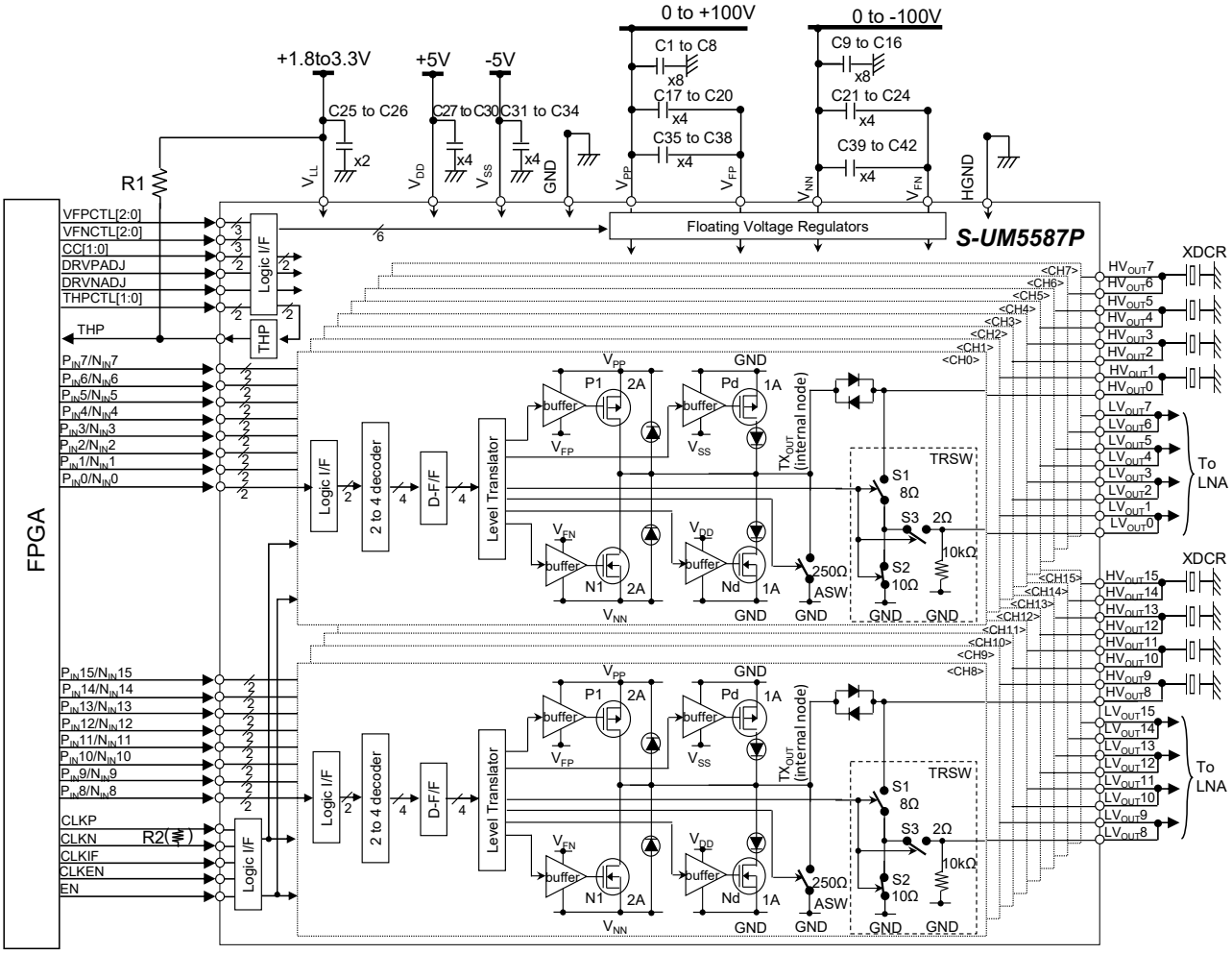

Figure 6 Typical Application Circuit

Remark C1 to C16: Ceramic capacitors of ≥200V 0.1μF to 1μF
C17 to C24: Ceramic capacitors of ≥16V 10μF
C25 to C42: Ceramic capacitors of ≥16V 0.1μF
R1: 2.5kΩ
R2: 100Ω (for LVDS I/F only)

■ Electrical Characteristics

1. Operating supply currents

Table 6 Operating Supply Currents (1/2)

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, T_A=25°C, CLKP/CLKN=100MHz,VFPCTL[2:0]=VFNCTL[2:0]='000'
HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min.	Typ.	Max.		
1	V_{LL} current	TP	I_{LLQD}	–	0.15	–	mA	Quiescent current-1 EN=1(Disable) $P_{IN}x$=$N_{IN}x$=0 Current mode 3 (CC[1:0]='11') V_{PP}/V_{NN}=±100V
		CMOS CLK		–	0.2	–	mA	
		LVDS CLK		–	0.25	–	mA	
2	V_{DD} current	TP	I_{DDQD}	–	4.4	–	mA	
		CMOS CLK		–	4.4	–	mA	
		LVDS CLK		–	4.4	–	mA	
3	V_{SS} current		I_{SSQD}	–	0.7	–	mA	
4	V_{PP} current		I_{PPQD}	–	0.1	–	mA	
5	V_{NN} current		I_{NNQD}	–	0.1	–	mA	
6	V_{LL} current		I_{LLQE}	–	0.2	–	mA	Quiescent current-2 EN=0(Enable) $P_{IN}x$=$N_{IN}x$=0 Current mode 3 (CC[1:0]='11') V_{PP}/V_{NN}=±100V
				–	0.25	–	mA	
				–	0.3	–	mA	
7	V_{DD} current		I_{DDQE}	–	5	–	mA	
				–	29	–	mA	
				–	31	–	mA	
8	V_{SS} current		I_{SSQE}	–	1	–	mA	
9	V_{PP} current		I_{PPQE}	–	0.3	–	mA	
10	V_{NN} current		I_{NNQE}	–	0.3	–	mA	
11	V_{LL} current	TP	I_{LLPW}	–	0.25	–	mA	PW operating current EN=0 Current mode 3 (CC[1:0]='11') 16-channel active Bipolar 3-level 2-cycle f=5MHz, PRT=200µs V_{PP}/V_{NN}=±60V
		CMOS CLK		–	0.3	–	mA	
		LVDS CLK		–	0.35	–	mA	
12	V_{DD} current	TP	I_{DDPW}	–	7	–	mA	
		CMOS CLK		–	29	–	mA	
		LVDS CLK		–	32	–	mA	
13	V_{SS} current		I_{SSPW}	–	2	–	mA	
14	V_{PP} current		I_{PPPW}	–	8	–	mA	
15	V_{NN} current		I_{NNPW}	–	9	–	mA	

Table 6 Operating Supply Currents (2/2)

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, T_A=25°C, CLKP/CLKN=100MHz,VFPCTL[2:0]=VFNCTL[2:0]='000'
HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min.	Typ.	Max.		
16	V_{LL} current	TP	I_{LLCW3}	–	1.1	–	mA	CW operating current-1 EN=0 Current mode 3 (CC[1:0]='11') 16-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=±5V
		CMOS CLK		–	1.15	–	mA	
		LVDS CLK		–	1.2	–	mA	
17	V_{DD} current	TP	I_{DDCW3}	–	77	–	mA	
		CMOS CLK		–	102	–	mA	
		LVDS CLK		–	106	–	mA	
18	V_{SS} current		I_{SSCW3}	–	51	–	mA	
19	V_{PP} current		I_{PPCW3}	–	400	–	mA	
20	V_{NN} current		I_{NNCW3}	–	420	–	mA	
21	V_{LL} current	TP	I_{LLCW2}	–	1.1	–	mA	CW operating current-2 EN=0 Current mode 2 (CC[1:0]='10') 16-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=±5V
		CMOS CLK		–	1.15	–	mA	
		LVDS CLK		–	1.2	–	mA	
22	V_{DD} current	TP	I_{DDCW2}	–	69	–	mA	
		CMOS CLK		–	95	–	mA	
		LVDS CLK		–	97	–	mA	
23	V_{SS} current		I_{SSCW2}	–	43	–	mA	
24	V_{PP} current		I_{PPCW2}	–	380	–	mA	
25	V_{NN} current		I_{NNCW2}	–	405	–	mA	
26	V_{LL} current	TP	I_{LLCW1}	–	1.1	–	mA	CW operating current-3 EN=0 Current mode 3 (CC[1:0]='01') 16-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=±5V
		CMOS CLK		–	1.15	–	mA	
		LVDS CLK		–	1.2	–	mA	
27	V_{DD} current	TP	I_{DDCW1}	–	60	–	mA	
		CMOS CLK		–	86	–	mA	
		LVDS CLK		–	88	–	mA	
28	V_{SS} current		I_{SSCW1}	–	35	–	mA	
29	V_{PP} current		I_{PPCW1}	–	360	–	mA	
30	V_{NN} current		I_{NNCW1}	–	380	–	mA	
31	V_{LL} current	TP	I_{LLCW0}	–	1.1	–	mA	CW operating current-4 EN=0 Current mode 2 (CC[1:0]='00') 16-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=±5V
		CMOS CLK		–	1.15	–	mA	
		LVDS CLK		–	1.2	–	mA	
32	V_{DD} current	TP	I_{DDCW0}	–	50	–	mA	
		CMOS CLK		–	77	–	mA	
		LVDS CLK		–	78	–	mA	
33	V_{SS} current		I_{SSCW0}	–	36	–	mA	
34	V_{PP} current		I_{PPCW0}	–	315	–	mA	
35	V_{NN} current		I_{NNCW0}	–	335	–	mA	

2. Static characteristics

Table 7 Static Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min.	Typ.	Max.		
1	$HV_{OUT}x$ output voltage range	$HV_{OUT}x$	-100	–	+100	V	
2	$HV_{OUT}x$ high-side peak current	I_{OH}	–	2.0	–	A	V_{PP}/V_{NN}=±60V, Current mode 3 (CC[1:0]='11')
			–	1.5	–	A	V_{PP}/V_{NN}=±60V, Current mode 2 (CC[1:0]='10')
			–	1.0	–	A	V_{PP}/V_{NN}=±60V, Current mode 1 (CC[1:0]='01')
			–	0.5	–	A	V_{PP}/V_{NN}=±60V, Current mode 0 (CC[1:0]='00')
3	$HV_{OUT}x$ high-side GND clamp peak current	I_{OHCL}	–	1.0	–	A	V_{PP}/V_{NN}=±60V
4	$HV_{OUT}x$ low-side peak current	I_{OL}	–	2.0	–	A	V_{PP}/V_{NN}=±60V, Current mode 3 (CC[1:0]='11')
			–	1.5	–	A	V_{PP}/V_{NN}=±60V, Current mode 2 (CC[1:0]='10')
			–	1.0	–	A	V_{PP}/V_{NN}=±60V, Current mode 1 (CC[1:0]='01')
			–	0.5	–	A	V_{PP}/V_{NN}=±60V, Current mode 0 (CC[1:0]='00')
5	$HV_{OUT}x$ low-side GND clamp peak current	I_{OLCL}	–	1.0	–	A	V_{PP}/V_{NN}=±60V
6	$HV_{OUT}x$ high-side on-resistance	R_{ONH}	–	10	–	Ω	I_{OH}=100mA, Current mode 3 (CC[1:0]='11')
			–	13	–	Ω	I_{OH}=100mA, Current mode 2 (CC[1:0]='10')
			–	18	–	Ω	I_{OH}=100mA, Current mode 1 (CC[1:0]='01')
			–	31	–	Ω	I_{OH}=100mA, Current mode 0 (CC[1:0]='00')
7	$HV_{OUT}x$ high-side GND clamp on-resistance	R_{ONHCL}	–	21	–	Ω	I_{OHCL}=100mA
8	$HV_{OUT}x$ low-side on-resistance	R_{ONL}	–	9	–	Ω	I_{OL}=100mA, Current mode 3 (CC[1:0]='11')
			–	12	–	Ω	I_{OL}=100mA, Current mode 2 (CC[1:0]='10')
			–	17	–	Ω	I_{OL}=100mA, Current mode 1 (CC[1:0]='01')
			–	30	–	Ω	I_{OL}=100mA, Current mode 0 (CC[1:0]='00')
9	$HV_{OUT}x$ low-side GND clamp on-resistance	R_{ONLCL}	–	20	–	Ω	I_{OLCL}=100mA
10	$HV_{OUT}x$ off-capacitance	C_{HVOFF}	–	34	–	pF	$TX_{OUT}x$=GND, TRSW=off

3. Dynamic characteristics

Table 8 Dynamic Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, T_A=25°C, CLKP/CLKN=100MHz,VFPCTL[2:0]=VFNCTL[2:0]='000'
HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min.	Typ.	Max.		
1	Output frequency		f_{OUT}	–	20	–	MHz	
2	Output rise propagation delay	TP mode	t_{dr}	–	31	–	ns	
		CLK mode		–	35	–	ns	
3	Output fall propagation delay	TP mode	t_{df}	–	31	–	ns	
		CLK mode		–	35	–	ns	
4	Output rise propagation delay clamp	TP mode	t_{drCL}	–	31	–	ns	
		CLK mode		–	35	–	ns	
5	Output fall propagation delay clamp	TP mode	t_{dfCL}	–	31	–	ns	
		CLK mode		–	35	–	ns	
6	Propagation delay matching		Δt_d	–	±1	±3	ns	
7	Output rise time		t_r	–	16	–	ns	CC[1:0]='11'
				–	24	–	ns	CC[1:0]='10'
				–	34	–	ns	CC[1:0]='01'
				–	44	–	ns	CC[1:0]='00'
			t_{rCL}	–	16	–	ns	
8	Output fall time		t_f	–	16	–	ns	CC[1:0]='11'
				–	24	–	ns	CC[1:0]='10'
				–	34	–	ns	CC[1:0]='01'
				–	44	–	ns	CC[1:0]='00'
			t_{fCL}	–	16	–	ns	
9	2nd harmonic distortion		HD2	–	-40	–	dBc	Bipolar, 2-cycle, f_{OUT}=5MHz
10	Pulse cancellation		HDPC	–	-40	–	dBc	
			HDPC2	–	-40	–	dBc	
11	RMS output jitter		t_J	–	10	–	ps	Bipolar CW, f_{OUT}=5MHz, V_{PP}/V_{NN}=±5V
12	Crosstalk between channels		X_{TLK}	–	-70	–	dB	f_{OUT}=5MHz, $10V_{p-p}$, HV_{OUT} load=50Ω
13	Output enable time	TP	t_{EN}	–	35	–	ns	
		LVDS CLK		–	1600	–	ns	
		CMOS CLK		–	1600	–	ns	
14	Output disable time		t_{DS}	–	37	–	ns	
15	Clock mode enable time		t_{CLKEN}	–	1600	–	ns	
16	Clock mode disable time		t_{CLKDS}	–	37	–	ns	

4. Integrated Peripheral Circuits Characteristics

4. 1 T/R Switch characteristics

Table 9 T/R Switch Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=±60V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min.	Typ.	Max.		
1	$LV_{OUT}x$ output voltage range	$LV_{OUT}x$	-0.85	–	+0.85	V	
2	TRSW on-resistance	R_{ONTR}	–	10	–	Ω	$HV_{OUT}x$=100mV, $LV_{OUT}x$=0V
3	TRSW on-capacitance	C_{ONTR}	–	15	–	pF	$LV_{OUT}x$=0V
4	TRSW off-resistance on HVOUTx	$R_{OFFTRHV}$	1	–	–	MΩ	
5	TRSW off-resistance on LVOUTx	$R_{OFFTRLV}$	8	10	12	kΩ	
6	Spike voltage on $HV_{OUT}x$ and $LV_{OUT}x$	V_{TRN}	–	–	50	mV_{PP}	50pF//200Ω load on $HV_{OUT}x$ 20pF//200Ω load on $LV_{OUT}x$
7	TRSW turn-on time	t_{dTRON}	–	300	–	ns	Logic input-to-ready for Rx signal See Fig.9
8	TRSW turn-off time	t_{dTROFF}	–	50	100	ns	See Fig.9
9	Tx setup time	t_{TXSU}	100	–	–	ns	$P_{IN}x=N_{IN}x$=0 (GND) for at least 100ns before Tx burst. See Fig.9

4. 2 Analog Switch

Table 10 Analog Switch Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min.	Typ.	Max.		
1	ASW on-resistance	R_{ONASW}	–	250	–	Ω	

4. 3 HV Blocking Diode

Table 11 Output HV Blocking Diode Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min.	Typ.	Max.		
1	Forward voltage	V_{FHVD}	–	1.0	–	V	I_F=100mA
			–	1.2	–	V	I_F=200mA
2	Reverse voltage	V_{RHVD}	200	–	–	V	I_R=1μA

4. 4 LV Noise-cut Diode

Table 12 Output LV Noise-cut Diode Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min.	Typ.	Max.		
1	Forward voltage	V_{FLVD}	–	1.1	–	V	I_F=100mA
			–	1.25	–	V	I_F=200mA

4. 5 Thermal Protection

Table 13 Thermal Protection Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=±5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min.	Typ.	Max.		
1	THP temperature threshold	T_{THP}	90	110	120	°C	THPCTL[1:0]=00
			120	130	140	°C	THPCTL[1:0]=01
			140	150	160	°C	THPCTL[1:0]=10
			120	130	140	°C	THPCTL[1:0]=11 (THP is disabled)
2	THP reset hysteresis	T_{HYSTHP}	5	10	20	°C	

■ Switching Time Diagram

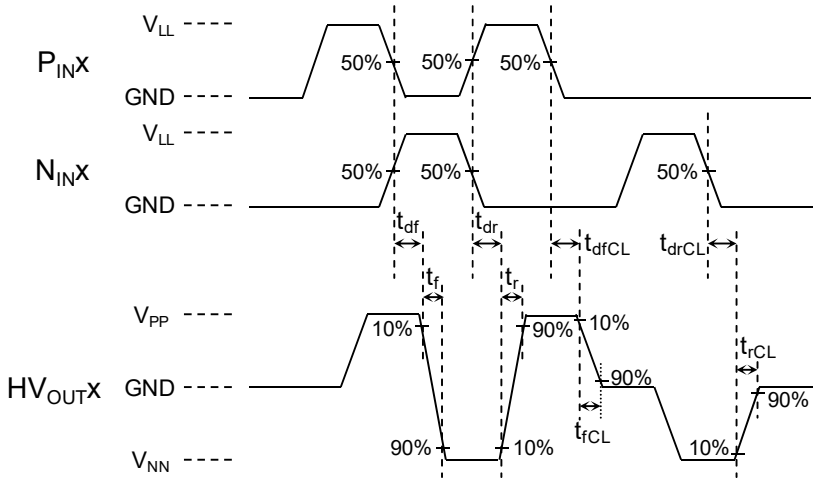

Figure 7 Propagation delay and Output rise/fall time

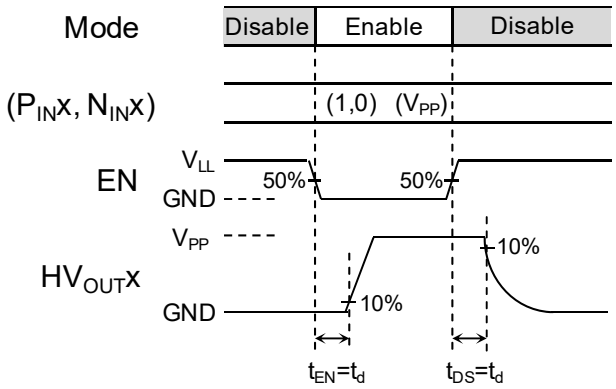

Figure 8 Output enable/disable time

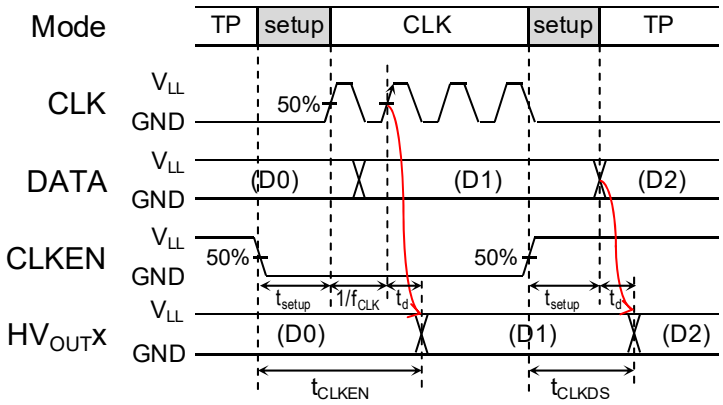

Figure 9 Clock enable/disable time

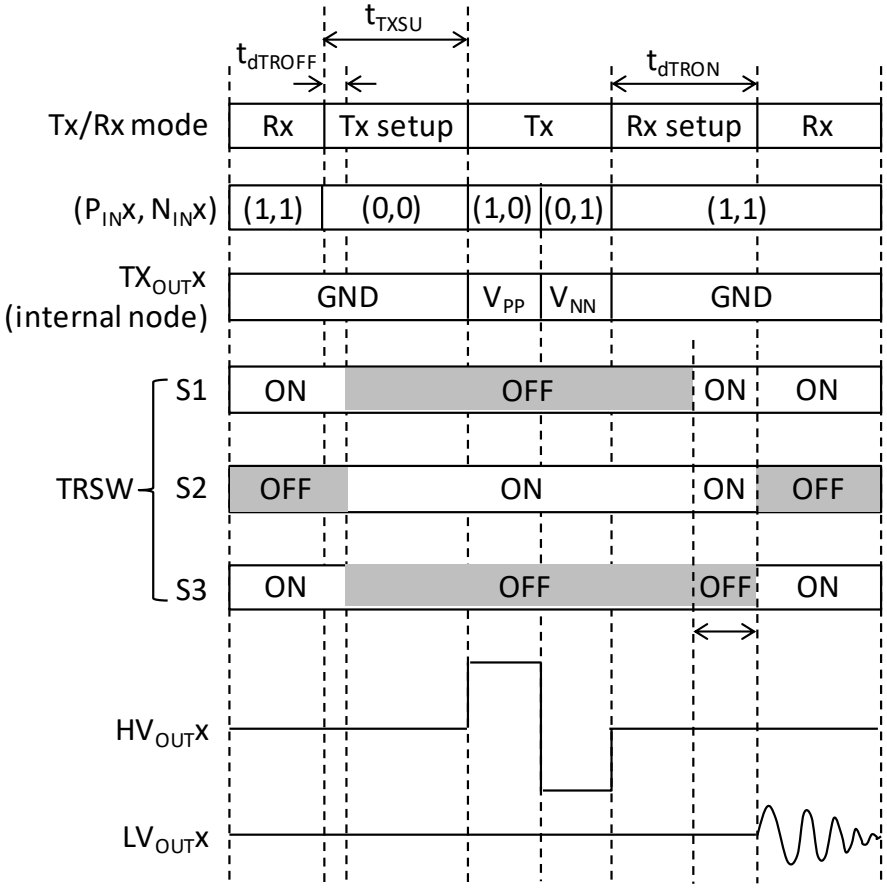

Figure 10 T/R Switch turn-on/off time

■ Truth Table

Table 14 Truth Table

Logic Inputs			Internal MOSFET state								Output state	
EN	P_{INx}	N_{INx}	P1	N1	P2	N2	ASW	TRSW			TX_{OUTx} (internal node)	LV_{OUTx}
			+HV	-HV	GND	GND	GND	S1	S2	S3		
0	0	0	OFF	OFF	**ON**	**ON**	**ON**	OFF	**ON**	OFF	GND	10kΩ
0	0	1	OFF	**ON**	OFF	OFF	OFF	OFF	**ON**	OFF	-HV	10kΩ
0	1	0	**ON**	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	+HV	10kΩ
0	1	1	OFF	OFF	**ON**	**ON**	**ON**	**ON**	OFF	**ON**	GND	HV_{OUTx}
1	*	*	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	Hi-Z	10kΩ

Table 15

Current mode	CC1	CC0	DRVP ADJ	DRVN ADJ	I_{OUT}[A]	
					P1	N1
0	0	0	×	×	0.5	0.5
1	0	1	×	×	1	1
2	1	0	×	×	1.5	1.5
3	1	1	0	0	2	2
			0	1	2	2.1
			1	0	2.1	2
			1	1	2.1	2.1

Remark ×: Don't care

Table 16

VFPCTL			VPP-VFP [V]
[2]	[1]	[0]	
0	0	0	5
0	0	1	5.15
0	1	0	5.3
0	1	1	5.45
1	0	0	5
1	0	1	4.85
1	1	0	4.7
1	1	1	4.55

Table 17

VFNCTL			VFN-VNN [V]
[2]	[1]	[0]	
0	0	0	5
0	0	1	5.15
0	1	0	5.3
0	1	1	5.45
1	0	0	5
1	0	1	4.85
1	1	0	4.7
1	1	1	4.55

Table 18

Current mode	CC1	CC0	DRVP ADJ	DRVN ADJ	I_{OUT}[A]	
					P1	N1
0	0	0	0	0	0.5	0.5
			0	1	0.5	0.6
			1	0	0.6	0.5
			1	1	0.6	0.6
1	0	1	0	0	1	1
			0	1	1	1.1
			1	0	1.1	1
			1	1	1.1	1.1
2	1	0	0	0	1.5	1.5
			0	1	1.5	1.6
			1	0	1.6	1.5
			1	1	1.6	1.6
3	1	1	0	0	2	2
			0	1	2	2.1
			1	0	2.1	2
			1	1	2.1	2.1

Table 19

VFPCTL			VPP-VFP [V]
[2]	[1]	[0]	
0	0	0	5
0	0	1	5.15
0	1	0	5.3
0	1	1	5.45
1	0	0	5
1	0	1	4.85
1	1	0	4.7
1	1	1	4.55

Table 20

VFNCTL			VFN-VNN [V]
[2]	[1]	[0]	
0	0	0	5
0	0	1	5.15
0	1	0	5.3
0	1	1	5.45
1	0	0	5
1	0	1	4.85
1	1	0	4.7
1	1	1	4.55

Table 21

THPCTL		THP Threshold [°C]	Tx reset function	FAULT Indication
[1]	[0]			
0	0	110	ON	ON
0	1	130	ON	ON
1	0	150	ON	ON
1	1	130	OFF	ON

■ Pin Configuration

Table 22 Pin Configuration

No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
A1	GND	C1	LVOUT1	E1	PIN0	G1	PIN2	J1	VDD	L1	VSS	N1	PIN13	Q1	PIN15	S1	LVOUT14	U1	GND
A2	VNN	C2	GND	E2	NIN0	G2	NIN2	J2	VDD	L2	VSS	N2	NIN13	Q2	NIN15	S2	GND	U2	VNN
A3	VFN	C3	GND	E3	GND	G3	GND	J3	VLL	L3	GND	N3	GND	Q3	GND	S3	GND	U3	VFN
A4	HVOUT0	C4	GND	E4	GND(T)	G4	GND(T)	J4	GND(T)	L4	GND(T)	N4	GND(T)	Q4	GND(T)	S4	GND	U4	HVOUT15
A5	HGND	C5	GND	E5	GND(T)	G5	GND(T)	J5	GND(T)	L5	GND(T)	N5	GND(T)	Q5	GND(T)	S5	GND	U5	HGND
A6	HVOUT2	C6	GND	E6	GND(T)	-	-	-	-	-	-	-	-	Q6	GND(T)	S6	GND	U6	HVOUT13
A7	VFP	C7	GND	E7	GND(T)	G7	GND(T)	J7	GND(T)	L7	GND(T)	N7	GND(T)	Q7	GND(T)	S7	GND	U7	VFP
A8	VPP	C8	GND	E8	GND(T)	G8	GND(T)	J8	GND(T)	L8	GND(T)	N8	GND(T)	Q8	GND(T)	S8	GND	U8	VPP
A9	LVOUT2	C9	GND	E9	GND(T)	G9	GND(T)	J9	GND(T)	L9	GND(T)	N9	GND(T)	Q9	GND(T)	S9	GND	U9	LVOUT13
A10	HGND	C10	GND	E10	GND(T)	G10	GND(T)	J10	GND(T)	L10	GND(T)	N10	GND(T)	Q10	GND(T)	S10	GND	U10	HGND
A11	LVOUT4	C11	GND	E11	GND(T)	G11	GND(T)	J11	GND(T)	L11	GND(T)	N11	GND(T)	Q11	GND(T)	S11	GND	U11	LVOUT11
A12	VPP	C12	GND	E12	GND(T)	G12	GND(T)	J12	GND(T)	L12	GND(T)	N12	GND(T)	Q12	GND(T)	S12	GND	U12	VPP
A13	VFP	C13	GND	E13	GND(T)	G13	GND(T)	J13	GND(T)	L13	GND(T)	N13	GND(T)	Q13	GND(T)	S13	GND	U13	VFP
A14	HVOUT4	C14	GND	E14	GND(T)	-	-	-	-	-	-	-	-	Q14	GND(T)	S14	GND	U14	HVOUT11
A15	HGND	C15	GND	E15	GND(T)	G15	GND(T)	J15	GND(T)	L15	GND(T)	N15	GND(T)	Q15	GND(T)	S15	GND	U15	HGND
A16	HVOUT6	C16	GND	E16	GND(T)	G16	GND(T)	J16	GND(T)	L16	GND(T)	N16	GND(T)	Q16	GND(T)	S16	GND	U16	HVOUT9
A17	VFN	C17	GND	E17	GND	G17	GND	J17	GND	L17	VLL	N17	GND	Q17	GND	S17	GND	U17	VFN
A18	VNN	C18	GND	E18	NIN7	G18	NIN5	J18	VSS	L18	VDD	N18	NIN10	Q18	NIN8	S18	GND	U18	VNN
A19	GND	C19	LVOUT7	E19	PIN7	G19	PIN5	J19	VSS	L19	VDD	N19	PIN10	Q19	PIN8	S19	LVOUT8	U19	GND
B1	LVOUT0	D1	VFNCTL0	F1	PIN1	H1	PIN3	K1	CLKP	M1	PIN12	P1	PIN14	R1	VFPCTL0	T1	LVOUT15		
B2	VNN	D2	VFNCTL1	F2	NIN1	H2	NIN3	K2	CLKN	M2	NIN12	P2	NIN14	R2	VFPCTL1	T2	VNN		
B3	VNN	D3	VFNCTL2	F3	GND	H3	EN	K3	GND	M3	CLKEN	P3	GND	R3	VFPCTL2	T3	VNN		
B4	HVOUT1	D4	GND(T)	F4	GND(T)	H4	GND(T)	K4	GND(T)	M4	GND(T)	P4	GND(T)	R4	GND(T)	T4	HVOUT14		
B5	HGND	D5	GND(T)	F5	GND(T)	H5	GND(T)	K5	GND(T)	M5	GND(T)	P5	GND(T)	R5	GND(T)	T5	HGND		
B6	HVOUT3	D6	GND(T)	F6	GND(T)	-	-	-	-	-	-	-	-	R6	GND(T)	T6	HVOUT12		
B7	VPP	D7	GND(T)	-	-	H7	GND(T)	K7	GND(T)	M7	GND(T)	-	-	R7	GND(T)	T7	VPP		
B8	VPP	D8	GND(T)	-	-	H8	GND(T)	K8	GND(T)	M8	GND(T)	-	-	R8	GND(T)	T8	VPP		
B9	LVOUT3	D9	GND(T)	-	-	H9	GND(T)	K9	GND(T)	M9	GND(T)	-	-	R9	GND(T)	T9	LVOUT12		
B10	HGND	D10	GND(T)	-	-	H10	GND(T)	K10	GND(T)	M10	GND(T)	-	-	R10	GND(T)	T10	HGND		
B11	LVOUT5	D11	GND(T)	-	-	H11	GND(T)	K11	GND(T)	M11	GND(T)	-	-	R11	GND(T)	T11	LVOUT10		
B12	VPP	D12	GND(T)	-	-	H12	GND(T)	K12	GND(T)	M12	GND(T)	-	-	R12	GND(T)	T12	VPP		
B13	VPP	D13	GND(T)	-	-	H13	GND(T)	K13	GND(T)	M13	GND(T)	-	-	R13	GND(T)	T13	VPP		
B14	HVOUT5	D14	GND(T)	-	-	-	-	-	-	-	-	-	-	R14	GND(T)	T14	HVOUT10		
B15	HGND	D15	GND(T)	F15	GND(T)	H15	GND(T)	K15	GND(T)	M15	GND(T)	P15	GND(T)	R15	GND(T)	T15	HGND		
B16	HVOUT7	D16	GND(T)	F16	GND(T)	H16	GND(T)	K16	GND(T)	M16	GND(T)	P16	GND(T)	R16	GND(T)	T16	HVOUT8		
B17	VNN	D17	GND	F17	GND	H17	DRVNADJ	K17	GND	M17	DRVPADJ	P17	GND	R17	GND	T17	VNN		
B18	VNN	D18	THPCTL0	F18	NIN6	H18	NIN4	K18	CLKIF	M18	NIN11	P18	NIN9	R18	CC0	T18	VNN		
B19	LVOUT6	D19	THPCTL1	F19	PIN6	H19	PIN4	K19	THP	M19	PIN11	P19	PIN9	R19	CC1	T19	LVOUT9		

■ Pin Configuration (MAP)

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	GND	VNN	VFN	HVOUT 0	HGND	HVOUT 2	VFP	VPP	LVOUT 2	HGND	LVOUT 4	VPP	VFP	HVOUT 4	HGND	HVOUT 6	VFN	VNN	GND
B	LVOUT 0	VNN	VNN	HVOUT 1	HGND	HVOUT 3	VPP	VPP	LVOUT 3	HGND	LVOUT 5	VPP	VPP	HVOUT 5	HGND	HVOUT 7	VNN	VNN	LVOUT 6
C	LVOUT 1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	LVOUT 7
D	VFN CTL0	VFN CTL1	VFN CTL2	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND	THP CTL0	THP CTL1
E	PIN0	NIN0	GND	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND	NIN7	PIN7
F	PIN1	NIN1	GND	GND(T)	GND(T)	GND(T)	-	-	-	-	-	-	-	-	GND(T)	GND(T)	GND	NIN6	PIN6
G	PIN2	NIN2	GND	GND(T)	GND(T)	-	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	-	GND(T)	GND(T)	GND	NIN5	PIN5
H	PIN3	NIN3	EN	GND(T)	GND(T)	-	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	-	GND(T)	GND(T)	DRVN ADJ	NIN4	PIN4
J	VDD	VDD	VLL	GND(T)	GND(T)	-	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	-	GND(T)	GND(T)	GND	VSS	VSS
K	CLKP	CLKN	GND	GND(T)	GND(T)	-	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	-	GND(T)	GND(T)	GND	CLKIF	THP
L	VSS	VSS	GND	GND(T)	GND(T)	-	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	-	GND(T)	GND(T)	VLL	VDD	VDD
M	PIN12	NIN12	CLKEN	GND(T)	GND(T)	-	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	-	GND(T)	GND(T)	DRVP ADJ	NIN11	PIN11
N	PIN13	NIN13	GND	GND(T)	GND(T)	-	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	-	GND(T)	GND(T)	GND	NIN10	PIN10
P	PIN14	NIN14	GND	GND(T)	GND(T)	-	-	-	-	-	-	-	-	-	GND(T)	GND(T)	GND	NIN9	PIN9
Q	PIN15	NIN15	GND	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND	NIN8	PIN8
R	VFP CTL0	VFP CTL1	VFP CTL2	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND(T)	GND	CC0	CC1
S	LVOUT 14	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	LVOUT 8
T	LVOUT 15	VNN	VNN	HVOUT 14	HGND	HVOUT 12	VPP	VPP	LVOUT 12	HGND	LVOUT 10	VPP	VPP	HVOUT 10	HGND	HVOUT 8	VNN	VNN	LVOUT 9
U	GND	VNN	VFN	HVOUT 15	HGND	HVOUT 13	VFP	VPP	LVOUT 13	HGND	LVOUT 11	VPP	VFP	HVOUT 11	HGND	HVOUT 9	VFN	VNN	GND

Figure 11 Pin Configuration (MAP)

■ Pin Description

Table 23 Pin Description

Pin name	Function	Pin name	Function
VPP	Positive high voltage power supply (0 to +100V)	CLKP	Positive clock input (up to 200MHz)
VFP	Built-in power supply for P-MOS (P1) gate drive	CLKN	Negative clock Input (up to 200MHz)
VNN	negative high voltage power supply (0 to -100V)	CLKIF	Clock I/F selection: H=CMOS L=LVDS (50kΩ internal pull-up)
VFN	Built-in power supply for N-MOS (N1) gate drive	CLKEN	Control of clock enable, H=disable, L=enable (50kΩ internal pull-up)
VLL	Positive low voltage power supply (+2.5 ~ 3.3V)	THPCTL[1:0]	THP detection control (00: 110deg, 01:130deg, 10:150deg, 11:disabled)
VDD	Positive low voltage power supply (+5V)	DRVPADJ	Size adjustment for P1 Driver (0:none, 1:+0.1A to P1drive current)
VSS	Negative low voltage power supply (-5V)	DRVNADJ	Size adjustment for N1 Driver (0:none, 1:+0.1A to N1 drive current)
HGND	Drive power ground (0V)	CC[1:0]	Control of P1/N1 drive current (50kΩ internal pull-up)
GND	Logic power ground (0V)	VFPCTL:[2:0]	Built-in power supply control for P-MOS gatedrive
GND(T)	Ground for Thermal heat sink	VFNCTL:[2:0]	Built-in power supply control for N-MOS gatedrive
EN	Control of chip enable, H=disable, L=enable (50kΩ internal pull-up)	THP	THP output flag, Open N-MOS drain
$P_{IN}0$	Logic inputs for channel 0	HVOUT0	High voltage output of channel 0
$N_{IN}0$		HVOUT1	High voltage output of channel 1
$P_{IN}1$	Logic inputs for channel 1	HVOUT2	High voltage output of channel 2
$N_{IN}1$		HVOUT3	High voltage output of channel 3
$P_{IN}2$	Logic inputs for channel 2	HVOUT4	High voltage output of channel 4
$N_{IN}2$		HVOUT5	High voltage output of channel 5
$P_{IN}3$	Logic inputs for channel 3	HVOUT6	High voltage output of channel 6
$N_{IN}3$		HVOUT7	High voltage output of channel 7
$P_{IN}4$	Logic inputs for channel 4	HVOUT8	High voltage output of channel 8
$N_{IN}4$		HVOUT9	High voltage output of channel 9
$P_{IN}5$	Logic inputs for channel 5	HVOUT10	High voltage output of channel 10
$N_{IN}5$		HVOUT11	High voltage output of channel 11
$P_{IN}6$	Logic inputs for channel 6	HVOUT12	High voltage output of channel 12
$N_{IN}6$		HVOUT13	High voltage output of channel 13
$P_{IN}7$	Logic inputs for channel 7	HVOUT14	High voltage output of channel 14
$N_{IN}7$		HVOUT15	High voltage output of channel 15
$P_{IN}8$	Logic inputs for channel 8	LVOUT0	Low voltage output of channel 0
$N_{IN}8$		LVOUT1	Low voltage output of channel 1
$P_{IN}9$	Logic inputs for channel 9	LVOUT2	Low voltage output of channel 2
$N_{IN}9$		LVOUT3	Low voltage output of channel 3
$P_{IN}10$	Logic inputs for channel 10	LVOUT4	Low voltage output of channel 4
$N_{IN}10$		LVOUT5	Low voltage output of channel 5
$P_{IN}11$	Logic inputs for channel 11	LVOUT6	Low voltage output of channel 6
$N_{IN}11$		LVOUT7	Low voltage output of channel 7
$P_{IN}12$	Logic inputs for channel 12	LVOUT8	Low voltage output of channel 8
$N_{IN}12$		LVOUT9	Low voltage output of channel 9
$P_{IN}13$	Logic inputs for channel 13	LVOUT10	Low voltage output of channel 10
$N_{IN}13$		LVOUT11	Low voltage output of channel 11
$P_{IN}14$	Logic inputs for channel 14	LVOUT12	Low voltage output of channel 12
$N_{IN}14$		LVOUT13	Low voltage output of channel 13
$P_{IN}15$	Logic inputs for channel 15	LVOUT14	Low voltage output of channel 14
$N_{IN}15$		LVOUT15	Low voltage output of channel 15

■ Package

Table 24 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
BGA-330(1313)A	RA330-A-P-SD	RA330-A-T-SD	RA330-A-M-SD	RA330-A-L-SD	RA330-A-K-SD

■ Storage, Mounting

1. Storage Conditions

1. 1 The storage location should be kept at 5 to 35 ºC and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125 ºC lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 12 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

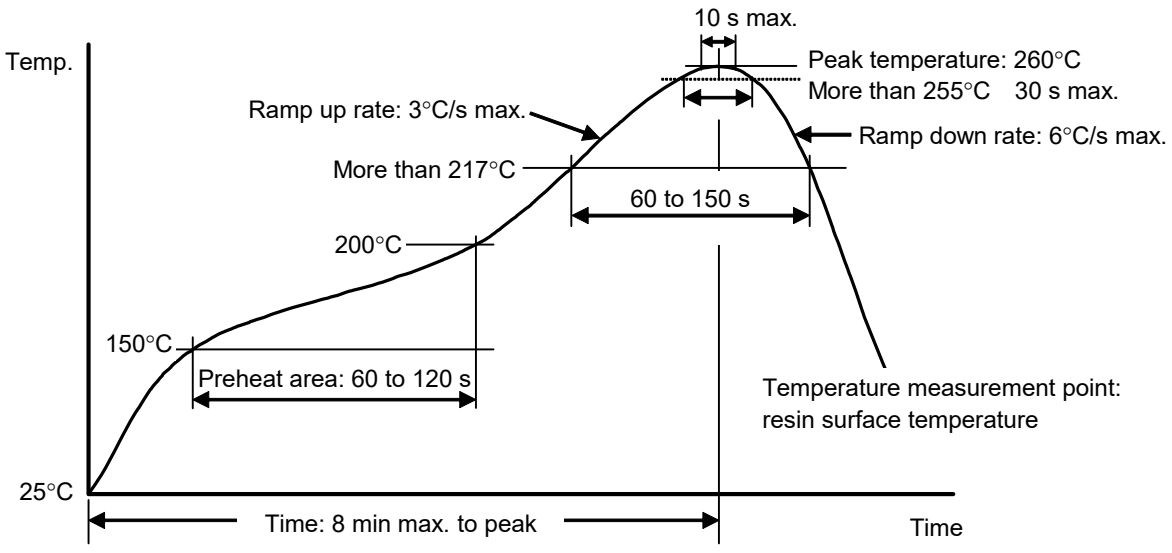

Figure 12 Resistance to soldering heat condition for package (Reflow method)

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2. Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before of such claim shall not be counted for such response.

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■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

   1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

   1. 2 Those what touch products such as work platform, machine, measurement/test equipment should be grounded.

   1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

   1. 4 Prevent friction with other materials made with high polymer.

   1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

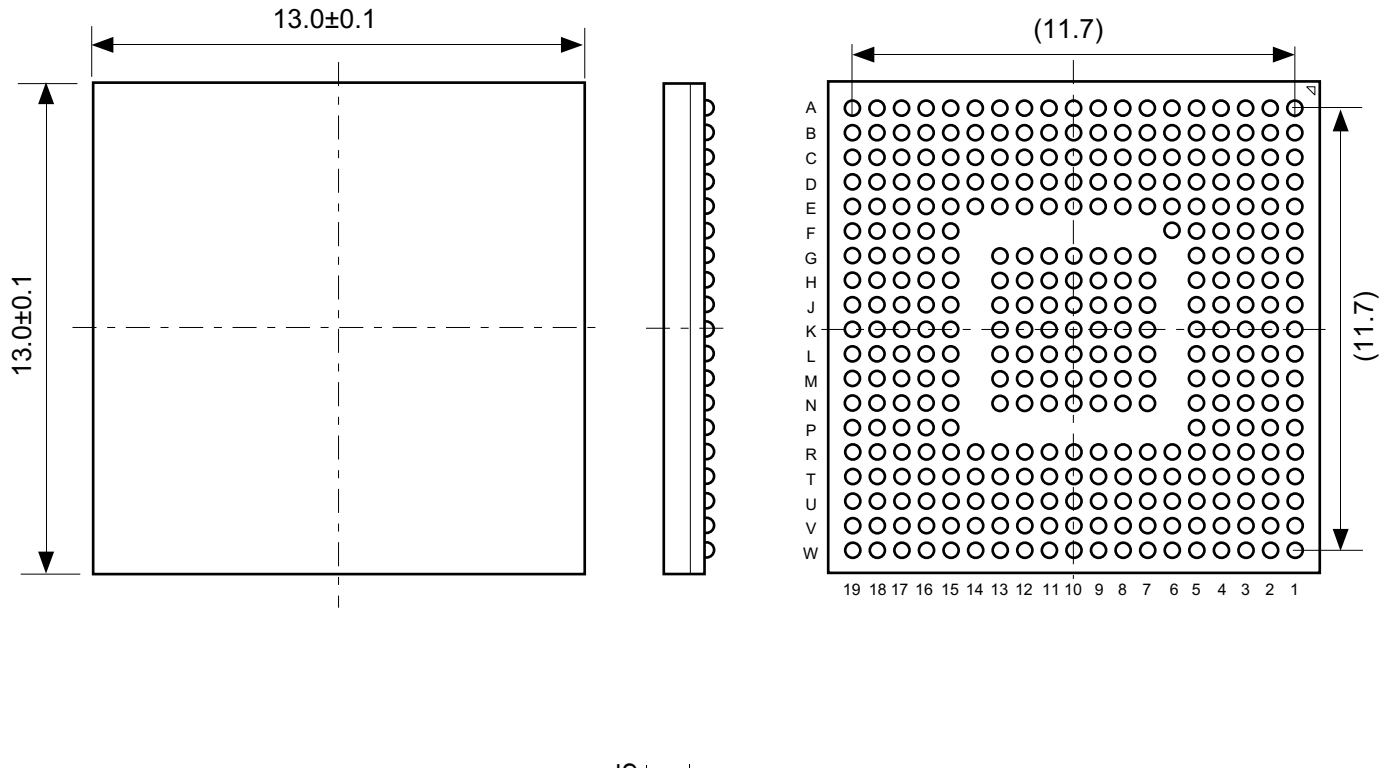
   1. 6 Avoid dealing with or storing products in an extremely arid environment.

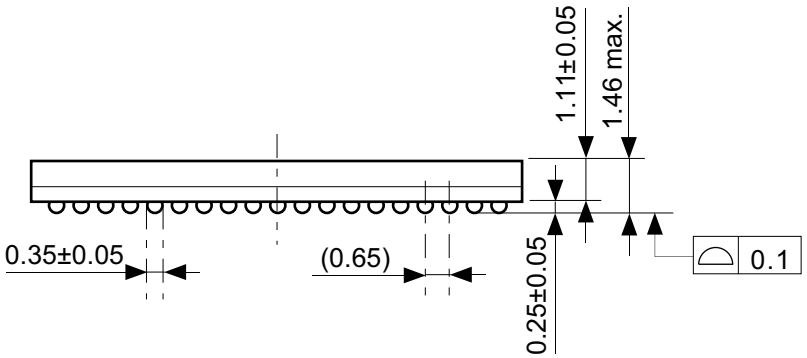
2. “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

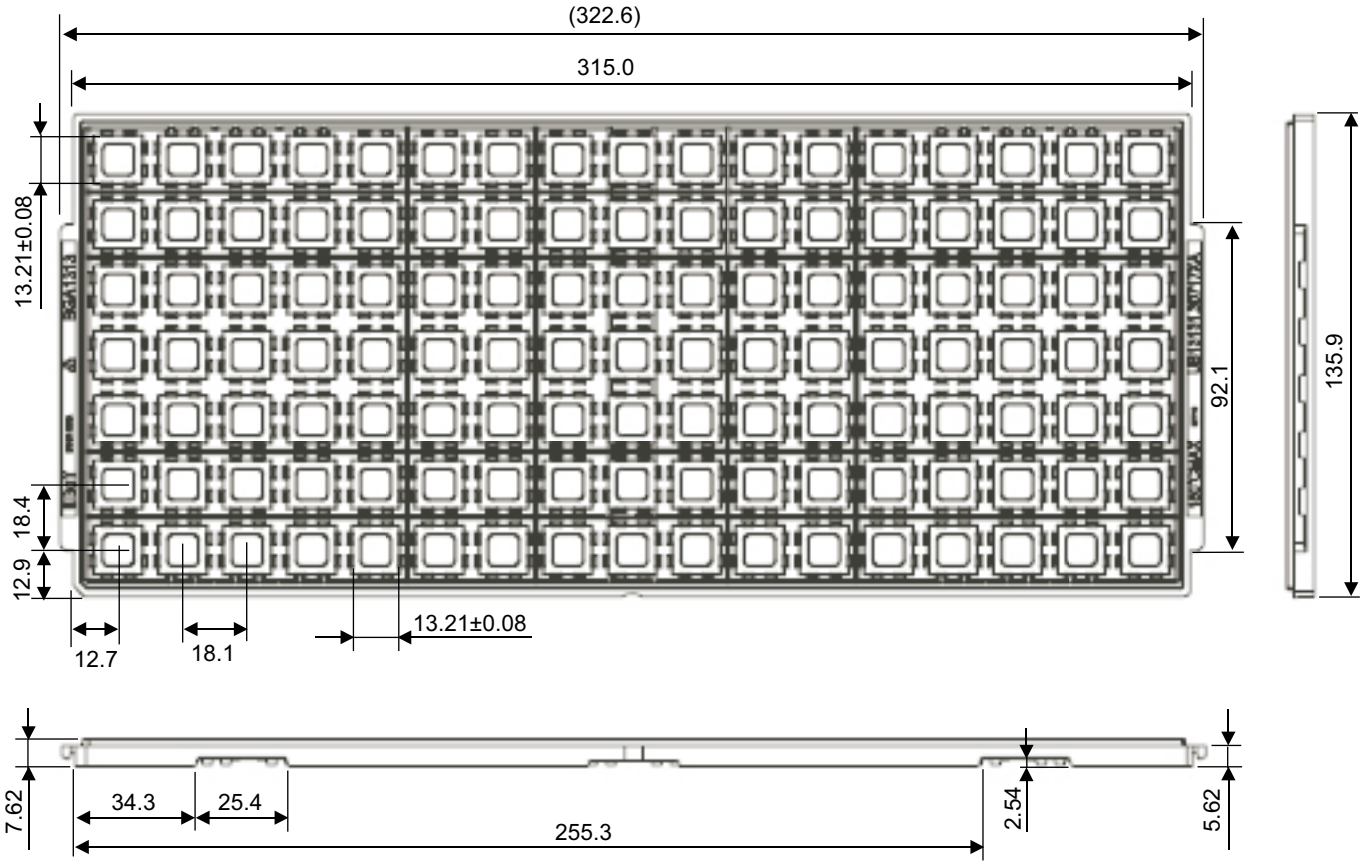
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

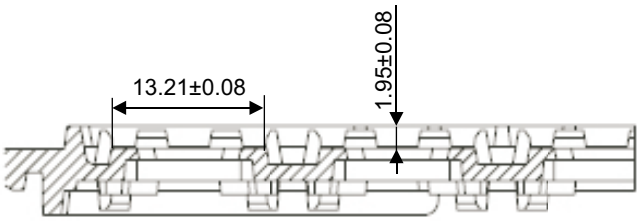




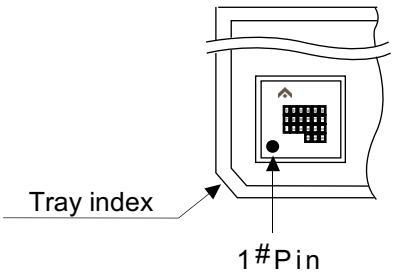
No. RA330-A-P-SD-1.0

TITLE	BGA330-A-PKG Dimensions
No.	RA330-A-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	





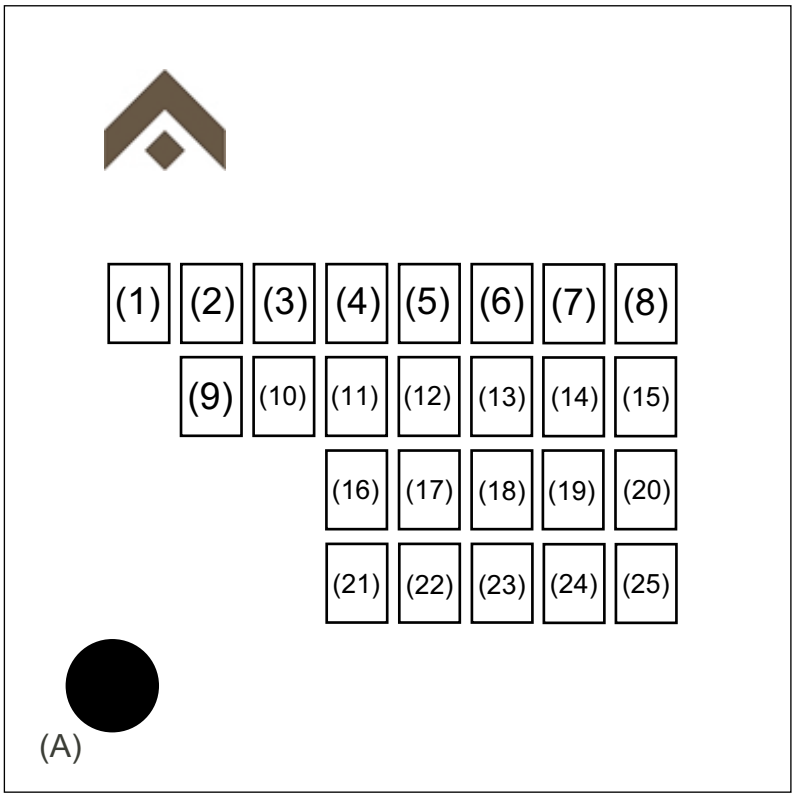
(Direction of IC in tray)



No. RA330-A-T-SD-2.0

TITLE	BGA330-A-Tray		
No.	RA330-A-T-SD-2.0		
ANGLE		QTY.	119
UNIT	mm		

ABLIC Inc.



(1) to (10) : Product code

(11) , (12) : Quality control code

(13) : Year of assembly

(14) : Month of assembly

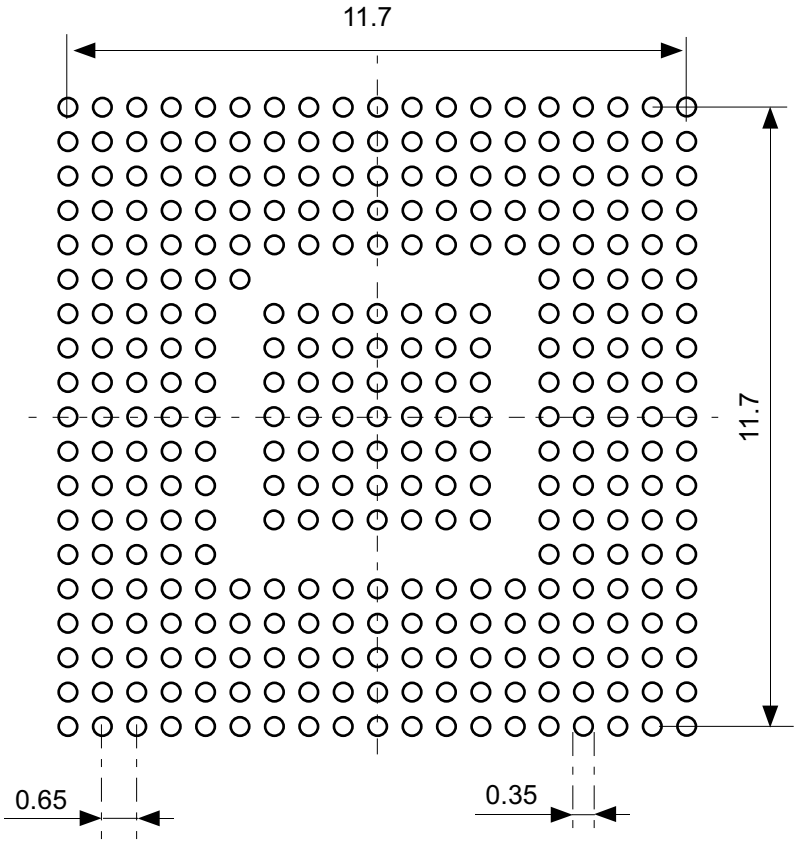
(15) : Week of assembly

(16) to (25) : Quality control code

(A) : 1-pin mark

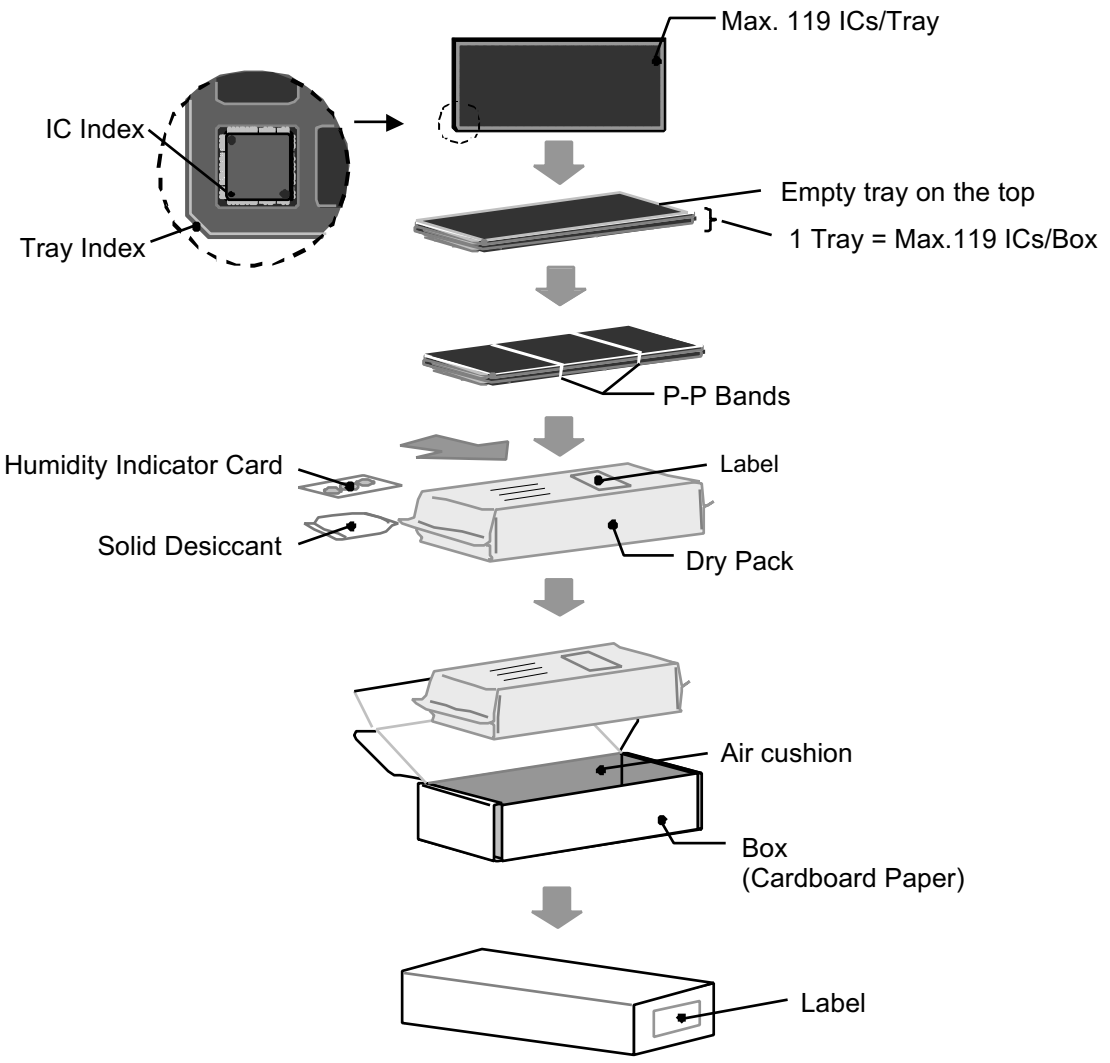
No. RA330-A-M-SD-1.0

TITLE	BGA330-A-Markings		
No.	RA330-A-M-SD-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. RA330-A-L-SD-1.0

TITLE	BGA330-A -Land Recommendation
No.	RA330-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



TITLE	BGA330-A -Packing Procedure
No.	RA330-A-K-SD-1.0
ANGLE	
UNIT	
ABLIC Inc.	

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2.4-2019.07