AMERICAN MICROSYSTEMS, INC.

FS6011-02

Digital Audio/Video Clock Generator IC

July 1998

1.0 Features

- Triple phase-locked loop (PLL) device provides exact ratiometric derivation of Audio, Processor, and Utility Clocks
- On-chip tunable voltage-controlled crystal oscillator (VCXO) allows precise system frequency tuning
- Serial interface for Audio and Utility Clock frequency selection
- Board-programmable Processor Clock frequency selection
- Supports 32, 44.1, and 48kHz 256x oversampled DACs as well as 384x at 44.1kHz and 512x at 48kHz
- Tunable Audio Clock frequencies for undetectable resynchronization of audio and video streams
- Small circuit board footprint (16-pin 0.150″ SOIC)
- Custom frequency selections available - contact your local AMI Sales Representative for more information

2.0 Description

The FS6011-02 is a monolithic CMOS clock generator IC designed to minimize cost and component count in digital video/audio systems.

At the core of the FS6011-02 is circuitry that implements a voltage-controlled crystal oscillator when an external resonator (nominally 27MHz) is attached. The VCXO allows device frequencies to be precisely adjusted for use in systems that have frequency matching requirements, such as digital satellite receivers.

Three high-resolution phase-locked loops independently generate three other selectable frequencies derived from the VCXO frequency. These clock frequencies are related to the VCXO frequency and to each other by exact ratios. The locking of all the output frequencies together can eliminate unpredictable artifacts in video systems and unpredictable electromagnetic interference (EMI) performance due to frequency harmonic stacking.

Figure 1: Block Diagram

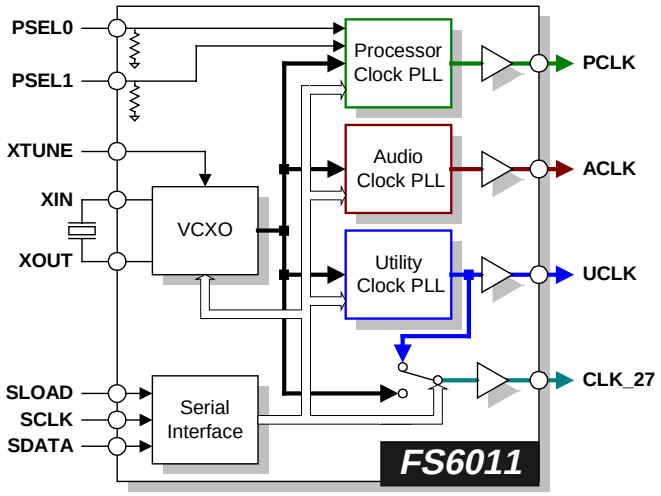
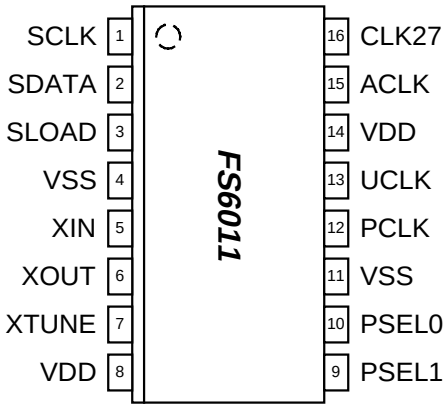


Figure 2: Pin Configuration



16-pin (0.150″) SOIC

Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	DI	SCLK	Serial Data Clock
2	DI	SDATA	Serial Data Input
3	DI	SLOAD	Serial Port Load
4	P	VSS	Ground
5	AI	XIN	VCXO Feedback
6	AO	XOUT	VCXO Drive
7	AI	XTUNE	VCXO Tune
8	P	VDD	Power Supply (+5V)
9	DI_D	PSEL1	PCLK Select MSB
10	DI_D	PSEL0	PCLK Select LSB
11	P	VSS	Ground
12	DO	PCLK	Processor Clock Output
13	DO	UCLK	Utility Clock Output
14	P	VDD	Power Supply (+5V)
15	DO	ACLK	Audio Clock Output
16	DO	CLK27	Reference Clock Output

3.0 Functional Block Description

3.1 Phase-Locked Loops

Each of the three on-chip PLLs in the FS6011 multiplies the reference frequency to the desired frequency by a ratio of integers. This frequency multiplication is exact.

3.2 Output Tristate Control

All four clock outputs of the FS6011 may be tristated to facilitate circuit board testing. To place the outputs in tristate mode, follow this sequence:

1. force XIN low (i.e. ground)
2. apply power to the device
3. wait until the internal power-on reset has deasserted
4. apply a negative-going transition to the PSEL0 pin

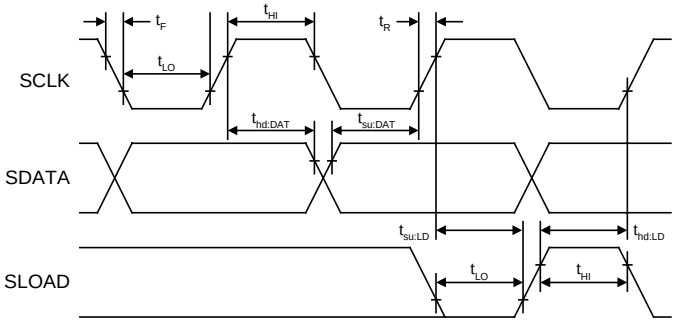
Outputs may be re-enabled by removing and reapplying power to the FS6011. To re-enable outputs without removing power, apply a rising edge transition to the XIN in and follow it with a falling edge transition on the PSEL0 pin.

3.3 Digital Interface

Digital data is placed on the SDATA pin and clocked into the FS6011 internal shift register (D[0] first) with a rising edge on the SCLK pin. The shift register data is transferred to the FS6011 control registers with a rising edge on the SLOAD pin. Fifteen bits must be shifted into the internal registers before the parallel load can be performed. In addition to the normal control functions performed by D[13:0], there is one reserved bit, D[14], that should be set to zero.

All control registers are initialized to zero on power-up.

Figure 3: Communications Protocol



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3.4 Voltage-Controlled Crystal Oscillator (VCXO)

The VCXO provides a tunable, low-jitter frequency reference for the rest of the FS6011 system components. Loading capacitance for the crystal is internal to the FS6011. No external components (other than the resonator itself) are required for operation of the VCXO.

The resonator loading capacitance is adjustable under register control. This permits factory coarse tuning of inexpensive resonators to the necessary precision for digital video applications. Refer to Section 4.6.

Continuous fine-tuning of the VCXO frequency is accomplished by varying the voltage on the XTUNE pin. The total change (from one extreme to the other) in effective loading capacitance is 1.5pF nominal.

The oscillator operates the crystal resonator in the parallel-resonant mode. Crystal warping, or the “pulling” of the crystal oscillation frequency, is accomplished by altering the effective load capacitance presented to the crystal by the oscillator circuit. The actual amount that changing the load capacitance alters the oscillator frequency will be dependent on the characteristics of the crystal as well as the oscillator circuit itself.

Specifically, the motional capacitance of the crystal (usually referred to by crystal manufacturers as C_1), the static capacitance of the crystal (C_0), and the load capacitance (C_L) of the oscillator determine the warping capability of the crystal in the oscillator circuit.

A simple formula to obtain the warping capability of a crystal oscillator is:

$$\Delta f\ (ppm) = \frac{C_1 \times (C_{L2} - C_{L1}) \times 10^6}{2 \times (C_0 + C_{L2}) \times (C_0 + C_{L1})}$$

where C_{L1} and C_{L2} are the two extremes of the applied load capacitance.

A crystal with the following parameters is used. With C_1 = 0.02pF, C_0 = 5pF, C_{L1} = 10pF, and C_{L2} = 22.66pF, the coarse tuning range is

$$\Delta f = \frac{0.02 \times (22.66 - 10) \times 10^6}{2 \times (5 + 22.66) \times (5 + 10)} = 305\,ppm.$$

4.0 Programming Information

Table 2: Register Summary

BIT D[x]	REGISTER BIT DESCRIPTION	
0	ACLK Select (LSB)	
1	ACLK Select	
2	ACLK Select (MSB)	
3	ACLK Off-Speed Mode	
	Bit = 0	Disable Off-Speed Mode
	Bit = 1	Enable Off-Speed Mode
4	ACLK Speed Control	
	Bit = 0	Low Speed
	Bit = 1	High Speed
5	UCLK Select (LSB)	
6	UCLK Select	
7	UCLK Select (MSB)	
8	CLK27 Select	
	Bit = 0	Selects VCXO Frequency
	Bit = 1	Selects UCLK Frequency
9	Crystal Oscillator Coarse Tune (LSB)	
10	Crystal Oscillator Coarse Tune	
11	Crystal Oscillator Coarse Tune	
12	Crystal Oscillator Coarse Tune (MSB)	
13	VCXO Enable/Disable Control	
	Bit = 0	Disable VCXO Mode
	Bit = 1	Enable VCXO Mode
14	Reserved (should be set to 0)	

4.1 Audio PLL Clock Frequencies (ACLK)

The ACLK frequency is controlled by register bits D[0], D[1], and D[2] accessed via the serial interface. The ACLK frequencies listed below are derived via the PLL Divider Ratio from a reference frequency of 27MHz.

Table 3: ACLK Frequency Select

D[2]	D[1]	D[0]	PLL DIVIDER RATIO	AUDIO OVERSAMPLING	ACLK (MHz)
0	0	0	1024 / 2250	48kHz x 256	12.288
0	0	1	1024 / 3375	32kHz x 256	8.192
0	1	0	1024 / 4500	48kHz x 256 / 2	6.144
0	1	1	1024 / 6750	32kHz x 256 / 2	4.096
1	0	0	1568 / 3750	44.1kHz x 256	11.2896
1	0	1	1568 / 2500	44.1kHz x 384	16.9344
1	1	0	1568 / 7500	44.1kHz x 256 / 2	5.6448
1	1	1	1024 / 1125	48kHz x 512	24.576

NOTE: Contact AMI for custom PLL frequencies

4.2 Audio Clock Off-Speed Frequencies

The ACLK frequencies shown may be smoothly modified to a slightly higher or lower value under register control. Register bit D[3] must be a logic-one to activate this mode. The value of D[4] controls whether the frequency will be adjusted slightly low (D[4] = 0) or high (D[4] = 1).

Table 4: Audio Off Speed Frequencies

D[4]	D[3]	D[2]	D[1]	D[0]	PLL DIVIDER RATIO	ACLK (MHz)
0	1	0	0	0	1023 / 2250	12.276
0	1	0	0	1	1023 / 3375	8.184
0	1	0	1	0	1023 / 4500	6.138
0	1	0	1	1	1023 / 6750	4.092
0	1	1	0	0	1567 / 3750	11.2824
0	1	1	0	1	1567 / 2500	16.9236
0	1	1	1	0	1567 / 7500	5.6412
0	1	1	1	1	1023 / 1125	24.5520
1	1	0	0	0	1025 / 2250	12.3000
1	1	0	0	1	1025 / 3375	8.2000
1	1	0	1	0	1025 / 4500	6.1500
1	1	0	1	1	1025 / 6750	4.1000
1	1	1	0	0	1569 / 3750	11.2968
1	1	1	0	1	1569 / 2500	16.9432
1	1	1	1	0	1569 / 7500	5.6484
1	1	1	1	1	1025 / 1125	24.6000

4.3 Utility PLL Clock Frequencies (UCLK)

The UCLK frequency is controlled by register bits D[5], D[6] and D[7], accessed via the serial interface. UCLK frequencies listed below are derived via the PLL Divider Ratio from a reference frequency of 27MHz.

Table 5: UCLK Frequency Select

D[7]	D[6]	D[5]	PLL DIVIDER RATIO	UCLK (MHz)
0	0	0	16 / 27	16.0000
0	0	1	35 / 33	28.6363
0	1	0	1568 / 3750	11.2896
0	1	1	1	27.0000
1	0	0	544 / 375	39.1680
1	0	1	728 / 375	52.4160
1	1	0	10 / 9	30.0000
1	1	1	1024 / 1125	24.5760

NOTE: Contact AMI for custom PLL frequencies

4.4 Processor PLL Frequencies (PCLK)

The PCLK frequency is controlled by the logic levels on the PSEL0 and PSEL1 inputs. These inputs have weak pull-downs. PCLK frequencies listed below are derived via the PLL Divider Ratio from a reference frequency of 27MHz.

Table 6: PCLK Frequency Select

PSEL1	PSEL0	PLL DIVIDER RATIO	PCLK (MHz)
0	0	32 / 27	32.0000
0	1	40 / 27	40.0000
1	0	50 / 27	50.0000
1	1	60 / 41	39.5122

NOTE: Contact AMI for custom PLL frequencies

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4.5 Reference Frequencies (CLK27)

The CLK27 output frequency is controlled by register bit D[8] that selects either the VCXO reference frequency or the UCLK frequency.

Table 7: CLK27 Frequency Select

D[8]	CLK27 Output
0	VCXO Frequency
1	UCLK Frequency

4.6 VCXO Coarse Tuning and Enable

The VCXO may be coarse tuned by a programmable adjustment of the crystal load capacitance via D[12:9]. The actual amount of frequency warping caused by the tuning capacitance will depend on the crystal used. The VCXO tuning capacitance includes an external 6pF load capacitance (12pF from the XIN pin to ground and 12pF from the XOUT pin to ground).

The fine tuning capability of the VCXO can be enabled by setting D[13] to a logic-one or disabled by clearing the bit to a logic-zero.

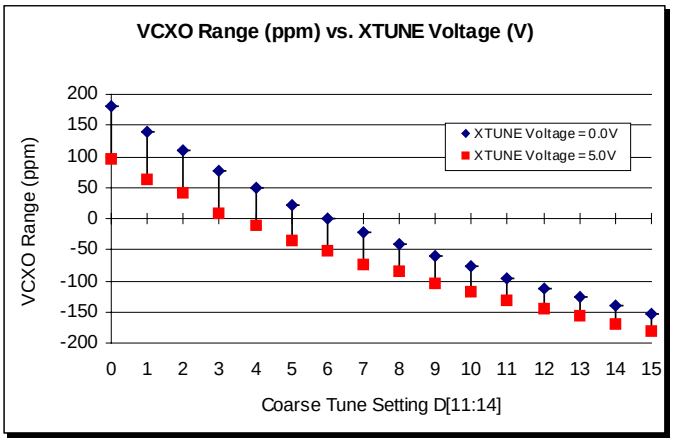
Table 8: VCXO Tuning Capacitance

D[12]	D[11]	D[10]	D[9]	VCXO TUNING CAPACITANCE (pF)
0	0	0	0	10.00
0	0	0	1	10.84
0	0	1	0	11.69
0	0	1	1	12.53
0	1	0	0	13.38
0	1	0	1	14.22
0	1	1	0	15.06
0	1	1	1	15.91
1	0	0	0	16.75
1	0	0	1	17.59
1	0	1	0	18.43
1	0	1	1	19.28
1	1	0	0	20.13
1	1	0	1	20.97
1	1	1	0	21.81
1	1	1	1	22.66

Figure 4 shows the typical effect of the coarse and fine tuning mechanisms. The difference in VCXO frequency in parts-per-million (ppm) is shown as the fine tuning voltage on the XTUNE pin varies from 0V to 5V. The coarse tune range as shown is about 350ppm. As the crystal load capacitance is increased (with increasing Coarse Tune setting) the frequency is pulled somewhat less with each coarse step and the fine tuning range decreases.

The fine tuning range always overlaps a few coarse tuning ranges, eliminating the possibility of holes in the VCXO response. Note that different crystal warping characteristics will change the scaling on the Y-axis, but not the overall characteristic of the curves.

Figure 4: VCXO Coarse and Fine Tuning



5.0 Electrical Specifications

Table 9: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (human-body model)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 10: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	5V ± 10%	4.5	5	5.5	V
Ambient Operating Temperature Range	T_A		0		70	°C
Output Load Capacitance	C_L				15	pF
Crystal Resonator Frequency	f_{XIN}		24	27	28	MHz
Crystal Resonator Motional Capacitance	C_{MOT}	AT cut		25		fF
Serial Data Transfer Rate			10		100	kb/s

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Table 11: DC Electrical Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{CLK} = 27MHz; $C_L \approx$ 50pF		58	80	mA
Serial Communication Inputs (SCLK, SDATA, SLOAD)						
High-Level Input Voltage	V_{IH}		2.4		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Hysteresis Voltage	V_{hys}				300	mV
Input Leakage Current	I_I		-1		1	µA
PCLK Select Inputs (PSEL0, PSEL1)						
High-Level Input Voltage	V_{IH}		2.4		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
High-Level Input Current (pull-down)	I_{IH}	V_{IH} = 5V	5	12.7	50	µA
Low-Level Input Current	I_{IL}		-1		1	µA
Crystal Oscillator Feedback (XIN)						
Threshold Bias Voltage *	V_{TH}			0.5V_{DD}		V
Input Leakage Current	I_I		-1		1	µA
Crystal Loading Capacitance *	$C_{L(xtal)}$	As seen by an external crystal connected to XIN and XOUT; VCXO tuning disabled		10		pF
Input Loading Capacitance *	$C_{L(XIN)}$	As seen by an external clock driver on XIN; XOUT unconnected; VCXO disabled		20		pF
Crystal Oscillator Drive (XOUT)						
High-Level Output Source Current *	I_{OH}	V_O = 0V; D[13] = 0		-45		mA
		V_O = 0V, V(XTUNE) = 5V; D[13] = 1		-52		
Low-Level Output Sink Current *	I_{OL}	V_O = 5V; D[13] = 0		53		mA
		V_O = 5V, V(XTUNE) = 5V; D[13] = 1		63		
VCXO Tuning Input (XTUNE)						
Input Leakage Current	I_I		-1		1	µA
Clock Outputs (ACLK, CLK27, PCLK, UCLK)						
High-Level Output Source Current *	I_{OH}	V_O = 2.4V		-46		mA
Low-Level Output Sink Current *	I_{OL}	V_O = 0.4V		64		mA
Output Impedance *	z_{OH}	V_O = 0.5V_{DD}; output driving high		53		Ω
	z_{OL}	V_O = 0.5V_{DD}; output driving low		57		
Tristate Output Current	I_{OZ}		-10		+10	µA
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-60		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 5V; shorted for 30s, max.		65		mA

Table 12: AC Timing Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Output (ACLK)							
Duty Cycle *		From rising edge to rising edge at 2.5V	12.288	48		52	%
			8.192	48		52	
			6.144	48		52	
			4.096	48		52	
			11.289	47		52	
			16.344	48		52	
			5.644	48		52	
			24.576	47		51	
Jitter, Absolute (long term) *	$t_{j(ab)}$	Measured from rising edge to 1st rising edge after 0.1s at 2.5V; C_L = 15pF, f_{REF} = 27MHz	12.288		740		ps
			8.192		760		
			6.144		730		
			4.096		710		
			11.289		650		
			16.344		570		
			5.644		680		
			24.576		730		
Jitter, Period *	$t_{j(\Delta P)}$	Measured on the rising edges at 2.5V; C_L = 15pF, f_{REF} = 27MHz	12.288		370		ps
			8.192		270		
			6.144		190		
			4.096		140		
			11.289		470		
			16.344		680		
			5.644		240		
			24.576		770		
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.5		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.3		ns
Clock Stabilization Time *	t_{STB}	Output active from power-up			740		µs

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Table 13: AC Timing Specifications, continued

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Output (UCLK)							
Duty Cycle *		From rising edge to rising edge at 2.5V	16.000	48		52	%
			28.636	48		52	
			11.289	48		52	
			27.000	44		48	
			39.168	43		47	
			52.416	42		46	
			30.000	48		52	
			24.576	48		52	
Jitter, Absolute (long term) *	$t_{j(ab)}$	Measured from rising edge to 1st rising edge after 0.1s at 2.5V; C_L = 15pF, f_{REF} = 27MHz	16.000		580		ps
			28.636		620		
			11.289		780		
			27.000		2800		
			39.168		640		
			52.416		780		
			30.000		650		
			24.576		680		
Jitter, Period *	$t_{j(\Delta P)}$	Measured on the rising edges at 2.5V; C_L = 15pF, f_{REF} = 27MHz	16.000		250		ps
			28.636		400		
			11.289		400		
			27.000		900		
			39.168		670		
			52.416		1500		
			30.000		790		
			24.576		680		
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.6		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.4		ns
Clock Stabilization Time *	t_{STB}	Output active from power-up			380		µs

Table 14: AC Timing Specifications, continued

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
Clock Output (PCLK)							
Duty Cycle *		From rising edge to rising edge at 2.5V	32.000	48		52	%
			40.000	48		52	
			50.000	48		52	
			39.512	48		52	
Jitter, Absolute (long term) *	$t_{j(ab)}$	Measured from rising edge to 1st rising edge after 0.1s at 2.5V; C_L = 15pF, f_{REF} = 27MHz	32.000		410		ps
			40.000		620		
			50.000		630		
			39.512		620		
Jitter, Period *	$t_{j(\Delta P)}$	Measured on the rising edges at 2.5V; C_L = 15pF, f_{REF} = 27MHz	32.000		430		ps
			40.000		460		
			50.000		530		
			39.512		670		
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.6		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.4		ns
Clock Stabilization *	t_{STB}	Output active from power-up			400		µs
Clock Output (CLK27)							
Duty Cycle *		Crystal oscillator frequency out, from rising edge to rising edge at 2.5V	27	44		48	%
Clock Stabilization Time *	t_{STB}	Output active from power-up			150		µs
Rise Time *	t_r	V_O = 0.5V to 4.5V; C_L = 15pF			3.8		ns
Fall Time *	t_f	V_O = 4.5V to 0.5V; C_L = 15pF			2.9		ns

Table 15: Serial Interface Timing Specifications

Unless otherwise stated, V_{DD} = 5.0V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	MAX.	UNITS
SCLK clock frequency	f_{SCLK}		0	100	kHz
Set up time, load	$t_{su:LD}$	SLOAD	4.7		µs
Hold time, load	$t_{hd:LD}$	SLOAD	4.0		µs
Set up time, data	$t_{su:DAT}$	SDATA	250		ns
Hold time, data	$t_{hd:DAT}$	SDATA	0		µs
Rise time	t_r	SDATA, SCLK		1000	ns
Fall time	t_f	SDATA, SCLK		300	ns
High time, serial clock	t_H	SCLK	4.0		µs
Low time, serial clock	t_L	SCLK	4.7		µs

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6.0 Package Information

Table 16: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

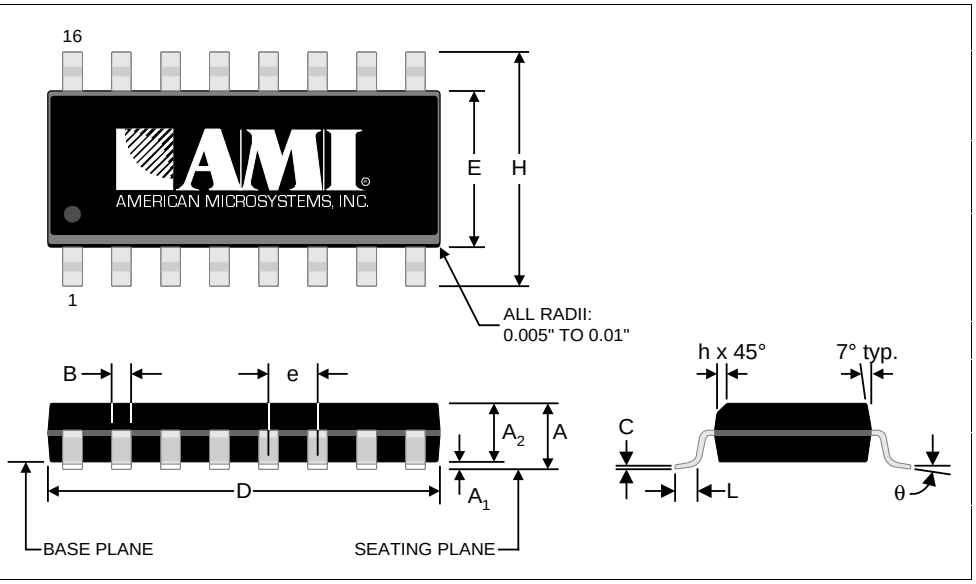

Table 17: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{jA}	Air flow = 0 m/s	108	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

7.0 Ordering Information

ORDERING CODE	DEVICE NUMBER	FONT	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11228-003	FS6011	-02	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tube
11228-005	FS6011	-02	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape-and-Reel

American Microsystems, Inc., 2300 Buckskin Rd., Pocatello, ID 83201, (208) 233-4690, FAX (208) 234-6796, WWW Address: http://www.amis.com E-mail: tgp@amis.com

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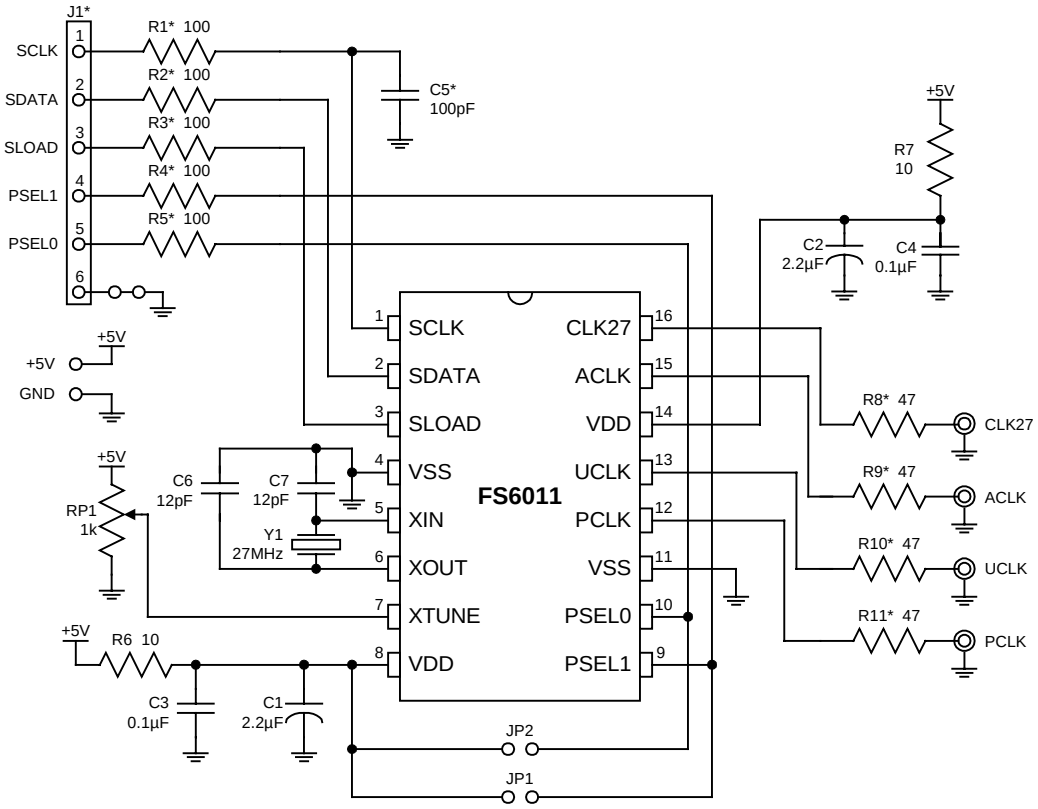
8.0 Demonstration Board

A simple demonstration board and DOS-based software is available from American Microsystems that illustrates the capabilities of the FS6011. The board schematic is shown below. Components listed with an asterisk (*) are not required in an actual application, and are used here to preserve signal integrity with the cabling associated with the board. A cabled interface between a computer parallel port (DB25 connector) and the board (J1) is provided.

Contact your local sales representative or the company directly for more information.

Figure 5: Board Schematic



8.1 Contents

- Demonstration board
- Interface cable (DB25 to 6-pin connector)
- Data sheet
- Demonstration software, including:
  - INSTALL.BAT 0.75kB
  - FS6011.BAT 0.24kB
  - FS6011G.BAS 5.3kB

8.2 Requirements

- PC running MS-DOS or MS Windows 3.1x, with accessible parallel (LPT1) port
- MS-QBasic v. 1.1 or later (or equivalent software)
- 6.3kB available space on drive C:

8.3 Board Setup and Software Installation Instructions

1. At the appropriate disk drive prompt (A:\) type **Install** to automatically copy demo files to the C: drive. NOTE: This demo software requires Microsoft QBasic or equivalent to run. Make sure the directory containing qbasic.exe is in the DOS path statement, or move the demo files to a directory containing Basic.
2. Connect a +5 Volt power supply to the board: RED = +5V, BLACK = ground.
3. Remove all software keys from the computer parallel port.
4. Connect the supplied interface cable to the parallel port (DB25 connector) and to the demo board (6-pin connector). Make sure the cable is facing away from the board – pin 1 is the red wire.
5. Connect the clock outputs to the target application board with a twisted-pair cable.

8.4 Demo Program

1. Type **FS6011** at the C:\FS6011 prompt to run the Qbasic-based demo program.
2. The following banner should appear:

```
**************************************
*                                    *
*        FS6011 Utility Program      *
*                                    *
*    PRESS ANY KEY TO CONTINUE.....  *
*                                    *
**************************************
```

3. After pressing any key, a menu should appear containing a list of the program hot keys, a message that the computer parallel (LPT1) port was found, and the address at which the port was found.

```
        ************************
        * FS6011 Pgm. Utility  *
        *                      *
        * chip (R)efresh       *
        * chip (I)nitialize    *
        * (A)clk          =  0 *
        * a(O)ffset       =  0 *
        * (C)lk27         =  0 *
        * (U)clk          =  0 *
        * (V)cxo          =  0 *
        * vcxo (E)nable   =  0 *
        * (P)clk          =  0 *
        * e(X)it               *
        ************************
```

Refer to Table 18 for a description of each hot key.

4. To change the frequency of the desired clock, press the appropriate hot key. The keys are *not* case sensitive.
5. Refer (in the FS6011 data sheet) to Table 3 and Table 4 for ACLK frequencies, Table 5 for UCLK frequencies, and Table 6 for PCLK frequencies.
6. Observe the response to the hot key selection. Repeated pressing of the same key will scroll through the entire range of frequencies for the selected clock, returning to the initial frequency.
7. Pressing a hot key strobes a 15-bit message to the demo board via the interface cable. The response to the key selection is shown below:

```
Writing...
(0x000) Binary: LSB 000000000000000 MSB
```

where the numbers are the data in hex and binary.

Note that the PCLK frequency is changed by directly addressing pins 4 and 5 (PSEL0 and PSEL1) of the device. Therefore the hot key response message will be unchanged when selecting the (**P**)CLK hot key. Press **X** to exit the demo program.

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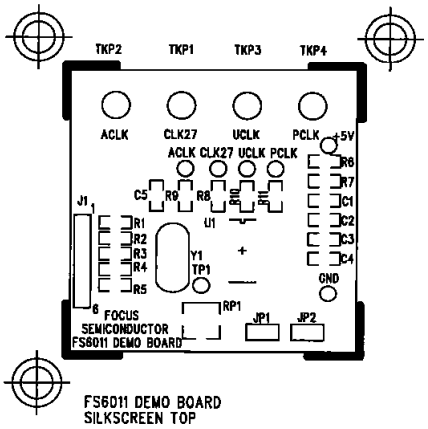
Table 18: Hot Key Description

Command	Hot Key	Bits	Range	Description
Refresh	R			Reloads the register bit values into the device
Initialize	I			Initializes all register bit values to zero (default setting)
ACLK	A	0-2	000-111	Cycles through ACLK frequencies (Table 3)
ACLK Offset	O	3-4	00-11	Bit 3 enables or disables off-speed mode; Bit 4 adjusts ACLK off-speed high or low
UCLK	U	5-7	000-111	Cycles through UCLK frequencies (Table 5)
CLK27	C	8	0-1	Switches the CLK27 output between the VCXO and UCLK frequency
VCXO	V	9-12	0000-1111	Digital Coarse tune adjustment of the VCXO
VCXO Enable	E	13	0-1	Enables fine tune of the VCXO via the XTUNE pin
PCLK	P	-	00-11	Cycles through PCLK frequencies via PSEL0 and PSEL1 pins (Table 6)
Exit	X			Exits the demo program

Table 19: Cable Interface

Color	J1	DB25	Signal
Red	1	2	SCLK
White	2	16	SDATA
Green	3	8	SLOAD
Blue	4	5	PSEL1
Brown	5	4	PSEL0
Black	6	25	GND

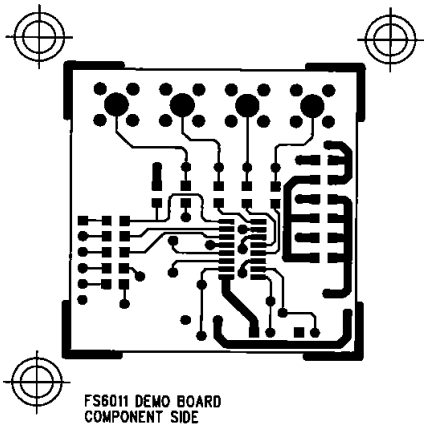
Figure 6: Board Silkscreen



FS6011 DEMO BOARD
SILKSCREEN TOP

Figure 7: Board Traces - Component Side

Left

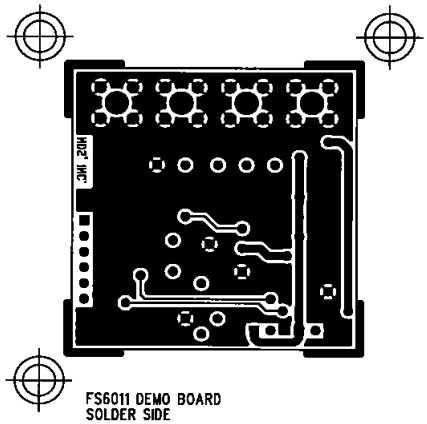


Right

FS6011 DEMO BOARD
COMPONENT SIDE

Figure 8: Board Traces - Solder Side

Right



Left

FS6011 DEMO BOARD
SOLDER SIDE