

# High efficiency、Low noise、Constant large volume、Multi-level AGC Eighth generation Class K Audio Amplifier

## FEATURES

- ◆ Multi-Level AGC audio algorithm , effectively eliminate noise, make sound pure natural
- ◆ Low noise: 43 $\mu$ V
- ◆ Ultra-low distortion: 0.008%
- ◆ Power amplifier overall efficiency is up to 83%
- ◆ Speaker and Receiver two-in-one application
  - ◆ Receiver: 1V/V, Vn=19 $\mu$ V, THD+N=0.025%
  - ◆ Receiver: 3V/V, Vn=22 $\mu$ V, THD+N=0.025%
- ◆ Selectable speaker-guard power level : 0.6W, 0.7W, 0.8W, 0.9W, 1W, 1.1W, 1.2W
- ◆ Within Lithium battery voltage range, maintained constant large volume
- ◆ Support 6ohm speaker
- ◆ Compatible with AW8736, AW8737
- ◆ Super TDD-Noise suppression
- ◆ Excellent pop-click suppression
- ◆ One wire pulse control
- ◆ High PSRR: -68dB (217Hz)
- ◆ ESD protection:  $\pm$ 6kV (HBM)
- ◆ Small 0.4mm pitch 1.6mm $\times$ 1.68mm CSP-14package

## APPLICATIONS

- ◆ Smart phone

## DESCRIPTION

AW87318 is specifically designed to eliminate smart mobile phone music noise, to enhance overall sound quality, which is a new high efficiency, low noise, ultra-low distortion, constant large volume, upgrading eighth generation class K audio amplifiers. AW87318 integrated Awinic proprietary multi-level AGC audio algorithm, effectively eliminate music noise, improve sound quality and volume. Using a new generation K-Chargepump technology, efficiency reaches 93%, power amplifier's overall efficiency reaches 83%, greatly prolong the mobile phone usage time. AW87318 noise floor is as low as to 43 $\mu$ V, with 98.8dB high signal-to-noise-ratio(SNR). The ultra-low distortion 0.008% and unique multi-level AGC technology brings high quality music enjoyment.

AW87318 has 0.6W,0.7W,0.8W,0.9W,1W,1.1W and 1.2W seven subdivision selectable speaker-guard output power levels, which is suitable for different rated power speakers. With multi-level AGC audio algorithms, the music is pure natural and melodious. Within lithium battery voltage range (3.3V--4.35V), output power is constant, preventing voice becomes smaller and smaller during usage of cell phone.

AW87318 supports speaker and receiver two-in-one application. In receiver mode, the output noise is as low as to 19 $\mu$ V, amplifier is in class D mode, powered by VBAT.

AW87318 has built-in over current protection, over-temperature protection and short circuit protection function, effectively protect the chip. AW87318 uses small 0.4mm pitch 1.6mm $\times$ 1.68mm CSP-14 package.

## APPLICATION DIAGRAM

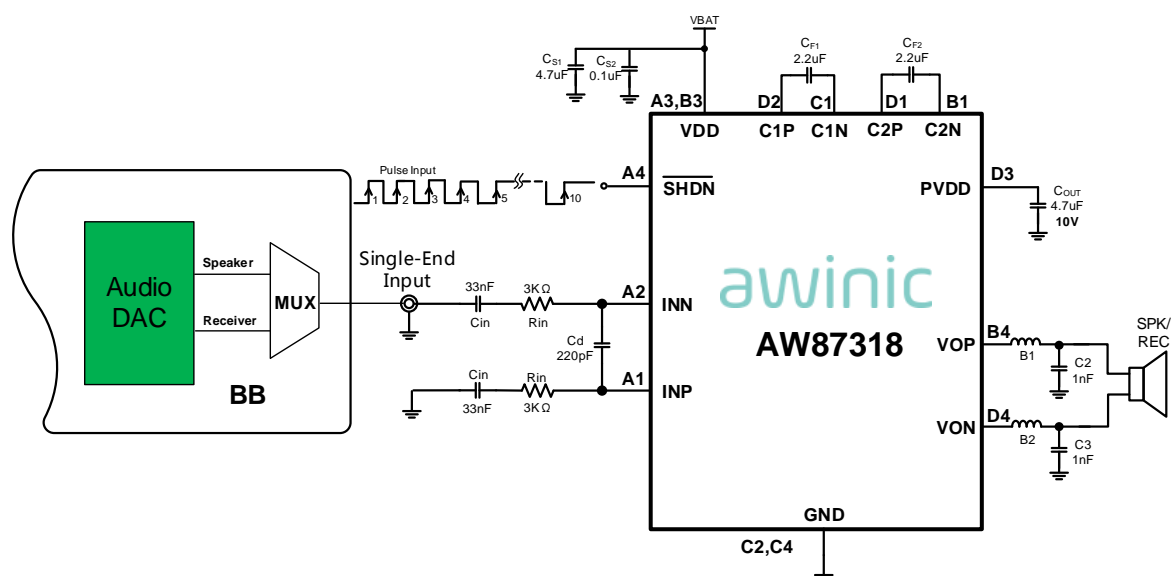


Figure1 AW87318 application diagram

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## PIN CONFIGURATION AND TOP MARK

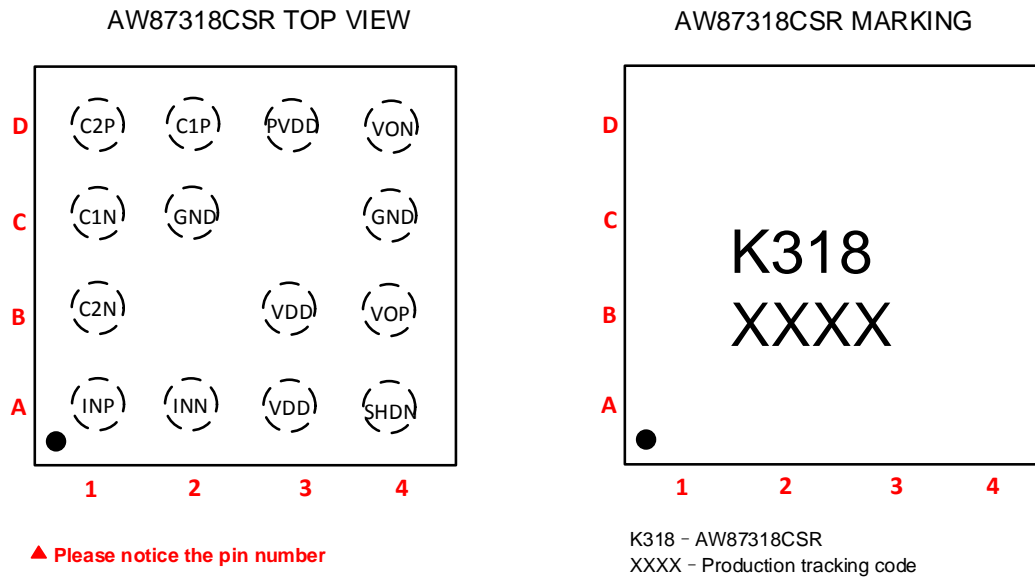


Figure 2 AW87318 pin diagram top view and device marking

## PIN DESCRIPTION

Number	Symbol	Description
A1	INP	Positive audio input terminal
A2	INN	Negative audio input terminal
A3	VDD	Power supply
A4	SHDN	Chip power down pin, active low; one wire pulse control;
B1	C2N	Negative side of the external charge pump flying capacitor C2
B3	VDD	Power supply
B4	VOP	Positive audio output terminal
C1	C1N	Negative side of the external charge pump flying capacitor C1
C2, C4	GND	Ground
D1	C2P	Positive side of the external charge pump flying capacitor C2
D2	C1P	Positive side of the external charge pump flying capacitor C1
D3	PVDD	Boost charge pump output voltage
D4	VON	Negative audio output terminal

## AWINIC CLASS K FAMILY

ITEM	TEST CONDITION	AW8736	AW8737	AW87317	AW8738	AW87318
PVDD(V)	VDD=4.2V	5.8	6.05	6.05	6.05	6.05
Ouput noise( $\mu$ V)	VDD=4.2V, f=20Hz to 20kHz, input ac grounded, 8V/V,A-weighting	125	52	53	40	43
Efficiency(%)	V <sub>DD</sub> =3.6V, P <sub>O</sub> =1.0W, R <sub>L</sub> =8 $\Omega$ +33 $\mu$ H	75	80	80	83	83

FUNCTIONAL DIAGRAM

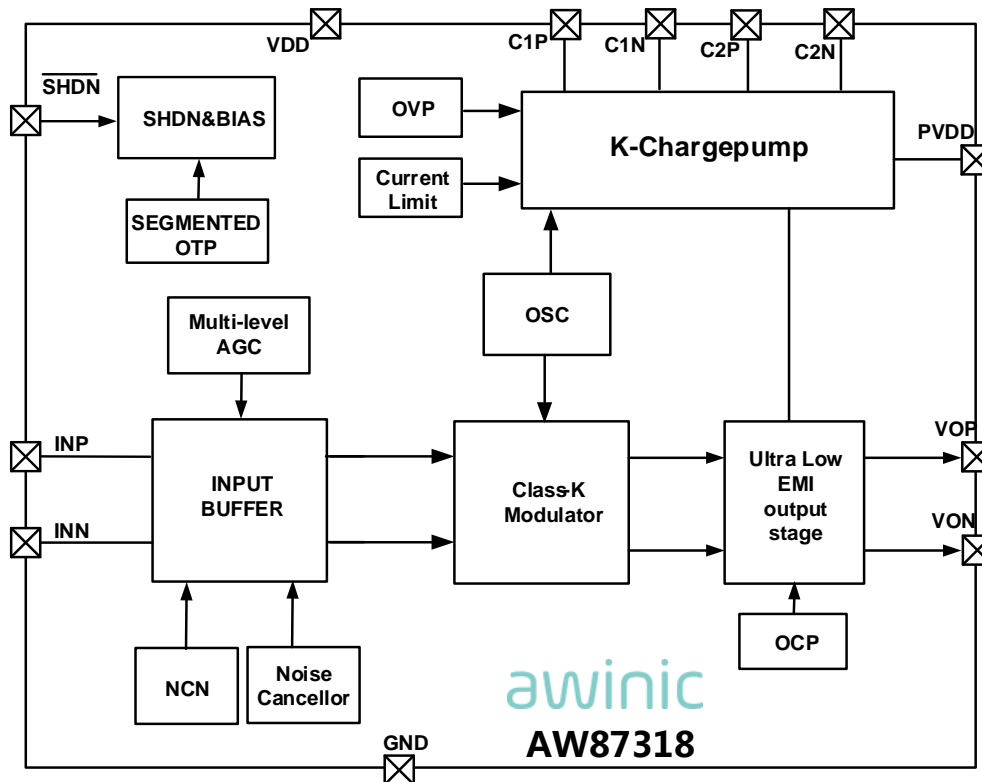


Figure 3 AW87318 functional diagram

APPLICATION DIAGRAM

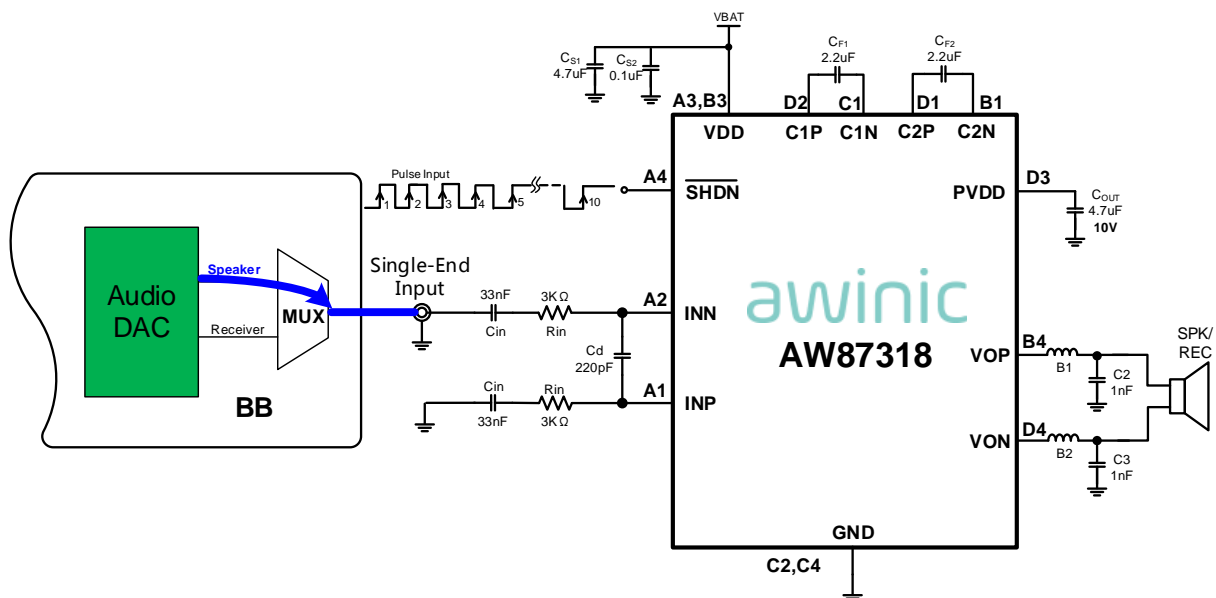


Figure 4 AW87318 speaker mode application diagram (Note 1)

**Note1:** when single-ended input, input audio signal can arbitrarily connect to one of INN, INP input terminal, the other terminal connects to ground through input capacitor and resistance.

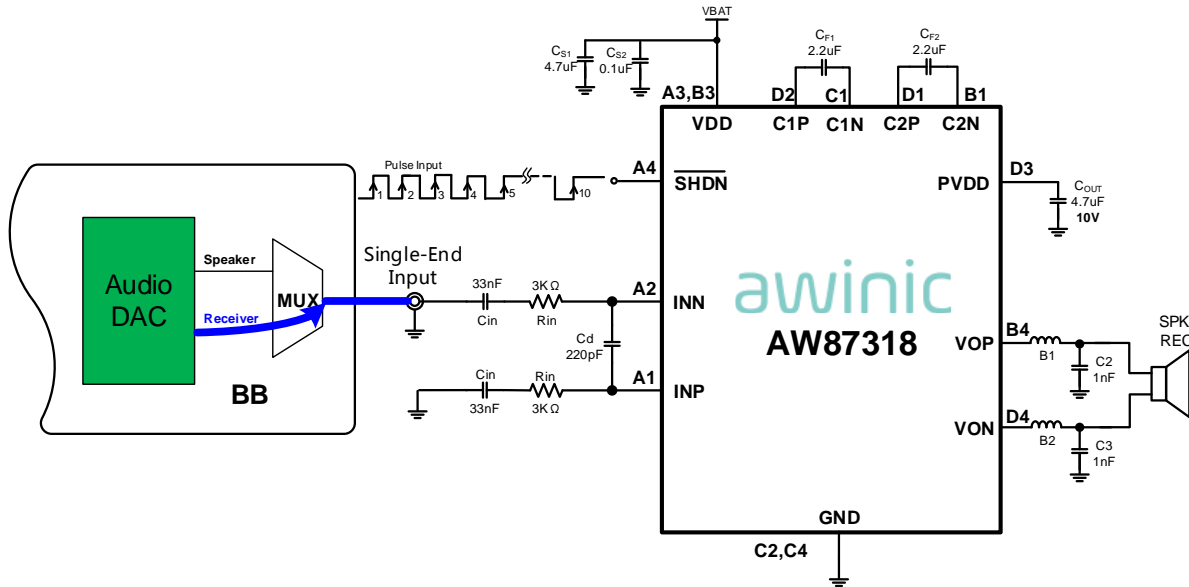
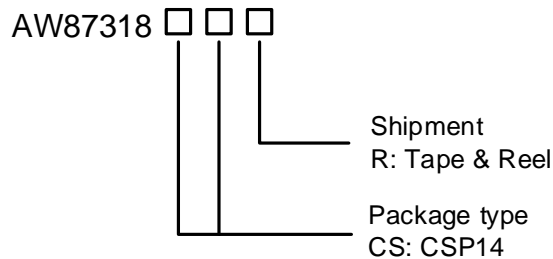


Figure 5 AW87318 receiver mode application diagram

## ORDERING INFORMATION

Product Type	Operation temperature range	Package	Device Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW87318CSR	-40°C~85°C	CSP-14	K318	MSL1	ROHS+HF	Tape and Reel 3000 pcs



## ABSOLUTE MAXIMUM RATING (Note2)

Parameter	Range
Supply Voltage VDD	-0.3V to 6V
Chargepump output voltage PVDD	-0.3V to 7V
VOP,VON	-0.3V to PVDD+0.3V
C1P ,C2P	-0.3V to PVDD+0.3V
C1N,C2N	-0.3V to VDD+0.3V
INP, INN Input Pin Voltage	-0.3V to VDD +0.3V
Package Thermal Resistance $\theta_{JA}$	84.9°C/W

Ambient Temperature Range	-40°C to 85°C
Maximum Junction Temperature T <sub>JMAX</sub>	165°C
Storage Temperature Range T <sub>STG</sub>	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating <sup>(Note 3)</sup>	
HBM (human body model)	±6KV
CDM	±1.5KV
MM	±250V
Latch-up	
Test Condition: JEDEC STANDARD NO.78D NOVEMBER 2011	+IT: 450mA -IT: -450mA

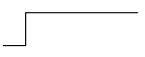

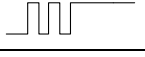





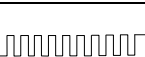
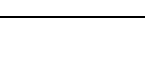
**Note 2:** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**Note 3:** The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883H Method 3015.8

## MODE DESCRIPTION (TA=25°C, VDD=4.2V)

AW87318 audio amplifier outer input capacitor is Cin, outer input resist is Rin, inner input resist is 6.6KΩ, gain Av is 159.5K/(Rin+6.6K). Recommended typical application is:

- 1、Cin=33nF, Rin=3KΩ, Av=16.6V/V;

MODE	Enable Signal	Gain (V/V)	AGC Power (W)				Multi-Level AGC Function	Receiver Mode
			RL=8Ω +33μH	RL=6Ω +33μH	RL=4Ω +15μH	RL=3Ω +15μH		
MODE1		16.6	1.2	1.6	—	—	√	
MODE2		16.6	1.1	1.5	—	—	√	
MODE3		16.6	1.0	1.3	2.0	—	√	
MODE4		16.6	0.9	1.2	1.8	—	√	
MODE5		16.6	0.8	1.0	1.6	2.0	√	
MODE6		16.6	0.7	0.9	1.4	1.8	√	
MODE7		16.6	0.6	0.8	1.2	1.6	√	
MODE8		1						√
MODE9		3						√
MODE10		16.6	1.75W@ THD=1%	2.05W@ THD=1%	2.4W@ THD=1%	2.35W@ THD=1%		

## ELECTRICAL CHARACTERISTICS

Test condition:  $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=3.6\text{V}$ ,  $R_L=8\Omega+33\mu\text{H}$ ,  $f=1\text{kHz}$  (unless otherwise noted)

Parameter		Test conditions	Min	Typ	Max	Units
$V_{DD}$	Power supply voltage		3.0		5.5	V
$V_{IH}$	$\overline{\text{SHDN}}$ high input voltage		1.3		$V_{DD}$	V
$V_{IL}$	$\overline{\text{SHDN}}$ low input voltage		0		0.35	V
$ V_{OS} $	Output offset voltage	$V_{in}=0\text{V}$ , $V_{DD}=3.0\text{V}$ to $5.5\text{V}$	-30	0	30	mV
$I_{SD}$	Shutdown current	$V_{DD}=3.6\text{V}$ , $\overline{\text{SHDN}}=0\text{V}$			1	$\mu\text{A}$
$T_{TG}$	Thermal AGC start temperature threshold			150		$^{\circ}\text{C}$
$T_{TGR}$	Thermal AGC exit temperature threshold			130		$^{\circ}\text{C}$
$T_{SD}$	Over temperature protection threshold			160		$^{\circ}\text{C}$
$T_{SDR}$	Over temperature protection recovery threshold			120		$^{\circ}\text{C}$
$T_{ON}$	Start-up time			40		ms
<b>K-Chargepump</b>						
PVDD	Output voltage	$V_{DD}=3.0\text{V}$ to $4\text{V}$		1.5* VDD		V
		$V_{DD}>4\text{V}$		6.05		V
$V_{HYS}$	OVP hysteresis	$V_{DD}>4\text{V}$		50		mV
$F_{CP}$	Charge Pump frequency	$V_{DD}=3.0\text{V}$ to $5.5\text{V}$	0.8	1.06	1.33	MHz
$\eta_{CP}$	Charge pump efficiency	$V_{DD}=3.6\text{V}$ , $I_{load}=200\text{mA}$		93		%
$T_{ST}$	Soft-start time	No load, $C_{OUT}=4.7\mu\text{F}$	1	1.2	1.4	ms
$I_L$	Current limit when PVDD short to ground		200	300	400	mA
<b>Class K power amplifier (mode1-mode7, mode10)</b>						
$I_q$	Quiescent current	$V_{DD}=4.2\text{V}$ , $V_{in}=0$ , no load		10	15	mA
$\eta$	Efficiency	$V_{DD}=3.6\text{V}$ , $P_o=1.0\text{W}$ , $R_L=8\Omega+33\mu\text{H}$		83		%
		$V_{DD}=3.6\text{V}$ , $P_o=1.0\text{W}$ , $R_L=6\Omega+33\mu\text{H}$		83		%
$F_{osc}$	Modulation frequency	$V_{DD}=3.0\text{V}$ to $5.5\text{V}$	600	800	1000	kHz
$A_v$	gain	external input resistance=3k $\Omega$		16.6		V/V
$V_{in}$	Recommend input voltage	$V_{DD}=3.0\text{V}$ to $5.5\text{V}$			1	Vp
$R_{in}$	Inner input resistance	mode1~mode7, mode10		6.6		k $\Omega$
$F_{hin}$	Input high pass filter corner frequency	$C_{in}=33\text{nF}$ , external input resistance=3k $\Omega$		502		Hz
Pagc	Mode1 Multi-Level AGC power	$V_{DD}=4.2\text{V}$ , $R_L=8\Omega+33\mu\text{H}$	1.08	1.2	1.32	W
		$V_{DD}=4.2\text{V}$ , $R_L=6\Omega+33\mu\text{H}$	1.44	1.6	1.76	W
		$V_{DD}=4.2\text{V}$ , $R_L=4\Omega+15\mu\text{H}$	2.16	2.4	2.64	W
		$V_{DD}=4.2\text{V}$ , $R_L=3\Omega+15\mu\text{H}$	2.16	2.4	2.64	W
	Mode2 Multi-Level AGC power	$V_{DD}=4.2\text{V}$ , $R_L=8\Omega+33\mu\text{H}$	0.99	1.1	1.21	W
Pagc	Mode2 Multi-Level AGC power	$V_{DD}=4.2\text{V}$ , $R_L=6\Omega+33\mu\text{H}$	1.35	1.5	1.65	W

Parameter		Test conditions	Min	Typ	Max	Units
		$V_{DD}=4.2V, R_L=4\Omega+15\mu H$	1.98	2.2	2.42	W
		$V_{DD}=4.2V, R_L=3\Omega+15\mu H$	2.16	2.4	2.64	W
	Mode3 Multi-Level AGC power	$V_{DD}=4.2V, R_L=8\Omega+33\mu H$	0.9	1	1.1	W
		$V_{DD}=4.2V, R_L=6\Omega+33\mu H$	1.17	1.3	1.43	W
		$V_{DD}=4.2V, R_L=4\Omega+15\mu H$	1.8	2	2.2	W
		$V_{DD}=4.2V, R_L=3\Omega+15\mu H$	2.16	2.4	2.64	W
	Mode4 Multi-Level AGC power	$V_{DD}=4.2V, R_L=8\Omega+33\mu H$	0.81	0.9	0.99	W
		$V_{DD}=4.2V, R_L=6\Omega+33\mu H$	1.08	1.2	1.32	W
		$V_{DD}=4.2V, R_L=4\Omega+15\mu H$	1.62	1.8	1.98	W
		$V_{DD}=4.2V, R_L=3\Omega+15\mu H$	2.16	2.4	2.64	W
	Mode5 Multi-Level AGC power	$V_{DD}=4.2V, R_L=8\Omega+33\mu H$	0.72	0.8	0.88	W
		$V_{DD}=4.2V, R_L=6\Omega+33\mu H$	0.9	1	1.1	W
		$V_{DD}=4.2V, R_L=4\Omega+15\mu H$	1.44	1.6	1.76	W
		$V_{DD}=4.2V, R_L=3\Omega+15\mu H$	1.8	2.0	2.2	W
	Mode6 Multi-Level AGC power	$V_{DD}=4.2V, R_L=8\Omega+33\mu H$	0.63	0.7	0.77	W
		$V_{DD}=4.2V, R_L=6\Omega+33\mu H$	0.81	0.9	0.99	W
		$V_{DD}=4.2V, R_L=4\Omega+15\mu H$	1.26	1.4	1.54	W
		$V_{DD}=4.2V, R_L=3\Omega+15\mu H$	1.62	1.8	1.98	W
	Mode7 Multi-Level AGC power	$V_{DD}=4.2V, R_L=8\Omega+33\mu H$	0.54	0.6	0.66	W
		$V_{DD}=4.2V, R_L=6\Omega+33\mu H$	0.72	0.8	0.88	W
$V_{DD}=4.2V, R_L=4\Omega+15\mu H$		1.08	1.2	1.32	W	
$V_{DD}=4.2V, R_L=3\Omega+15\mu H$		1.44	1.6	1.76	W	
PSRR	Power supply rejection ratio	$V_{DD}=4.2V, V_{p-p\_sin}=200mV$	217Hz		-68	dB
			1kHz		-68	dB
SNR	Signal-to-noise ratio	$V_{DD}=4.2V, P_o=1.7W, THD+N=1\%, R_L=8\Omega+33\mu H, A_v=8V/V$		98.8		dB
		$V_{DD}=4.2V, P_o=2.0W, THD+N=1\%, R_L=6\Omega+33\mu H, A_v=8V/V$		98.2		dB
Vn	Output noise voltage	$V_{DD}=4.2V, f=20Hz \text{ to } 20kHz, \text{ input ac grounded, } A_v=8V/V$	A-weighting	43		$\mu V_{rms}$
		$V_{DD}=4.2V, f=20Hz \text{ to } 20kHz, \text{ input ac grounded, } A_v=12V/V$		48		$\mu V_{rms}$
		$V_{DD}=4.2V, f=20Hz \text{ to } 20kHz, \text{ input ac grounded, } A_v=16V/V$		57		$\mu V_{rms}$
THD+N	Total harmonic distortion+noise	$V_{DD}=3.6V, P_o=1W, R_L=8\Omega+33\mu H, f=1kHz, \text{ Mode1}$		0.008		%
		$V_{DD}=3.6V, P_o=1W, R_L=6\Omega+33\mu H, f=1kHz, \text{ Mode10}$		0.009		%
P <sub>O</sub>	Mode10 output power	$THD+N=10\%, f=1kHz, R_L=8\Omega+33\mu H, V_{DD}=4.2V$		2.15		W
		$THD+N=1\%, f=1kHz, R_L=8\Omega+33\mu H, V_{DD}=4.2V$		1.75		W
		$THD+N=10\%, f=1kHz, R_L=8\Omega+33\mu H, V_{DD}=3.6V$		1.6		W
P <sub>O</sub>	Mode10 output power	$THD+N=1\%, f=1kHz, R_L=8\Omega+33\mu H, V_{DD}=3.6V$		1.28		W
		$THD+N=10\%, f=1kHz, R_L=6\Omega+33\mu H, V_{DD}=4.2V$		2.52		W

Parameter		Test conditions	Min	Typ	Max	Units
		THD+N=1%, f=1kHz, R <sub>L</sub> =6Ω+33μH, V <sub>DD</sub> =4.2V		2.05		W
		THD+N=10%, f=1kHz, R <sub>L</sub> =6Ω+33μH, V <sub>DD</sub> =3.6V		1.82		W
		THD+N=1%, f=1kHz, R <sub>L</sub> =6Ω+33μH, V <sub>DD</sub> =3.6V		1.5		W
		THD+N=10%, f=1kHz, R <sub>L</sub> =4Ω+15μH, V <sub>DD</sub> =4.2V		2.8		W
		THD+N=1%, f=1kHz, R <sub>L</sub> =4Ω+15μH, V <sub>DD</sub> =4.2V		2.4		W
		THD+N=10%, f=1kHz, R <sub>L</sub> =4Ω+15μH, V <sub>DD</sub> =3.6V		2.02		W
		THD+N=1%, f=1kHz, R <sub>L</sub> =4Ω+15μH, V <sub>DD</sub> =3.6V		1.68		W
		THD+N=10%, f=1kHz, R <sub>L</sub> =3Ω+15μH, V <sub>DD</sub> =4.2V		2.63		W
		THD+N=1%, f=1kHz, R <sub>L</sub> =3Ω+15μH, V <sub>DD</sub> =4.2V		2.35		W
		THD+N=10%, f=1kHz, R <sub>L</sub> =3Ω+15μH, V <sub>DD</sub> =3.6V		1.85		W
		THD+N=1%, f=1kHz, R <sub>L</sub> =3Ω+15μH, V <sub>DD</sub> =3.6V		1.65		W
<b>Receiver (mode8-mode9)</b>						
I <sub>q</sub>	Quiescent current	V <sub>DD</sub> =4.2V, Vin=0, no load		5	7.5	mA
η	Efficiency	V <sub>DD</sub> =3.6V, Po=0.8W, R <sub>L</sub> =8Ω+33μH, mode9		86		%
Fosc	Modulation frequency	V <sub>DD</sub> =3.0V to 5.5V	600	800	1000	kHz
A <sub>v</sub>	gain	external input resistance=3kΩ, mode8		1		V/V
		external input resistance=3kΩ, mode9		3		V/V
F <sub>hin</sub>	Input high pass filter corner frequency	mode8		106.6		kΩ
		mode9		36.6		kΩ
V <sub>n</sub>	Output noise voltage	Cin=33nF, external input resistance=3kΩ, mode8		44		Hz
		Cin=33nF, external input resistance=3kΩ, mode9		122		Hz
V <sub>n</sub>	Output noise voltage	V <sub>DD</sub> =4.2V, f=20Hz to 20kHz, input ac grounded, A <sub>v</sub> =1V/V	A-weighting	19		μVrms
		V <sub>DD</sub> =4.2V, f=20Hz to 20kHz, input ac grounded, A <sub>v</sub> =3V/V		22		μVrms
THD+N	Total harmonic distortion+noise	V <sub>DD</sub> =4.2V, Po=0.1W, R <sub>L</sub> =8Ω+33μH, f=1kHz, mode8		0.025		%
		V <sub>DD</sub> =4.2V, Po=0.4W, R <sub>L</sub> =8Ω+33μH, f=1kHz, mode9		0.025		%
<b>One wire pulse control</b>						
T <sub>H</sub>	$\overline{\text{SHDN}}$ high level duration time	V <sub>DD</sub> =3.0V to 5.5V	0.75	2	10	μs
T <sub>L</sub>	$\overline{\text{SHDN}}$ low level duration time	V <sub>DD</sub> =3.0V to 5.5V	0.75	2	10	μs
T <sub>LATCH</sub>	$\overline{\text{SHDN}}$ turn on delay time	V <sub>DD</sub> =3.0V to 5.5V	150		500	μs
T <sub>OFF</sub>	$\overline{\text{SHDN}}$ turn off delay time	V <sub>DD</sub> =3.0V to 5.5V	150		500	μs
<b>Multi-Level AGC</b> (Note 4)						
T <sub>ATF</sub>	Fast attack time	-13.5dB gain attenuation completed		1.5		ms
T <sub>ATS</sub>	Slow attack time	-13.5dB gain attenuation completed		6		ms
T <sub>ATT</sub>	Total attack time	-13.5dB gain attenuation completed		7.5		ms
T <sub>RLT</sub>	Release time	13.5dB gain release completed		280		ms
A <sub>MAX</sub>	Maximum attenuation			-13.5		dB

**Note 4:** Attack time points to 13.5dB gain attenuation time; Release time points to 13.5dB gain recovery time.



## MEASUREMENT SETUP

AW87318 features switching digital output, as shown in Figure 6. Need to connect a low pass filter to VOP/VON output respectively to filter out switch modulation frequency, then measure the differential output of filter to obtain analog output signal.

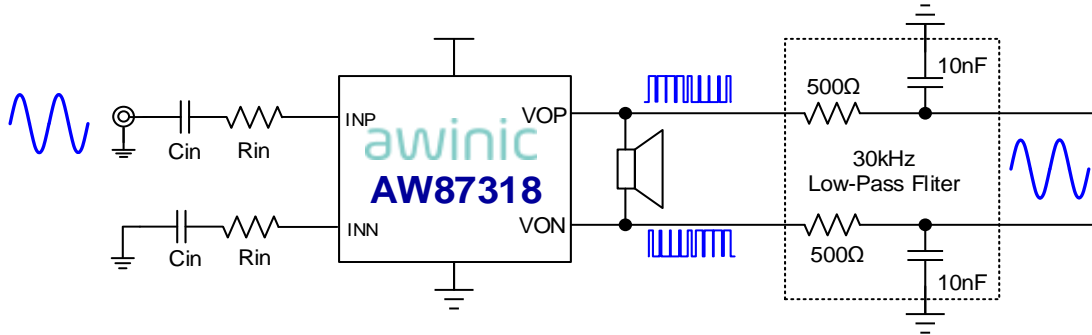


Figure 6 AW87318 test setup

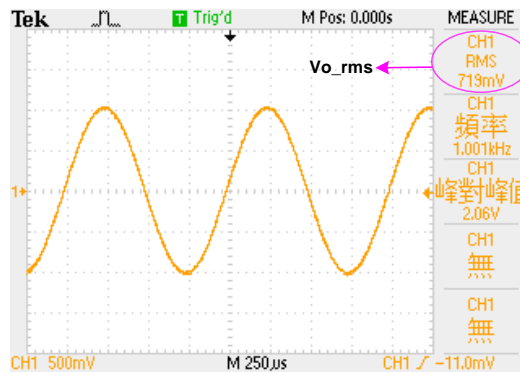
Low pass filter uses resistance and capacitor values listed in Table 1.

R <sub>filter</sub>	C <sub>filter</sub>	Low-pass cutoff frequency
500Ω	10nF	32kHz
1kΩ	4.7nF	34kHz

Table 1 AW87318 recommended values for low pass filter

### Output Power Calculation

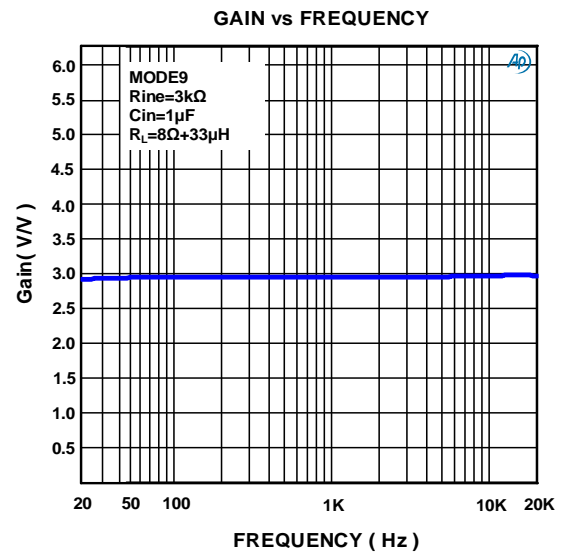
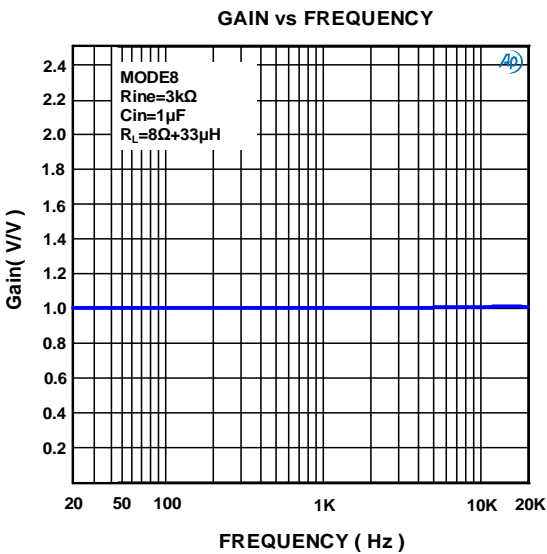
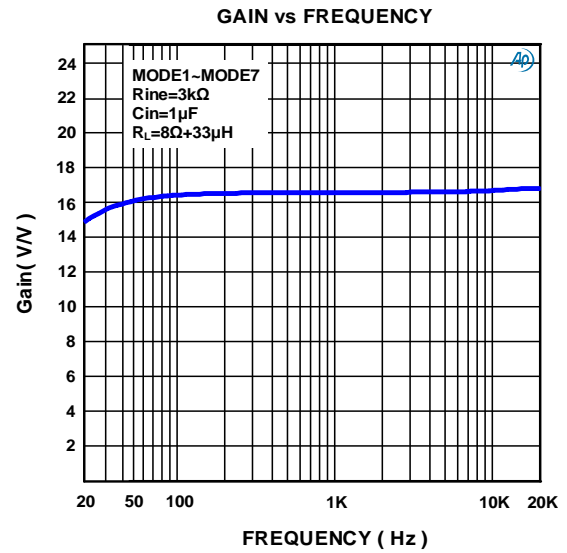
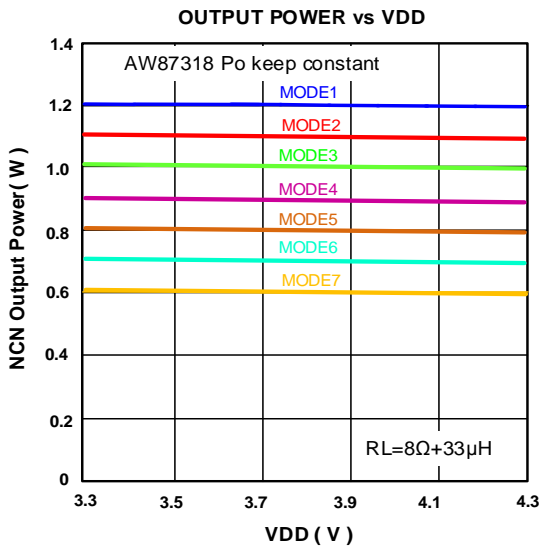
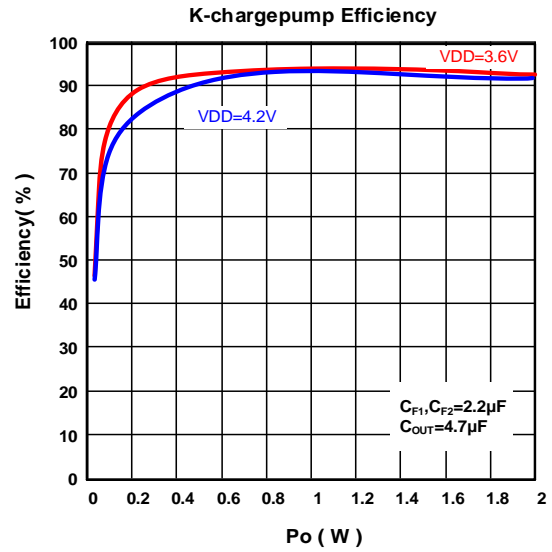
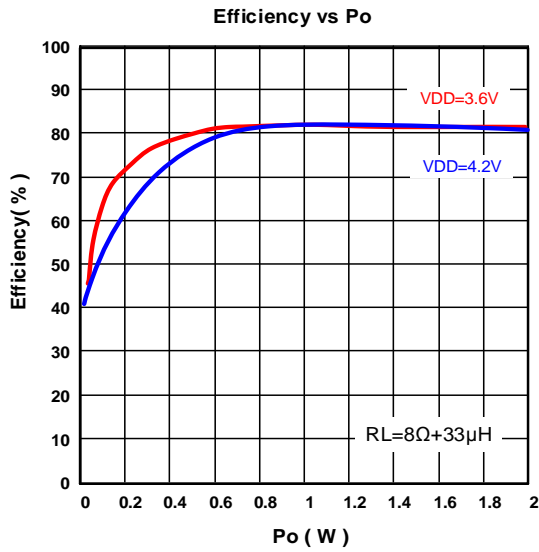
According to the above test methods, the differential analog output signal is obtained at the output of the low pass filter. The valid values Vo\_rms of the differential signal as shown below:

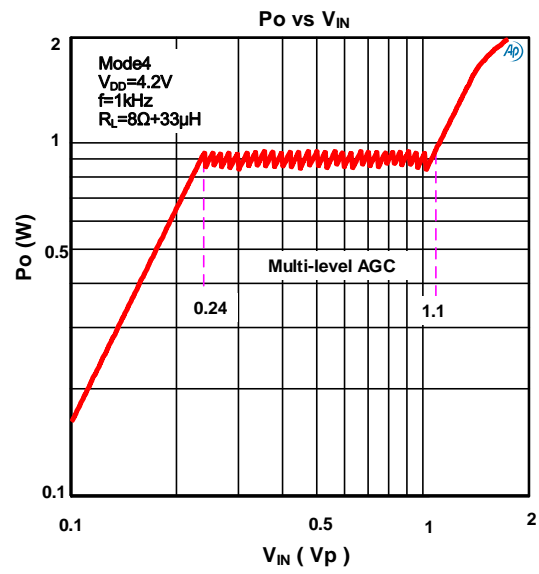
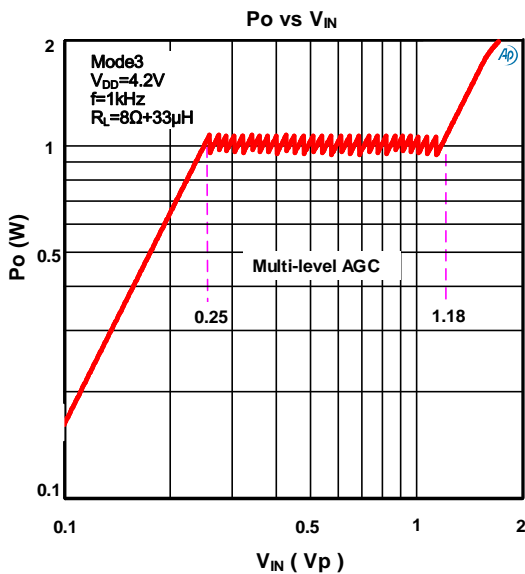
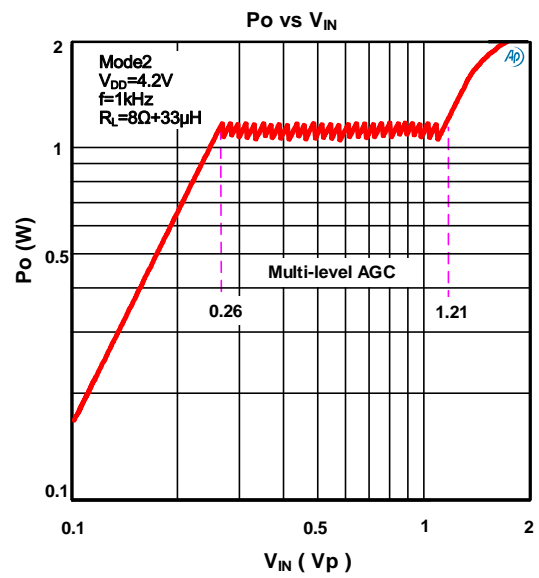
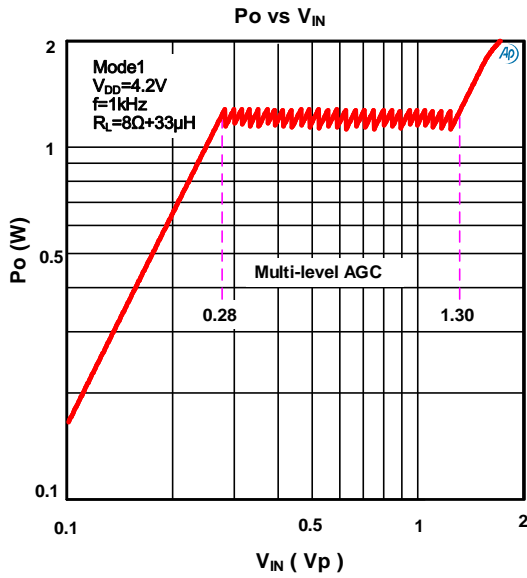
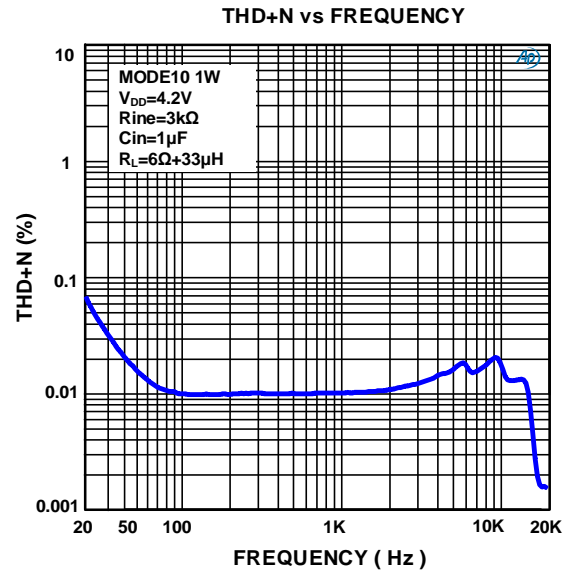
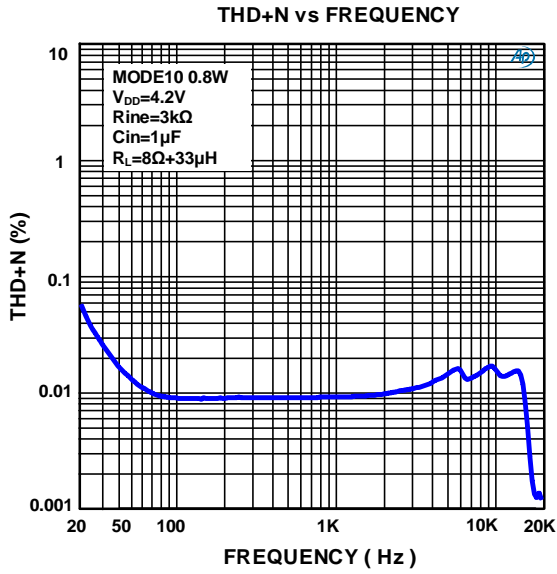


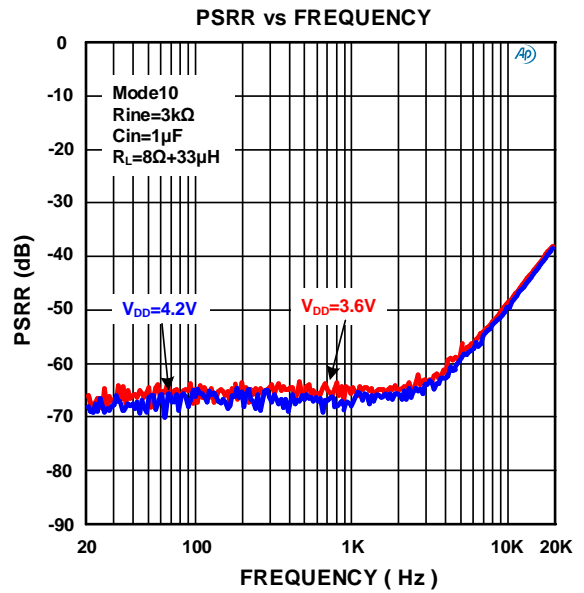
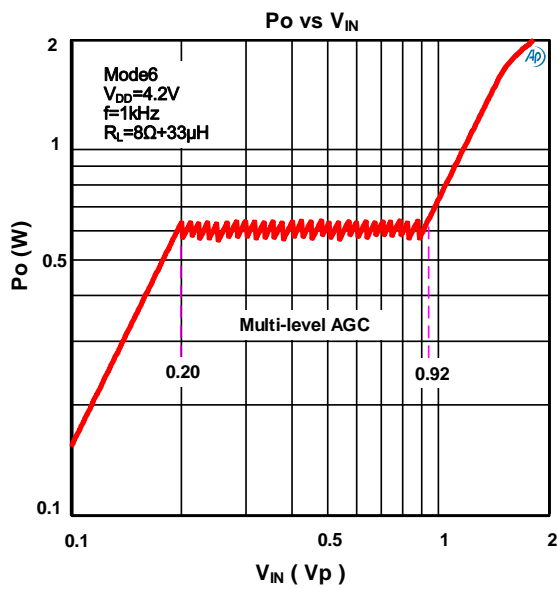
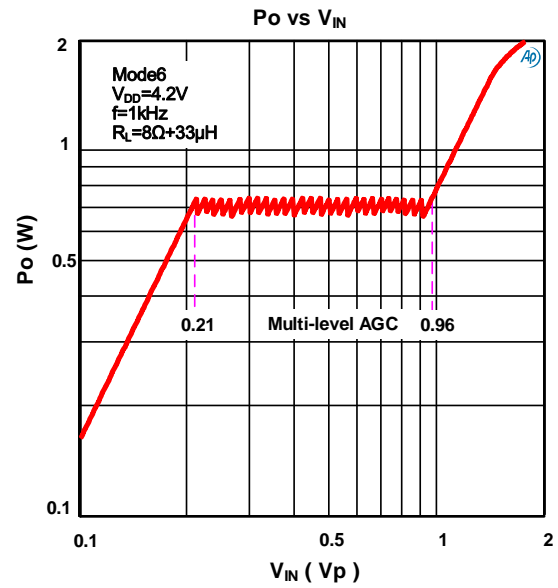
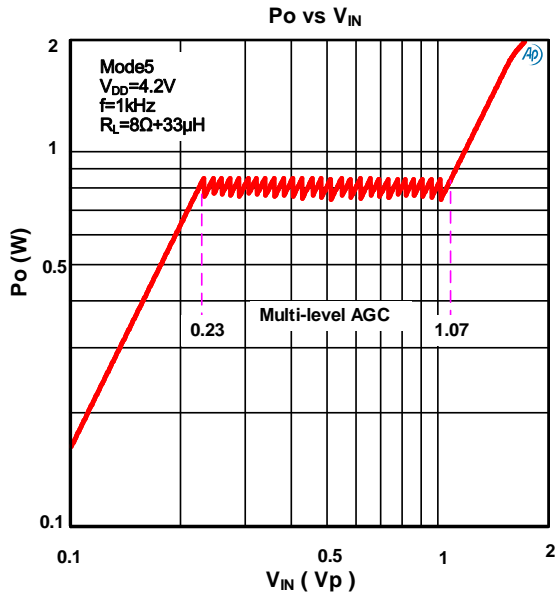
The power calculation of Speaker is as follows:

$$P_L = \frac{(V_{o\_rms})^2}{R_L} \quad (R_L: \text{load impedance of the speaker})$$

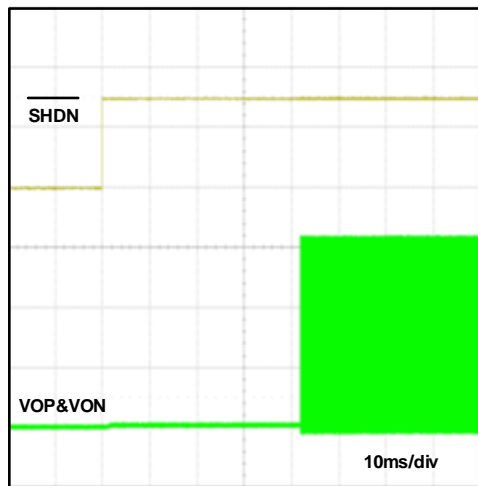
TYPICAL CHARACTERISTICS



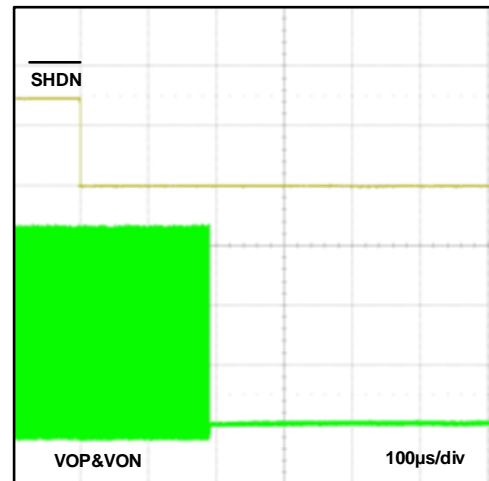




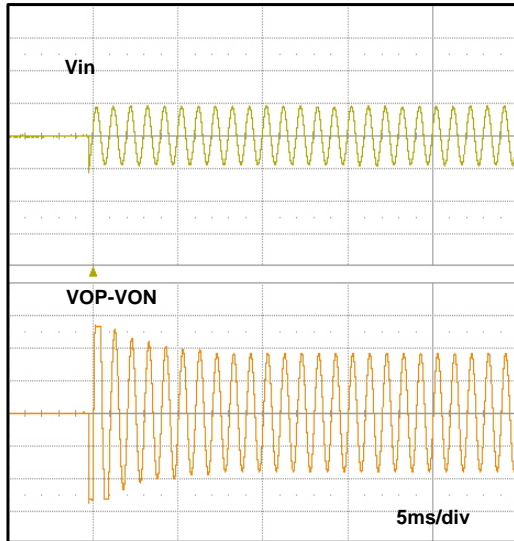
STARTUP SEQUENCE



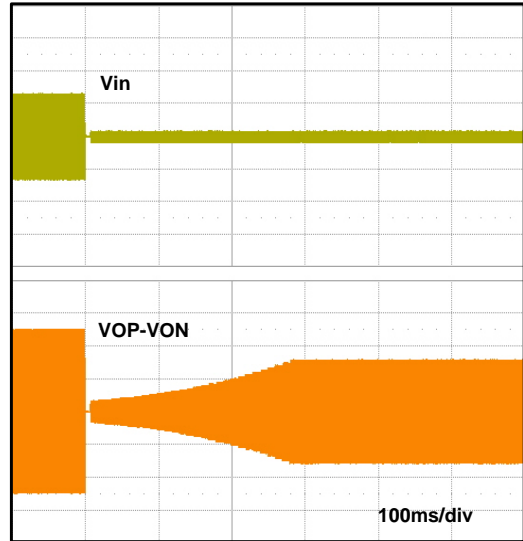
SHUTDOWN SEQUENCE



**MULTI-LEVEL-AGC  
ATTACK SEQUENCE**



**MULTI-LEVEL-AGC  
RELEASE SEQUENCE**



## DETAILED FUNCTIONAL DESCRIPTION

AW87318 is specifically designed to eliminate smart mobile phone music noise, to enhance overall sound quality, which is a new high efficiency, low noise, ultra-low distortion, constant large volume, upgrading eighth generation class K audio amplifiers. AW87318 integrated Awinic proprietary multi-level AGC audio algorithm, effectively eliminate music noise, improve sound quality and volume. Using a new generation K-Chargepump technology, efficiency reaches 93%, power amplifier's overall efficiency reaches 83%, greatly prolong the mobile phone usage time. AW87318 noise floor is as low as to 43uV, with 98.8dB high signal-to-noise-ratio(SNR). The ultra-low distortion 0.008% and unique multi-level AGC technology brings high quality music enjoyment.

AW87318 has 0.6W,0.7W,0.8W,0.9W,1W,1.1W and 1.2W seven subdivision selectable speaker-guard output power levels, which is suitable for different rated power speakers. With multi-level AGC audio algorithms, the music is pure natural and melodious. Within lithium battery voltage range (3.3V--4.35V), output power is constant, preventing voice becomes smaller and smaller during usage of cell phone.

AW87318 supports speaker and receiver two-in-one application. In receiver mode, the output noise is as low as to 19uV, amplifier is in class D mode, powered by VBAT.

The AW87318 built in excellent pop-click noise suppression circuit, effectively avoids pop-click noise during shutdown, wakeup, and power-up/down operation of AW87318.

The AW87318 uses Awinic proprietary TDD-Noise suppression technology and EMI suppression technology, effectively restrain TDD-Noise and EMI interference.

AW87318 has built-in over current protection, over-temperature protection and short circuit protection function, effectively protect the chip. AW87318 uses small 0.4mm pitch 1.6mmx1.68mm CSP-14 package. The AW87317 is specified over the industrial temperature range of -40°C to 85°C.

## CONSTANT OUTPUT POWER

In the mobile phone audio applications, the AGC function to promote music volume and quality is very attractive, but as the lithium battery voltage drops, general power amplifier output power will reduce gradually, leads to smaller and smaller music volume. So, it is hard to provide high quality music within the battery voltage range. The AW87318 integrated Awinic proprietary multi-level AGC audio algorithm, within lithium battery voltage range(3.3V-4.35V), output power is constant, the output power cannot drop along with lithium battery voltage lower down. Even if the battery voltage drops, AW87318 can still provide high quality large volume music enjoyment. AW87318 has ten operation modes, first seven modes have Multi-level AGC function, the output power levels are 1.2W,1.1W,1W,0.9W,0.8W,0.7W, 0.6W, respectively.

## Multi-level AGC technology

In the actual audio application, system output power tends to be more than rated power of speaker, such as in the 5V power supply, as for 8ohms speaker, the maximum undistorted power is about 1.56W, but many speakers' rated power is about 0.5W, if there is no output power control, the overload signal can cause damage to the speaker. The audio power amplifier with NCN function (that is single-level AGC) can protect the speaker effectively, with the increase of input signal, the output power increases. When output power exceeds the setting threshold, the NCN function reduces the internal gain of amplifier and restricts the output power under the set threshold.

But the NCN function has the attack time setting, which is the tradeoff between auditory effect and crack distortion noise, if the attack time is longer, the audio volume will be greater, but crack distortion will also increase; if the attack time is shorter, the crack distortion will decrease, but the audio volume will be reduced. General music has large peak factor, which is in the range of about 40~60dB, when playing music, the big peak signal output exceeds the maximum output amplitude, there will be more crack distortion, and obvious noise will be heard in some music, so it is need to use multi-level AGC technology to dynamically adjust the audio power amplifier, to increase music volume, at the same time, eliminate the emergence of obvious noise in large volume music and improve sound quality.

AW87318 integrated Awinic proprietary multi-Level AGC algorithm technology, effectively eliminating the noise in the music, make sound pure natural, and greatly enhancing the sound volume. The single-level AGC function and multi-level AGC function is shown in figure 7.

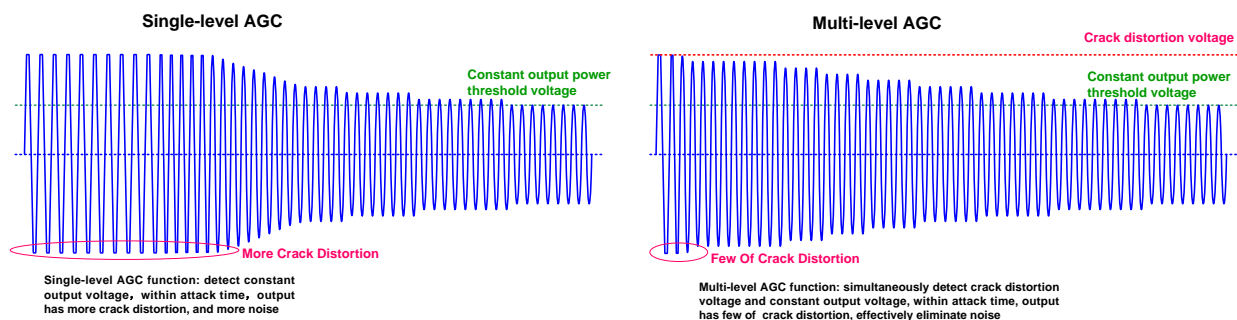


Figure 7 Single-level AGC/Multi-level AGC Operation Principle

### Attack time

Attack time is the time multi-level AGC takes for the gain to be attenuated -13.5dB once the audio signal exceeds the constant output power threshold voltage. When the output signal crack noise occurred, the Fast AGC of Multi-level AGC launched, attenuated the gain with 10dB within 1.5ms. When the crack noise eliminated, the Slow AGC of Multi-level AGC launched, attenuated the gain slowly, with 3.5dB within 6ms. According to smart mobile phone music noise features and demands for improve music quality and volume, adoption of the Awinic proprietary technology 'Multi-level AGC' inside AW87318, which keeping the music rhythm effectively, and at the same time eliminating the crack distortion, protecting the speaker.

### Release time

Release time is the time multi-level AGC takes for the gain to return to its normal level once the audio signal is smaller than crack distortion voltage or constant output power threshold voltage. According to smart mobile phone music noise features and demands for improve music quality and volume, release time of AW87318 is set to be 280ms, which can effectively eliminate the noise, make music sound pure natural.

### K-Chargepump

AW87318 adopts a new generation of charge pump technology: K -Chargepump structure, it has high efficiency and large driving ability, working frequency is 1.1MHz, built in soft start circuit, current limiting control loop and over-voltage-protection(OVP) loop, guaranteeing system stable and reliable operation.

### High Efficiency

AW87318 uses K-chargepump structure, booster output voltage PVDD is 1.5 times of supply voltage VDD, the ideal efficiency can reach 100%. K-chargepump efficiency is the ratio of output power to input power, that is

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\%$$

For example, in an ideal M times charge pump, the input current  $I_{IN}$  is M times of output current  $I_{OUT}$ , the efficiency formula can be written as:

$$\eta = \frac{P_{OUT}}{P_{IN}} * 100\% = \frac{V_{OUT} * I_{OUT}}{V_{IN} * M * I_{OUT}} * 100\% = \frac{V_{OUT}}{M * V_{IN}} * 100\%$$

M is charge pump work mode variable (1.5 times),  $V_{OUT}$  is charge pump output voltage,  $V_{IN}$  is power supply voltage,  $I_{OUT}$  is load current. For K-chargepump, the output voltage is 1.5 times of the input voltage, due to

the charge pump internal switch loss and IC static current loss, the actual efficiency will be up to 93%. Therefore, K-chargepump booster technology can greatly improve the power efficiency.

### Charge Pump Structure

Figure 8 is charge pump basic principle diagram, the charge pump used in AW87318 has seven switches, the output voltage PVDD is 1.5 times as input voltage VDD through seven switches timing control.

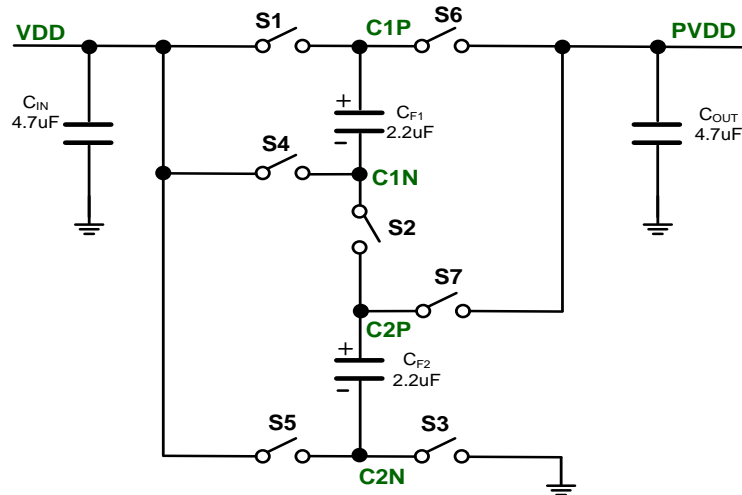


Figure 8 Charge Pump Principle Diagram

The operation of the charge pump has two phases. In  $\Phi 1$ , as shown in figure 9, switches S1, S2 and S3 are closed, VDD charges to the flying capacitor CF1 CF2.

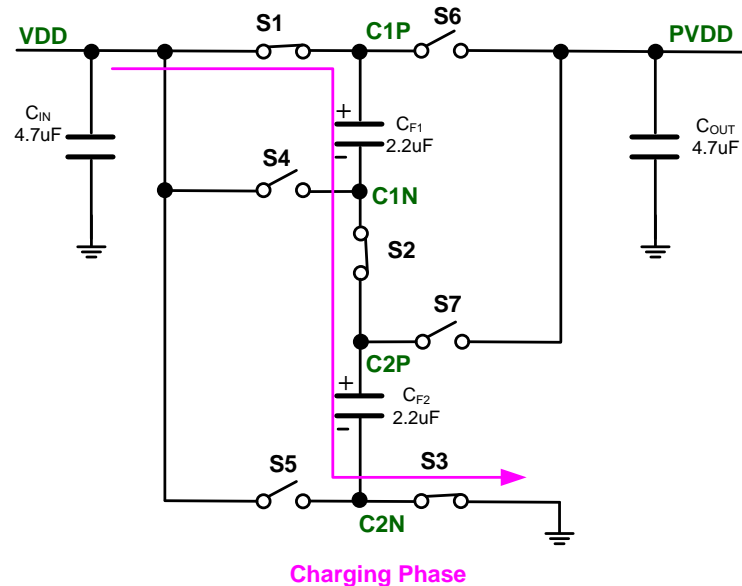


Figure 9  $\Phi 1$ : Flying Capacitor Charging

In  $\Phi 2$ , as shown in figure 10: switches S1, S2 and S3 are disconnected, switches S4, S5, S6 and S7 are closed. Because the voltage across the capacitor can't mutation, so the voltage on flying capacitor CF1 CF2, is added to the VDD, which make PVDD risen to a higher voltage.



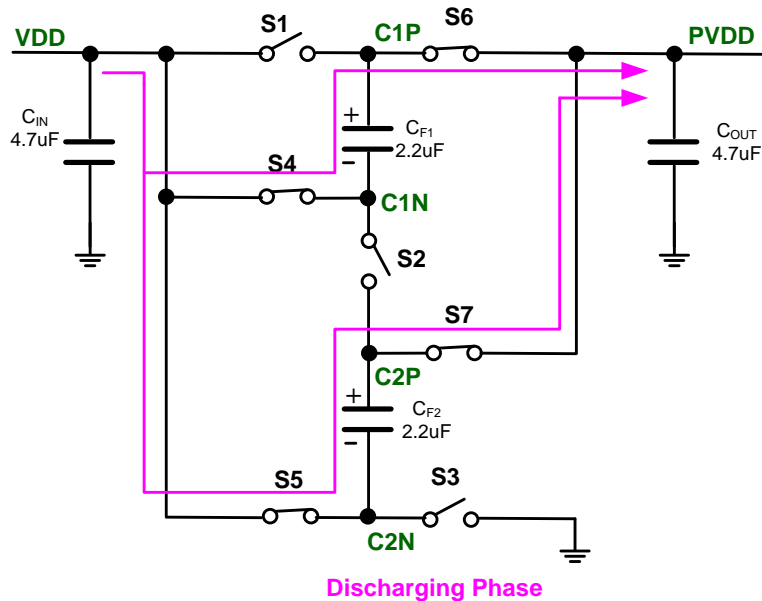


Figure 10 Φ2: Flying capacitor charge transfer to the output capacitance  $C_{out}$

### Soft start

K-chargepump has integrated soft start function in order to limit supply power inrush current during start-up. The supply current is limited to be 350 mA, and the soft start time is 1.2 ms.

### Current Limitation Control

K-chargepump has integrated the current limitation control loop. In normal operation, when the heavy load or a situation that make charge pump flow through very large current, the current limitation control loop will control charge pump maximum output current capacity, that is 2 A.

### Over Voltage Protection(OVP)Control

K-chargepump's output voltage PVDD is a multiple of the input voltage VDD, which provide a high voltage rail for internal power amplifier circuits, allowing the amplifiers provide greater output dynamic range in the lithium battery voltage range, so as to realize the large volume, high quality class K audio enjoyment. K-chargepump has integrated the over voltage protection control loop, when the input voltage VDD is greater than 4V, the output voltage PVDD is no longer a multiple of VDD, but is controlled by over voltage protection(OVP) loop and is stable in 6.05V, and the hysteresis voltage is about 50mV.

### Speaker & Receiver two-in-one application

AW87318 mode8, mode9 are receiver modes, the gain can be optional, 1V/V and 3V/V, respectively, which make the application flexible. Receiver modes use speakers' signal path, which has ultra-low distortion and a strong driving ability. So it is suitable for high definition voice application. Another advantage is that there is no need of additional external components, less system cost and PCB layout space.

In Figure 5 typical application, input capacitance  $C_{in}=33nF$ , input resistance  $R_{ine}=3k\Omega$ , speaker mode gain is about 16.6V/V, the input high-pass corner frequency is at 502Hz; When receiver mode gain is 1V/V, the output noise of receiver is 19uV, the input high-pass corner frequency is at 44Hz. AW87318 can achieve speaker and receiver two-in-one application without changing any hardware.

### One-wire pulse control

One wire pulse control technology only needs a single GPIO port to operate the chip, complete a variety of

functions, it is very popular in the area of the GPIO port shortage and portable systems.

When the control signal line is longer, because of the signal integrity or radio frequency interference problem, it will produce the narrow glitch signal. Awinic one wire pulse control technology integrated the Deglitch circuit in internal control pin, which can effectively eliminate the influence of the glitch signal, as shown in figure 11.

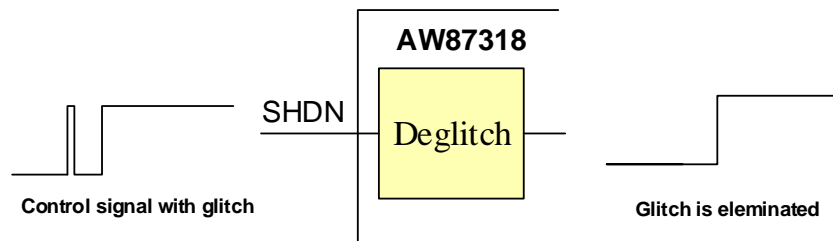


Figure 11 Awinic Deglitch function diagram

The traditional one wire pulse control technology still receives pulse signal from control port when chip is startup, so when the master control chip (such as mobile phone BB) sends wrong pulse during normal operation, the system will enter into error states. AW87318 uses one wire pulse latch technology, after the master control chip has sent pulses, the state will be latched, no longer receive the latter mis-sending pulse signals, as shown in figure 12.

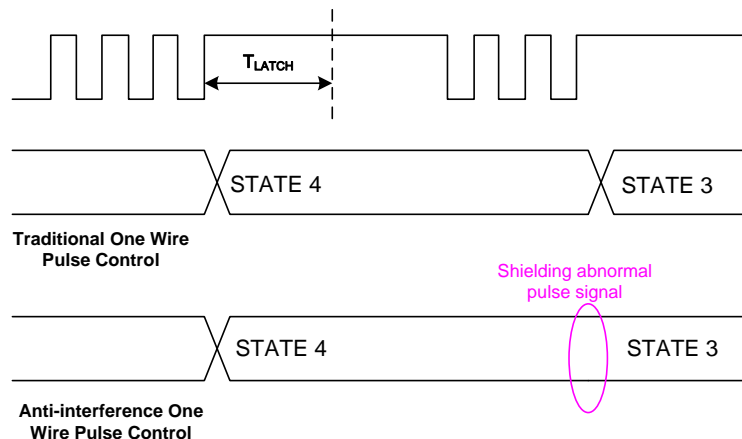
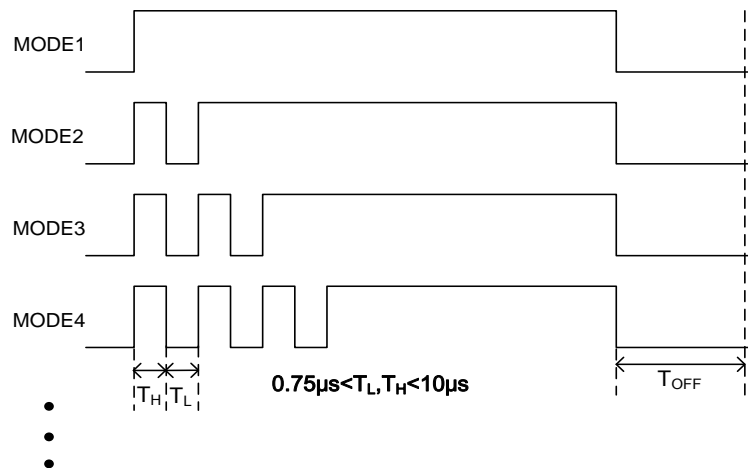


Figure 12 Anti-interference One Wire Pulse Control Function Diagram

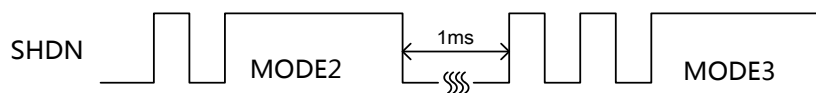
### One Wire Pulse Control

AW87318 select each mode through the detection of number of the pulse signal rising edge of SHDN pin, as shown in figure 13: When SHDN pin pull high from shutdown mode, there is only a rising edge, AW87318 enter into mode 1, Multi-level AGC output power is 1.2W; When high-low-high signal set to SHDN pin, there are two rising edges, AW87318 enter into mode 2, Multi-level AGC output power is 1.1W; When there are three rising edges, AW87318 enter into mode 3, Multi-level AGC output power is 1W; When there are four rising edges, AW87318 enter into mode 4, Multi-level AGC output power is 0.9W...; AW87318 has ten operation modes, the number of the rising edges does not allow more than ten.



**Figure 13 One Wire Pulse Control**

When AW87318 needs to work in different mode, PIN SHDN should be pull low longer than  $T_{OFF}$  first(recommended 1ms) which make the AW87318 shut down, Then send series pulse make the AW87318 enter into right mode, as shown in figure 14.



**Figure 14 One Wire Pulse Control Switching Sequence**

### RNS(RF TDD Noise Suppression)

GSM radios transmit using time-division multiple access with 217Hz intervals. The result is an RF signal with strong amplitude modulation at 217Hz and its harmonics that is easily demodulated by audio amplifiers.

In RF applications, improvements to both layout and component selection decrease the AW87318's susceptibility to RF noise and prevent RF signals from being demodulated into audible noise. Minimizing the trace lengths prevents them from functioning as antennas and coupling RF signals into the AW87318. Additional RF immunity can also be obtained from relying on the self-resonant frequency of capacitors as it exhibits the frequency response similar to a notch filter. Depending on the manufacturer, 10pF to 20pF capacitors typically exhibit self resonance at RF frequencies. These capacitors, when placed at the input pins, can effectively shunt the RF noise at the inputs of the AW87318. For these capacitors to be effective, they must have a low-impedance, low-inductance path to the ground plane.

Some RF energy will couple onto audio traces regardless of the effort to prevent this phenomenon from occurring, form audible TDD Noise. The AW87318 features a unique RNS technology, which effectively reduces RF energy, attenuate the RF TDD-noise, an acceptable audible level to the customer.

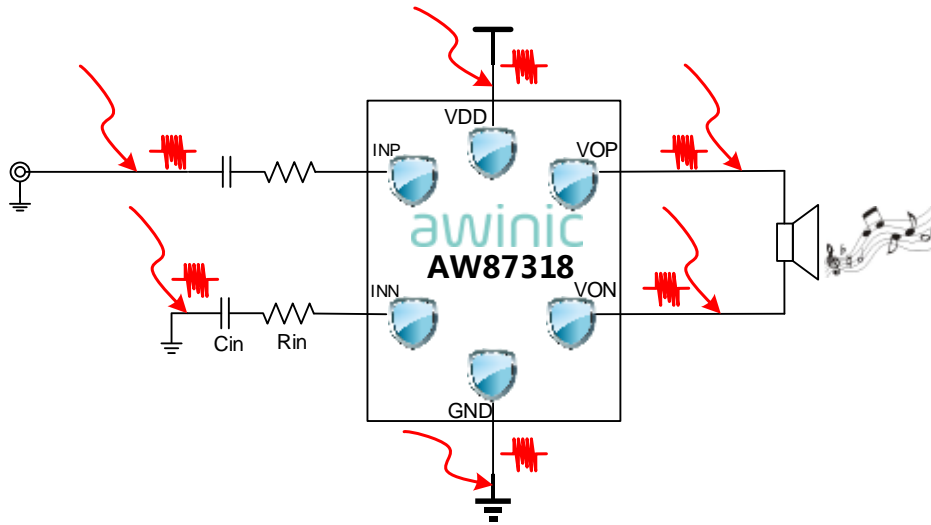


Figure 15 RF Radiation coupling schematic diagram

### Filter-Free Modulation Scheme

The AW87318 features a filter-free PWM architecture that reduces the LC filter of the traditional Class-D amplifier, increasing efficiency, reducing board area consumption and system cost.

### EEE

The AW87318 features a unique Enhanced Emission Elimination (EEE) technology, that controls fast transition on the output, greatly reduces EMI over the full bandwidth.

### Pop-Click Suppression

The AW87318 features unique timing control circuit, that comprehensively suppresses pop-click noise, eliminates audible transients on shutdown, wakeup, and power-up/down.

### Protection Function

When a short-circuit occurs between VOP/VON pin and VDD/GND or VOP and VON, the over-current circuit shutdown the device, preventing the device from being damaged. When the condition is removed, the AW87318 reactivate itself. When the junction temperature is high, the over-temperature circuit shutdown the device. The circuit switches back to normal operation when the temperature decreases to safe levels.

## APPLICATION INFORMATION

### External Input Resistor- $R_{ine}$ (Gain setting)

The AW87318 is a differential audio amplifier. The IC integrates two internal input resistors, which is  $R_{ini}=6.6k\Omega$ . Take external input resistor  $R_{ine}=3k\Omega$  for an example, gain setting as follows:

$$\text{Class K mode: } A_v = \frac{159.5k\Omega}{R_{ine} + R_{ini}} = \frac{159.5k\Omega}{3k\Omega + 6.6k\Omega} = 16.6V/V$$

$$\text{Receiver 1V/V mode: } A_v = \frac{110k\Omega}{R_{ine} + R_{ini}} = \frac{110k\Omega}{3k\Omega + 106.6k\Omega} = 1V/V$$

$$\text{Receiver 2V/V mode: } A_v = \frac{110k\Omega}{R_{ine} + R_{ini}} = \frac{110k\Omega}{3k\Omega + 36.6k\Omega} = 2.8V/V$$

### Input Capacitor- $C_{in}$ (input high-pass cutoff frequency)

The input coupling capacitor blocks the DC voltage at the amplifier input terminal. The input capacitors and input resistors form a high-pass filter with the corner frequency:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} \text{ (Hz)}$$

Setting the high-pass filter point high can block the 217Hz GSM noise coupled to inputs. Better matching of the input capacitors improves performance of the circuit and also helps to suppress pop-click noise.

Take typical application in Figure 1 as an example:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} \text{ (Hz)} = \frac{1}{2 * \pi * 9.6k\Omega * 33nF} \text{ (Hz)} = 502\text{Hz}$$

Take 1V/V receiver mode application as example, the input high-pass corner frequency is:

$$f_H(-3dB) = \frac{1}{2 * \pi * R_{intotal} * C_{in}} \text{ (Hz)} = \frac{1}{2 * \pi * 109.6k\Omega * 33nF} \text{ (Hz)} = 44\text{Hz}$$

### Differential input filter capacitor $C_d$ (input low-pass cutoff frequency)

Input differential input filter capacitor and input resistor together to form a low-pass filter, could be used to attenuate high frequency components of the input signal. When the musical sounds screechy, this low-pass filter can be appropriately attenuate the high frequency part of the input signal, so that the music signal sounds soft and comfortable. -3dB cutoff frequency of the low-pass filter is as follows:

$$f_L(-3dB) = \frac{1}{2 * \pi * (R_{ini} // R_{ine}) * 2 * C_d} \text{ (Hz)}$$

With input resistance  $R_{ine} = 3k\Omega$ , differential capacitance 220pF, for example, the low-pass cutoff frequency is as follows:

$$f_L(-3dB) = \frac{1}{2 * \pi * (R_{ini} // R_{ine}) * 2 * C_d} \text{ (Hz)} = \frac{1}{2 * \pi * 2.06k\Omega * 2 * 220pF} \text{ (Hz)} = 175.7\text{kHz}$$

### Supply Decoupling Capacitor ( $C_S$ )

The AW87318 is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically  $0.1\mu\text{F}$ . This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the AW87318 is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the  $0.1\mu\text{F}$  ceramic capacitor, place a  $10\mu\text{F}$  capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

### Flying Capacitor ( $C_F$ )

The value of the flying capacitor ( $C_F$ ) affects the load regulation and output resistance of the charge pump. A  $C_F$  value that is too small degrades the device's ability to provide sufficient current drive. Increasing the value of  $C_F$  improves load regulation and reduces the charge pump output resistance to an extent. A  $2.2\mu\text{F}@6.3\text{V}$  capacitor is recommended.

### Output Capacitor ( $C_{OUT}$ )

The output capacitor value and ESR directly affect the ripple at PVDD. Increasing  $C_{OUT}$  reduces output ripple. Likewise, decreasing the ESR of  $C_{OUT}$  reduces both ripple and output resistance. A  $4.7\mu\text{F}@10\text{V}$  capacitor is recommended.

### Optional Ferrite Bead Filter

The AW87318 passed FCC and CE radiated emissions with no ferrite chip beads and capacitors. Use ferrite chip beads and capacitors if device near the EMI sensitive circuits and/or there are long leads from amplifier to speaker, placed as close as possible to the output pin.

In the K class mode, the output is a square wave signal, which causing switch current at the output capacitor, increasing static power consumption, and therefore output capacitor should not be too large,  $1\text{nF}$  ceramic capacitors is recommended.

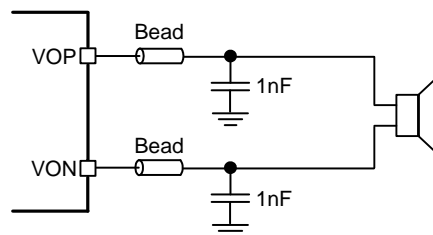


Figure 16 Ferrite Chip Bead and capacitor

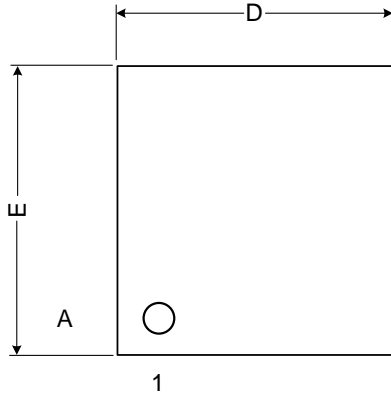
## PCB AND DEVICE LAYOUT CONSIDERATION

In order to obtain excellent performance of AW87318, PCB layout must be carefully considered. The design consideration should follow the following principles:

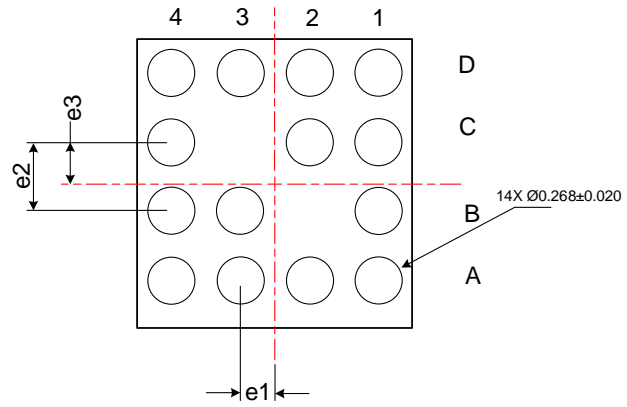
1. Try to provide a separate short and thick power line to AW87318, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to power supply pin.
2. The flying capacitors  $C_{F1}$ ,  $C_{F2}$  should be placed as close as possible to  $C_{1N}$ ,  $C_{1P}$  and  $C_{2N}$ ,  $C_{2P}$ , so the same to the output capacitor  $C_{OUT}$ , it should be close to PVDD pin. The connection from capacitor to PVDD pin should be short and thick.
3. The input capacitors and resistors should be close to AW87318 INN and INP input pin, the input line should be parallel to suppress noise coupling.
4. The beads and capacitor should be placed near to AW87318 VON and VOP pin. The output line from AW87318 to speaker should be as short and thick as possible. The width is recommended to be larger than 0.5mm.

PACKAGE DESCRIPTION

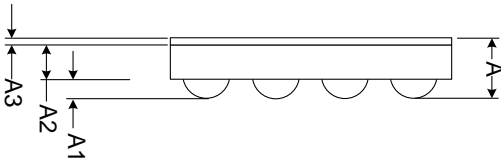
TOP VIEW



BOTTOM VIEW



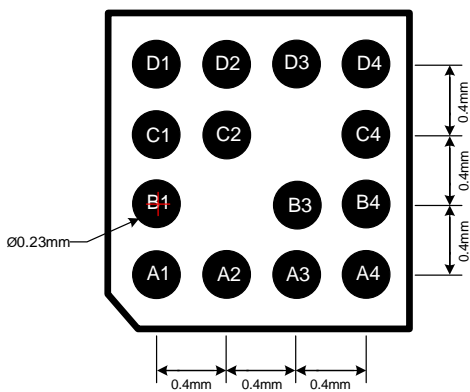
SIDE VIEW



Symbol	NOM	Tolerance
A	0.575	±0.055
A1	0.195	±0.020
A2	0.340	±0.025
A3	0.040	±0.010
D	1.600	±0.025
E	1.680	±0.025
e1	0.200	NA
e2	0.400	NA
e3	0.240	NA

Unit: mm

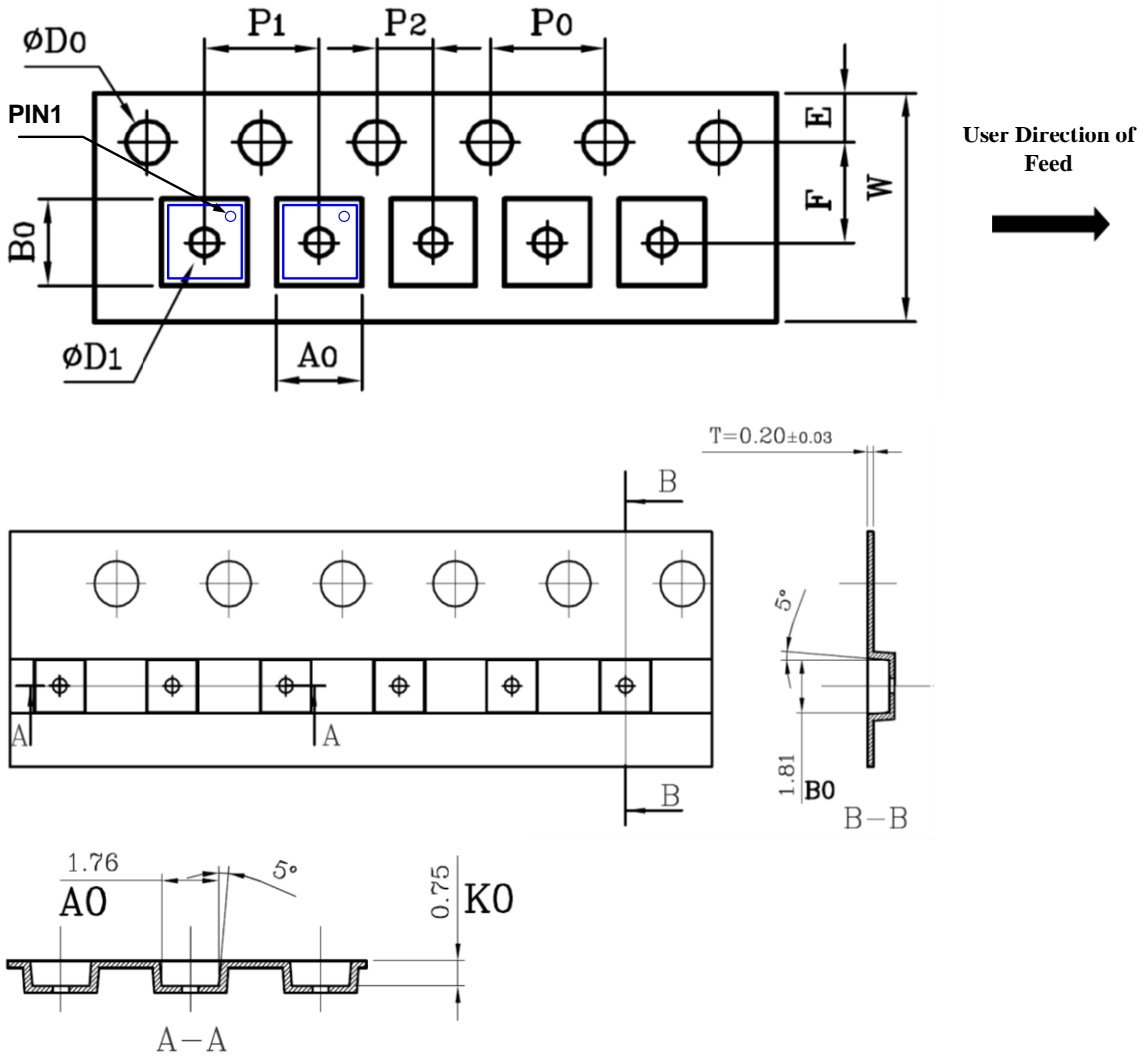
LAND PATTERN



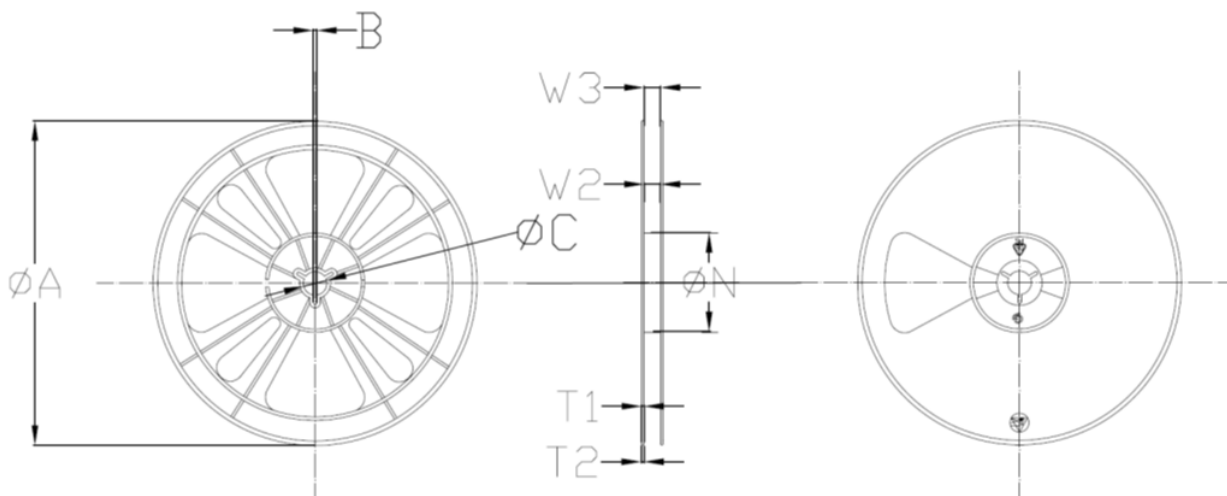


### Carrier Tape Description

Product Size and specification (UNIT : mm)									
Specification	W	P1	E	F	D0	D1	P0	P2	10P0
size	8.00 <sup>+0.30</sup> <sub>-0.10</sub>	4.0±0.1	1.75±0.1	3.5±0.05	1.50 <sup>+0.10</sup> <sub>-0</sub>	0.5±0.05	4.0±0.1	2.0±0.05	40±0.2
Specification	A0	A1	B0	B1	K0	K1	T		
size	1.76±0.05		1.81±0.05		0.75±0.05		0.20±0.03		



## Tape Description



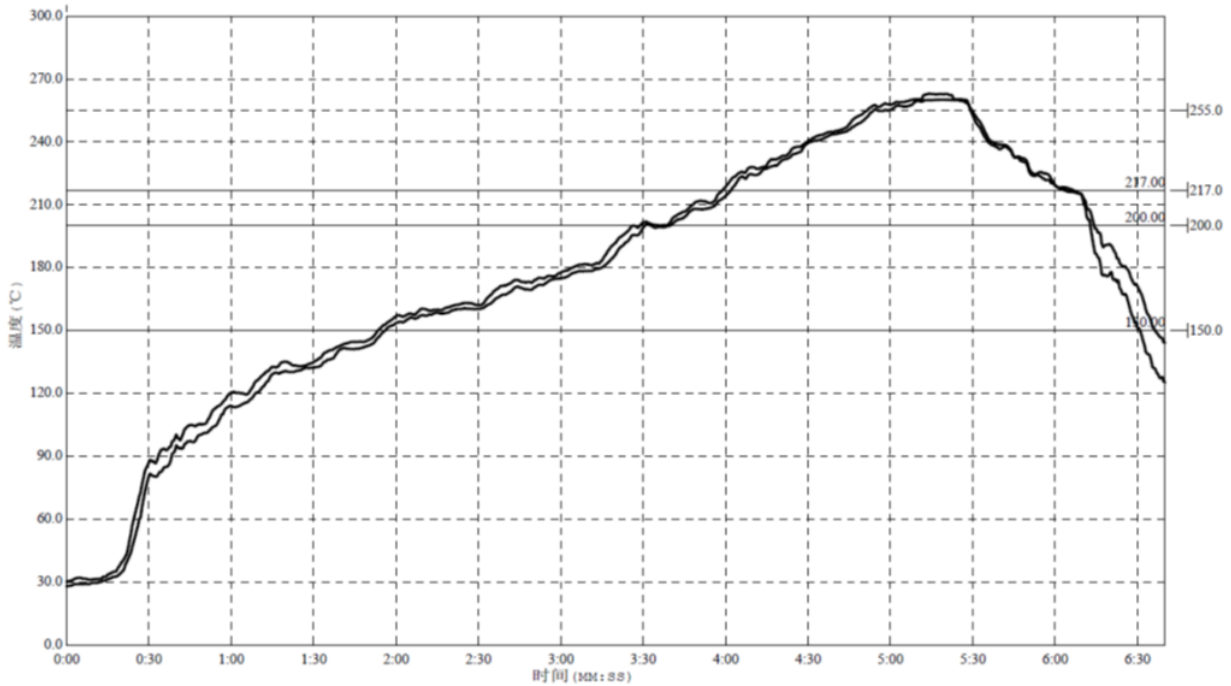
Unit: mm

Item	Value&Tolerance
A	179±1.0
B	2.0±0.1
C	13.5±0.2
N	54.8±0.2
W2	9.0±0.2
W3	9.2±1.0
T1	1.2±0.2
T2	1.5±0.2

Note:

1. Surface resistivity:  $10^5$  to  $10^{11}$  ohms/sq.
2. Restriction criterion of hazardous substance for packing material follow GP-M001.

## Reflow Soldering curve



Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C/sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 6°C/sec
Time from 25°C to peak temp	Max. 8min

## VERSION INFORMATION

Version	Date	Description
V1.0	2015-10-16	AW87318CSR datasheet V1.0
V1.1	2017-5-16	Add LAND PATTERN description, Carrier tap description, PIN1 location, tap description and reflow soldering curve, modify Flying capacitor rated voltage

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