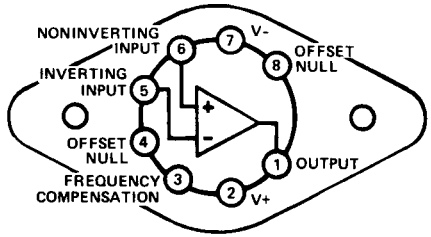
Fast-Settling, Wideband, FET-Input Op Amp

AD3554

4

FEATURES
Very High Slew Rate: 1000V/μs
Fast Settling: 150ns max to ±0.05%
Gain Bandwidth Product: 1.7GHz typical
High Output Current: 100mA min @ V_{OUT} = 10V
Full Differential Input

AD3554 FUNCTIONAL BLOCK DIAGRAM



TO-3 STYLE
BOTTOM VIEW

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PRODUCT DESCRIPTION

The AD3554 is a FET-input, hybrid operational amplifier that features an excellent combination of high slew rate, fast settling time and large gain-bandwidth product. The AD3554 has a full differential input with matched input FETs for low offset voltage.

The AD3554 can supply ±100mA at 10 volts. The slew rate is 1000V/μs minimum; 1200V/μs is typical. Settling time to ±0.05% of final value is only 150ns when configured as an inverting amplifier. The user can optimize the combination of bandwidth, slew rate, and settling time for a particular application by selecting the external compensation capacitor.

The AD3554 is recommended for any operational amplifier application where speed and bandwidth are important considerations. The high slew rate and fast settling time make the AD3554 an excellent choice for use in fast D/A converters, fast current amplifiers, integrators, waveform generators and multiplexer buffers.

The AD3554 is available in three versions: the "A" and "B" are specified over the -25°C to +85°C temperature range and "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed TO-3 style metal can.

The AD3554 is a pin-compatible replacement for 3554 devices from other manufacturers.

PRODUCT HIGHLIGHTS

1. The high slew rate (1000V/μs min) and fast settling time to 0.01% (250ns max) make the AD3554 ideal for D/A, A/D, sample-hold, and video instrumentation circuits.
2. Laser trimming techniques reduce initial offset voltage to as low as 1mV max (AD3554B), thus eliminating the need for external nulling in many applications.
3. Very high gain-bandwidth product (1.7GHz typical at A = 1000) makes the AD3554 an ideal choice for high frequency amplifier applications.
4. FET inputs result in a low bias current (50pA max, 10pA typ) in a high gain-bandwidth product operational amplifier.
5. Full differential input makes the AD3554 ideal for all standard operational amplifier applications such as high speed integrators, differentiators, and high gain amplifiers.
6. The 100mA at 10V output makes the AD3554 suitable for many applications that require high output power, such as cable drivers. The capacitance of coaxial cable (e.g., 29pF/foot for RG-58) does not load the AD3554 when the coaxial cable or transmission line is terminated in its characteristic impedance.

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SPECIFICATIONS (typical @ T_{CASE} = +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD3554AM	AD3554BM	AD3554SM
OPEN LOOP GAIN			
No Load	106dB (100dB min)	*	*
R_L = 100Ω	96dB (90dB min)	*	*
OUTPUT CHARACTERISTICS			
Voltage @ I_O = ±100mA	±11V (±10V min)	*	*
Output Resistance, Open Loop @ f = 10MHz	20Ω		
Current @ V_O = ±10V	±125mA (±100mA min)	*	*
FREQUENCY RESPONSE			
Bandwidth (0dB, Small Signal, C_F = 0)[1]	90MHz (70MHz min)	*	*
Gain-Bandwidth Product, C_F = 0			
G = 10V/V	225MHz (150MHz min)	*	*
G = 100V/V	725MHz (425MHz min)	*	*
G = 1000V/V	1700MHz (1000MHz min)	*	*
Full Power Bandwidth, C_F = 0, V_O = 20V p-p,			
R_L = 100Ω	19MHz (16MHz min)	*	*
Slew Rate, C_F = 0, V_O = 20V p-p,			
R_L = 100Ω	1200V/μs (1000V/μs min)	*	*
Settling Time, A = -1, to ±1%	60ns	*	*
to ±0.1%	120ns	*	*
to ±0.05%	140ns (150ns max)	*	*
to ±0.01%	200ns (250ns max)	*	*
INPUT OFFSET VOLTAGE			
Initial Offset	0.5mV (2.0mV max)	0.2mV (1.0mV max)	**
vs. Temperature	20μV/°C (50μV/°C max)	8μV/°C (15μV/°C max)	12μV/°C (25μV/°C max)
vs. Supply, T_A = min to max	80μV/V (300μV/V max)	*	*
INPUT BIAS CURRENT			
Either Input[2]	10pA (50pA max)	*	*
Initial Difference	2pA (10pA max)	*	*
vs. Supply Voltage	1pA/V	*	*
INPUT IMPEDANCE			
Differential	10^{11}Ω‖2pF	*	*
Common Mode	10^{11}Ω‖2pF	*	*
INPUT VOLTAGE RANGE			
Max Safe Input Voltage, Diff	±($\|V_{CC}\|$-8)	*	*
Common Mode	±($\|V_{CC}\|$-4)	*	*
Common Mode Rejection, V_{CM} = +7V, -10V	78dB (60dB min)	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(7 to 18)V	*	*
Quiescent Current	28mA (45mA max)	*	*
INPUT NOISE[1]			
Voltage, f_o = 1Hz	125nV/√Hz (450nV/√Hz max)	*	*
f_o = 10Hz	50nV/√Hz (160nV/√Hz max)	*	*
f_o = 100Hz	25nV/√Hz (90nV/√Hz max)	*	*
f_o = 1kHz	15nV/√Hz (50nV/√Hz max)	*	*
f_o = 10kHz	10nV/√Hz (35nV/√Hz max)	*	*
f_o = 100kHz	8nV/√Hz (25nV/√Hz max)	*	*
f_o = 1MHz	7nV/√Hz (25nV/√Hz max)	*	*
f_B = 0.3Hz to 10Hz	2μV p-p (7μV p-p max)	*	*
f_B = 10Hz to 1MHz	8μV rms (25μV rms max)	*	*
Current, f_B = 3Hz to 10Hz	45fA p-p	*	*
f_B = 10Hz to 1MHz	2pA rms	*	*
TEMPERATURE RANGE			
Operating, Rated Performance	-25°C to +85°C	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*
PACKAGE[3] – TO-3 Style (H08C)	AD3554AM	AD3554BM	AD3554SM

NOTES

[1] These parameters are untested and not guaranteed. This specification is established to a 90% confidence level.

[2] Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures, the current doubles every 10°C.

[3] See Section 19 for package outline information.

*Specifications same as AD3554AM.

**Specifications same as AD3554BM.

Specifications subject to change without notice.

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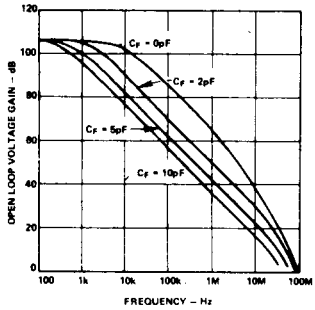

Figure 1. Open Loop Frequency Response (Voltage Gain)

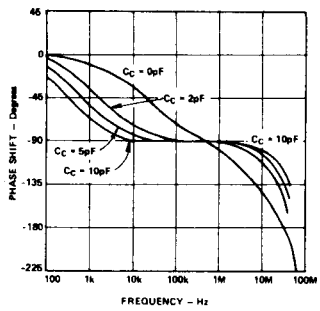

Figure 2. Open Loop Frequency Response (Phase Shift)

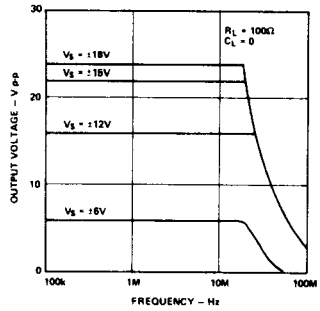

Figure 3. Output Voltage vs. Frequency

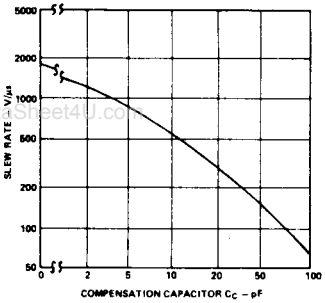

Figure 4. Slew Rate vs. Compensation

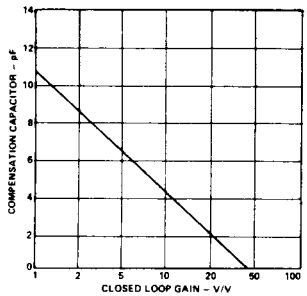

Figure 5. Recommended Compensation Capacitor vs. Closed Loop Gain

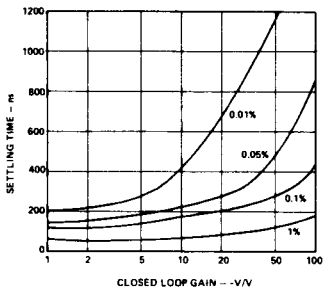

Figure 6. Settling Time vs. Closed Loop Gain (Circuit of Figure 18A)

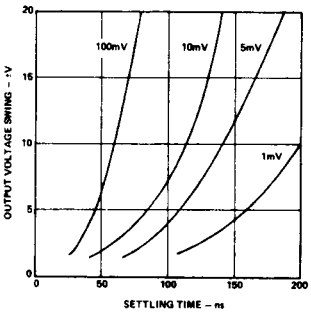

Figure 7. Settling Time vs. Output Voltage Change (Circuit of Figure 18A)

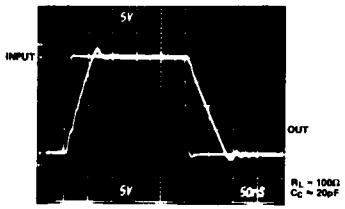

Figure 8. Voltage Follower Large Signal Response

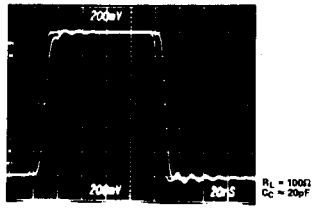

Figure 9. Voltage Follower Small Signal Response

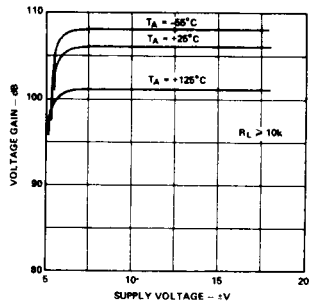

Figure 10. Open Loop Gain vs. Supply Voltage

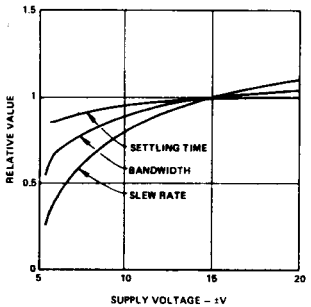

Figure 11. Dynamic Characteristics vs. Supply Voltage

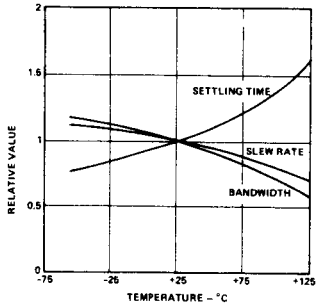

Figure 12. Dynamic Characteristics vs. Temperature

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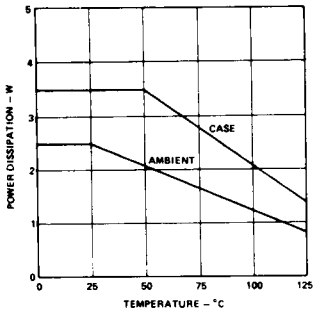

Figure 13. Power Dissipation vs. Temperature

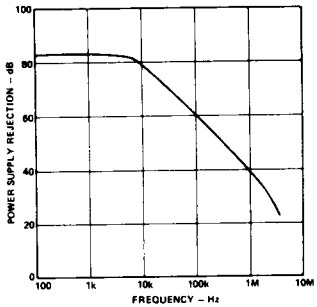

Figure 14. PSRR vs. Frequency

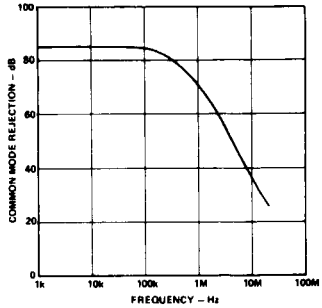

Figure 15. CMRR vs. Frequency

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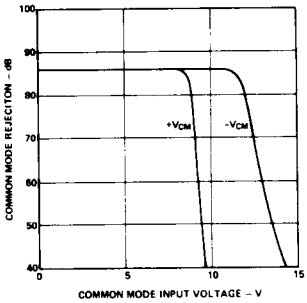

Figure 16. Common Mode Rejection vs. Input Voltage

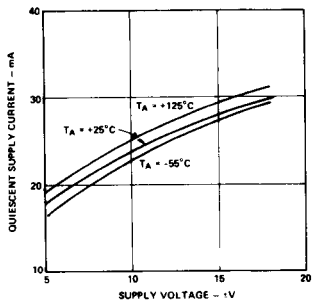

Figure 17. Quiescent Supply Current vs. Supply Voltage

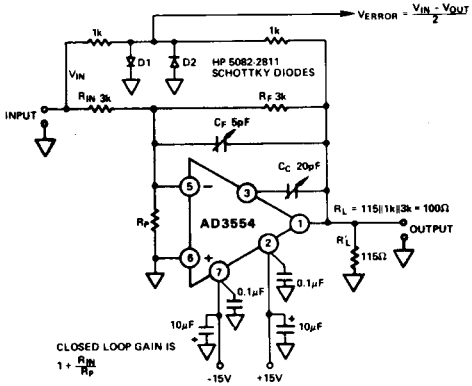

Figure 18A. Settling Time Test Circuit Schematic

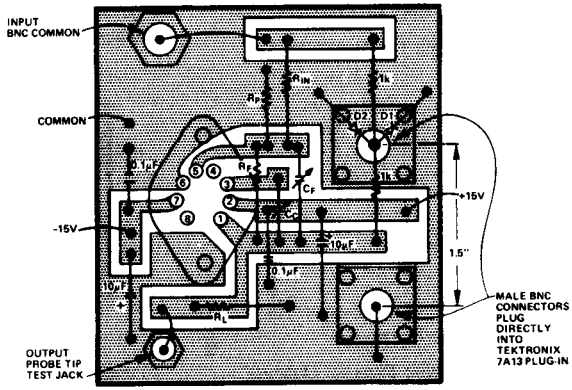

Figure 18B. Settling Time Test Circuit Layout

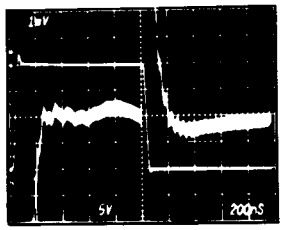

Figure 18C. Unity Gain Inverter Settling Time

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LAYOUT CONSIDERATIONS

As is the case with any high-speed design, proper layout is critical to avoid the introduction of unnecessary errors due to high-frequency coupling and stray capacitance.

Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as shielding the effects of high-frequency coupling. Sockets should be avoided, as the increased inter-lead capacitance can degrade bandwidth. Input and output connections should be kept as short as practical, particularly to the inverting input, which is especially sensitive to stray capacitances.

Low value resistors should be used to assure that the time constants formed with the circuit capacitances will not limit the amplifier performance. Resistor values less than 5.6kΩ are recommended.

Each power supply lead should be bypassed to ground as close as possible to the amplifier pins. A 10μF electrolytic or tantalum capacitor in parallel with a 0.01μF ceramic capacitor is recommended.

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GROUNDING

Grounding the case will add a slight capacitance to each pin. Therefore, we recommend leaving the case ungrounded.

In inverting applications we recommend grounding the non-inverting input rather than connecting it to a bias current compensating resistor. FET input amplifiers do not require compensating resistors because of their low input bias currents.

GUARDING

In high input impedance applications the input terminals may be surrounded by a conductive path to divert leakage currents. This guard ring should be connected to a low impedance point at the input signal potential.

In high frequency applications guarding may not be desirable as it increases the risk of oscillation due to increased printed circuit board capacitance.

COMPENSATION

The user can optimize the bandwidth, slew rate, or settling time by selecting the external frequency compensation capacitor. No compensation capacitor is required for closed loop gains above 50 and when the load capacitance is less than 100pF. When driving capacitive loads greater than 470pF, in low closed loop gain configurations, connect a 1000pF capacitor between pin 8 and the positive supply. The performance may be improved by connecting a small resistor in series with the output and a small capacitor from pin 1 to 5. See Typical Circuits.

The flat high frequency response of the AD3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin.

The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed loop gain.

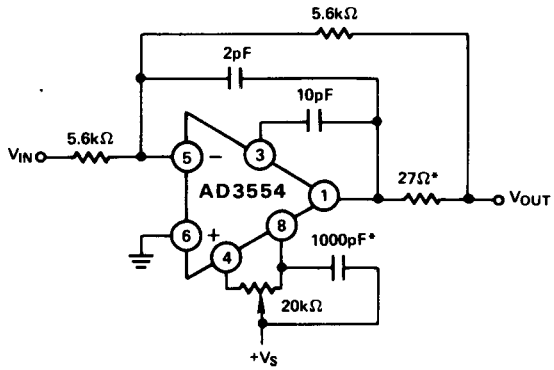
SHORT CIRCUIT PROTECTION

The AD3554 is short circuit protected for continuous output shorts to ground. Output shorts to either supply will destroy the device.

HEAT SINKING

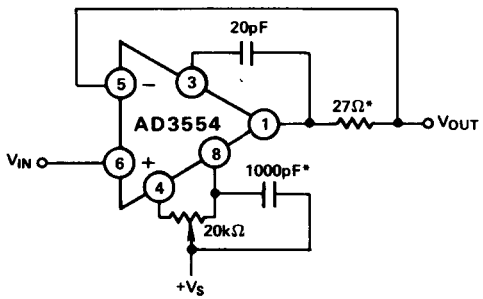
The AD3554 does not require heat sinking for most applications. However, at extreme temperature and full load conditions a heat sink will be necessary as indicated in the maximum power dissipation curve. We recommend connecting the heat sink to the amplifier case and keeping the combination ungrounded.

TYPICAL CIRCUITS



*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 19. Unity Gain Inverter



*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 20. Follower

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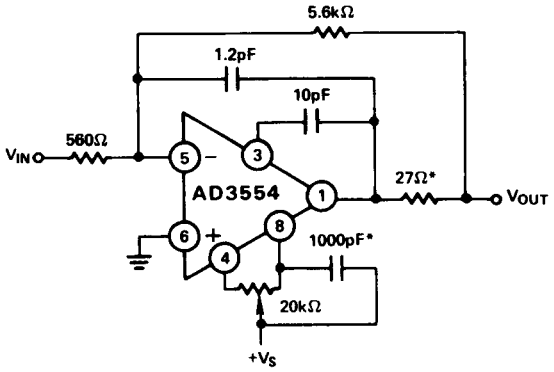

*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 21. Inverting Gain of 10 Amplifier

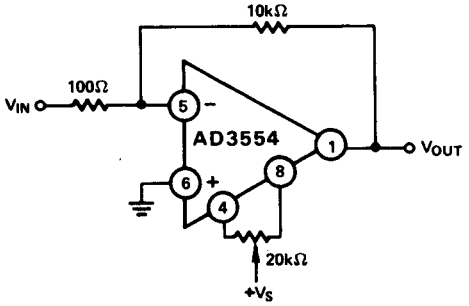

Figure 22. Inverting Gain of 100 Amplifier

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