ANALOG DEVICES

Adjustable Output 1-/2-/3-Phase Synchronous Buck Controller

ADP3182

FEATURES

Selectable 1-, 2-, or 3-phase operation at up to 1 MHz per phase

±2% worst-case differential sensing error over temperature

Externally adjustable 0.8 V to >5 V output from a 12 V supply

Logic-level PWM outputs for interface to external high power drivers

Active current balancing between all output phases

Built-in power good/crowbar functions

Programmable short-circuit protection with programmable latch-off delay

APPLICATIONS

Auxiliary supplies

DDR memory supplies

Point-of-load modules

GENERAL DESCRIPTION

The ADP3182 is a highly efficient multiphase, synchronous, buck-switching regulator controller optimized for converting a 12 V main supply into a high current, low voltage supply for use in point-of-load (POL) applications. It uses a multimode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 1-, 2-, or 3-phase operation, allowing for the construction of up to three complementary buck-switching stages. The ADP3182 also provides accurate and reliable short-circuit protection and adjustable current limiting.

ADP3182 is specified over the commercial temperature range of 0°C to +85°C and is available in a 20-lead QSOP package.
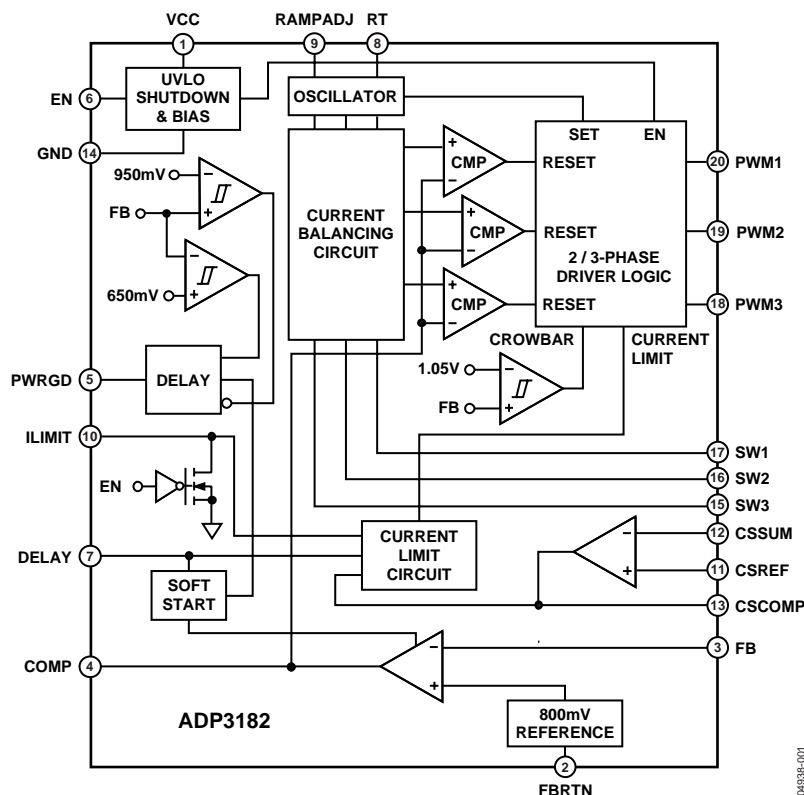
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

Rev. 0

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REVISION HISTORY

10/04—Revision 0: Initial Version

ADP3182

SPECIFICATIONS

VCC = 12 V, FBRTN = GND, T_A = 0°C to 85°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OSCILLATOR						
Frequency Range[2]	f_{OSC}		0.25		3	MHz
Frequency Variation	f_{PHASE}	T_A = 25°C, R_T = 348 kΩ, 3-phase	155	200	245	kHz
		T_A = 25°C, R_T = 174 kΩ, 3-phase		400		kHz
		T_A = 25°C, R_T = 100 kΩ, 3-phase		600		kHz
Output Voltage	V_{RT}	R_T = 100 kΩ to GND	1.9	2.0	2.1	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ − FB	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		0		100	μA
VOLTAGE ERROR AMPLIFIER						
Output Voltage Range[2]	V_{COMP}		0.7		3.1	V
Accuracy	V_{FB}	Referenced to FBRTN	784	800	816	mV
Line Regulation	ΔV_{FB}	VCC = 10 V to 14 V		0.05		%
Input Bias Current	I_{FB}	FB = 800 mV	−4		+4	μA
FBRTN Current	I_{FBRTN}			100	140	μA
Output Current	$I_{O(ERR)}$	FB forced to V_{OUT} − 3%		500		μA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		C_{COMP} = 10 pF		25		V/μs
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM − CSREF, Figure 2	−5.5		+5.5	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		−50		+50	nA
Gain Bandwidth Product	$GBW_{(CSA)}$			10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/μs
Input Common-Mode Range		CSSUM and CSREF	0		VCC − 2.5	V
Output Voltage Range			0.05		VCC − 2.5	V
Output Current	I_{CSCOMP}			500		μA
CURRENT BALANCE CIRCUIT						
Common-Mode Range	$V_{SW(X)CM}$		−600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0 V	20	30	40	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0 V	4	7	10	μA
Input Current Matching	$\Delta I_{SW(X)}$	SW(X) = 0 V	−7		+7	%
CURRENT LIMIT COMPARATOR						
Output Voltage						
Normal Mode	$V_{ILIMIT(NM)}$	EN > 2 V, R_{ILIMIT} = 250 kΩ	2.9	3	3.1	V
In Shutdown Mode	$V_{ILIMIT(SD)}$	EN < 0.8 V, I_{ILIMIT} = −100 μA			400	mV
Output Current, Normal Mode	$I_{ILIMIT(NM)}$	EN > 2 V, R_{ILIMIT} = 250 kΩ		12		μA
Maximum Output Current[2]			60			μA
Current Limit Threshold Voltage	V_{CL}	V_{CSREF} − V_{CSCOMP}, R_{ILIMIT} = 250 kΩ	105	125	145	mV
Current Limit Setting Ratio		V_{CL}/I_{ILIMIT}		10.4		mV/μA
DELAY Normal Mode Voltage	$V_{DELAY(NM)}$	R_{DELAY} = 250 kΩ	2.9	3	3.1	V
DELAY Overcurrent Threshold	$V_{DELAY(OC)}$	R_{DELAY} = 250 kΩ	1.7	1.8	1.9	V
Latch-Off Delay Time	t_{DELAY}	R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF		1.5		ms
SOFT START						
Output Current, Soft Start Mode	$I_{DELAY(SS)}$	During start-up, DELAY < 2.4 V	15	20	25	μA
Soft Start Delay Time	$t_{DELAY(SS)}$	R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF		500		μs

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ENABLE INPUT						
Input Low Voltage	$V_{IL(EN)}$				0.8	V
Input High Voltage	$V_{IH(EN)}$		2.0			V
Input Current	$I_{IN(EN)}$		−1		+1	μA
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to FBRTN	600	660	720	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to FBRTN	880	940	1000	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)} = 4\ mA$		225	400	mV
Power Good Delay Time				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to FBRTN	0.975	1.05	1.1	V
Crowbar Reset Point		Relative to FBRTN	550	650	750	mV
Crowbar Delay Time	$t_{CROWBAR}$	Overvoltage to PWM going low		400		ns
PWM OUTPUTS						
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)} = -400\ \mu A$		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)} = 400\ \mu A$	4.0	5		V
SUPPLY						
DC Supply Current				5	10	mA
UVLO Threshold Voltage	V_{UVLO}	VCC rising	6.5	6.9	7.3	V
UVLO Hysteresis			0.7	0.9	1.1	V

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or bench characterization, not tested in production.

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TEST CIRCUITS
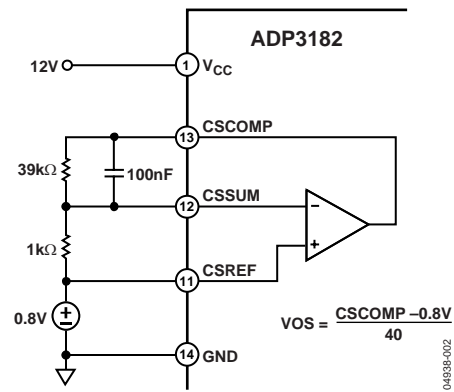
Figure 2. Current Sense Amplifier V$_{OS}$

$$VOS = \frac{CSCOMP - 0.8V}{40}$$

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +15 V
FBRTN	−0.3 V to +0.3 V
EN, DELAY, ILIMIT, RT, PWM1 to PWM3, COMP	−0.3 V to 5.5 V
SW1 to SW3	−5 V to +25 V
All Other Inputs and Outputs	−0.3 V to VCC + 0.3 V
Storage Temperature	−65°C to +150°C
Operating Ambient Temperature Range	0°C to 85°C
Operating Junction Temperature	125°C
Thermal Impedance (θ_{JA})	100°C/W
Lead Temperature	
Soldering (10 s)	300°C
Infrared (15 s)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
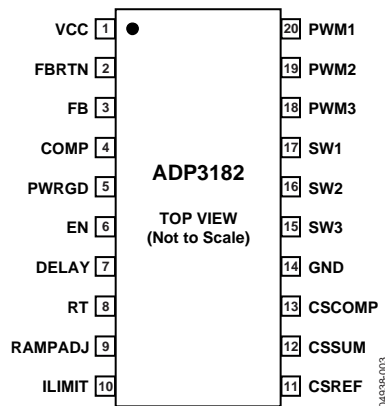
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PIN CONFIGURATION AND FUNCTION DESCRIPTION

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No.	Mnemonic	Description
1	VCC	Supply Voltage for the Device.
2	FBRTN	Feedback Return. Voltage error amplifier reference for remote sensing of the output voltage.
3	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor divider between the output and FBRTN connected to this pin sets the output voltage point. This pin is also the reference point for the power good and crowbar comparators.
4	COMP	Error Amplifier Output and Compensation Point.
5	PWRGD	Power Good Output. Open-drain output that signals when the output voltage is outside the proper operating range.
6	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
7	DELAY	Soft Start Delay and Current Limit Latch-Off Delay Setting Input. An external resistor and capacitor connected between this pin and GND sets the soft start, ramp-up time and the overcurrent latch-off delay time.
8	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
9	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
10	ILIMIT	Current Limit Setpoint/Enable Output. An external resistor from this pin to GND sets the current limit threshold of the converter. This pin is actively pulled low when the ADP3182's EN input is low, or when VCC is below its UVLO threshold, to signal to the driver IC that the driver high-side and low-side outputs should go low.
11	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier. This pin should be connected to the common point of the output inductors.
12	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
13	CSCOMP	Current Sense Compensation Point. A resistor and a capacitor from this pin to CSSUM determines the gain of the current sense amplifier.
14	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
15 to 17	SW3 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
18 to 20	PWM3 to PMW1	Logic-Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3418. Connecting the PWM3 output to GND causes that phase to turn off, allowing the ADP3182 to operate as a 1- or 2-phase controller.

TYPICAL PERFORMANCE CHARACTERISTICS
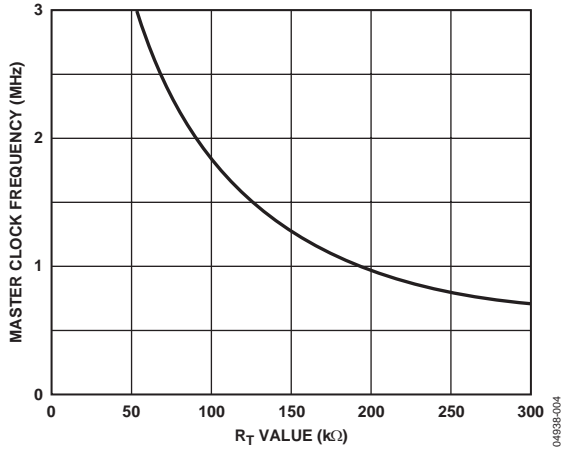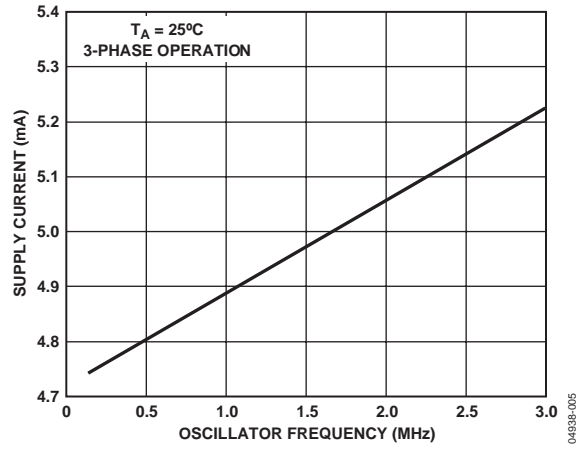

Figure 4. Master Clock Frequency vs. RT

Figure 5. Supply Current vs. Oscillator Frequency

THEORY OF OPERATION

The ADP3182 combines a multimode, fixed frequency PWM control with multiphase logic outputs for use in 1-, 2-, and 3-phase, synchronous, buck, point-of-load supply power converters. Multiphase operation is important for producing the high currents and low voltages demanded by auxiliary supplies in desktop computers, workstations, and servers. Handling the high currents in a single-phase converter would place high thermal demands on the components in the system, such as the inductors and MOSFETs.

The multimode control of the ADP3182 ensures a stable, high performance topology for

- Balancing currents and thermals between phases

- High speed response at the lowest possible switching frequency and output decoupling

- Minimizing thermal switching losses due to lower frequency operation

- Tight regulation and accuracy

- Reduced output ripple due to multiphase cancellation

- PC board layout noise immunity

- Ease of use and design due to independent component selection

- Flexibility in operation for tailoring design to low cost or high performance

START-UP SEQUENCE

During start-up, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP3182 operates as a 3-phase PWM controller. Grounding the PWM3 pin programs 1/2-phase operation.

When the ADP3182 is enabled, the controller outputs a voltage on PWM3 that is approximately 675 mV. An internal comparator checks the pin's voltage vs. a threshold of 300 mV. If the pin is grounded, it is below the threshold and the phase is disabled. The output resistance of the PWM pin is approximately 5 kΩ during this detection time. Any external pull-down resistance connected to the PWM pin should be more than 25 kΩ to ensure proper operation. PWM1 and PWM2 are disabled during the phase detection interval, which occurs during the first two clock cycles of the internal oscillator. After this time, if the PWM output is not grounded, the 5 kΩ resistance is removed, and the PWM output switches between 0 V and 5 V. If the PWM output is grounded, it remains off.

The PWM outputs are logic-level devices intended for driving external gate drivers such as the ADP3418. Because each phase is monitored independently, operation approaching 100% duty

cycle is possible. Also, more than one output can be on at the same time for overlapping phases.

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3182 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 4. To determine the frequency per phase, the clock is divided by the number of phases in use. If PWM3 is grounded, then divide the master clock by 2 for the frequency of the remaining two phases.

It is important to note that if only one phase is used, the clock will switch as if two phases were operating. This means that the oscillator frequency must be set at twice the expected value to program the desired PWM frequency.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3182 uses a differential-sensing, low offset voltage error amplifier. This maintains a worst-case specification of ±2% differential-sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the regulation point, usually the local bypass capacitor for the load. FBRTN should be connected directly to the remote sense ground point. The internal precision reference is referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing. The internal error amplifier compares the output of the reference to the FB pin to regulate the output voltage.

OUTPUT CURRENT SENSING

The ADP3182 provides a dedicated current sense amplifier (CSA) to monitor the total output current for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low-side MOSFET. This amplifier can be configured several ways depending on the objectives of the system:

- Output inductor DCR sensing without a thermistor for lowest cost

- Output inductor DCR sensing with a thermistor for improved accuracy for tracking inductor temperature

- Sense resistors for highest accuracy measurements

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output inductors) to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The

gain of the amplifier is programmable by adjusting the feedback resistor. The current information is then given as the difference of CSREF − CSCOMP. This difference in signal is used as a differential input for the current limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. In addition, the sensing gain is determined by external resistors so that the gain can be made extremely accurate.

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3182 has individual inputs for each phase that are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system, which has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for the current limit described previously.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control to compensate for changes in the supply voltage. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. External resistors can be placed in series with individual phases to create, if desired, an intentional current imbalance such as when one phase may have better cooling and can support higher currents. Resistors R_{SW1} through R_{SW3} (see the typical application circuit in Figure 9) can be used for adjusting thermal balance. Add placeholders for these resistors during the initial layout so that adjustments can be made after completing thermal characterization of the design.

To increase the current in any given phase, increase R_{SW} for that phase (set $R_{SW} = 0$ for the hottest phase and do not change it during balancing). Increasing R_{SW} to only 500 Ω substantially increases the phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase.

VOLTAGE CONTROL MODE

A high gain-bandwidth voltage mode error amplifier is used for the voltage-mode control loop. The control input voltage to the positive input is derived from the internal 800 mV reference. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the center point of a resistor divider from the output sense location. The main loop compensation is incorporated into the feedback network between FB and COMP.

SOFT START

The power-on, ramp-up time of the output voltage is set with a capacitor and resistor in parallel from the DELAY pin to ground. The RC time constant also determines the current limit latch-off time as explained in the following section. In UVLO or when EN is logic low, the DELAY pin is held at ground. After the UVLO threshold is reached and EN is logic high, the DELAY capacitor is charged with an internal 20 μA current source. The output voltage follows the ramping voltage on the DELAY pin, limiting the inrush. The soft start time depends on the value of C_{DLY}, with a secondary effect from R_{DLY}.

If either EN is taken low or VCC drops below UVLO, the DELAY capacitor is reset to ground to prepare for another soft start cycle. Figure 6 shows a typical soft start sequence for the ADP3182.
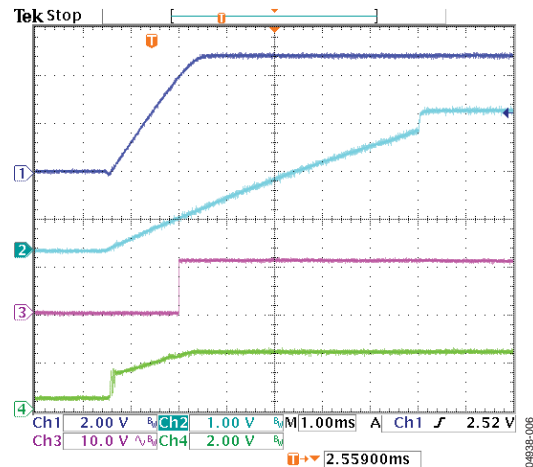

Figure 6. Typical Start-Up Waveforms
Channel 1: CSREF, Channel 2: DELAY,
Channel 3: PWRGD, Channel 4: COMP

CURRENT LIMIT, SHORT-CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3182 compares a programmable current limit setpoint to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3 V. The current through the external resistor is internally scaled to produce a current limit threshold of 10.4 mV/μA. If the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

After the limit is reached, the 3 V pull-up on the DELAY pin is disconnected, and the external delay capacitor is discharged through the external resistor. A comparator monitors the DELAY voltage and shuts off the controller when the voltage drops below 1.8 V. The current limit latch-off delay time is therefore set by the RC time constant discharging from 3 V to 1.8 V. Typical overcurrent latch-off waveforms are shown in Figure 7.

Because the controller continues to cycle the phases during the latch-off delay time, the controller returns to normal operation if the short is removed before the 1.8 V threshold is reached. The recovery characteristic depends on the state of PWRGD. If the output voltage is within the PWRGD window, the controller resumes normal operation. However, if a short circuit has caused the output voltage to drop below the PWRGD threshold, a soft start cycle is initiated.

The latch-off function can be reset by either removing and reapplying VCC to the ADP3182, or by pulling the EN pin low for a short time. To disable the short-circuit latch-off function, the external resistor to ground should be left open, and a high-value (>1 MΩ) resistor should be connected from DELAY to VCC. This prevents the DELAY capacitor from discharging, so the 1.8 V threshold is never reached. The resistor has an impact on the soft start time because the current through it adds to the internal 20 μA current source.

During start-up when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 2 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry.

An inherent per phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

POWER GOOD MONITORING

The power good comparator monitors the output voltage via the FB pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the electrical table. PWRGD goes low if the output voltage is outside this specified range or the EN pin is pulled low. Figure 8 shows the PWRGD output response when the input power is removed from the regulator.
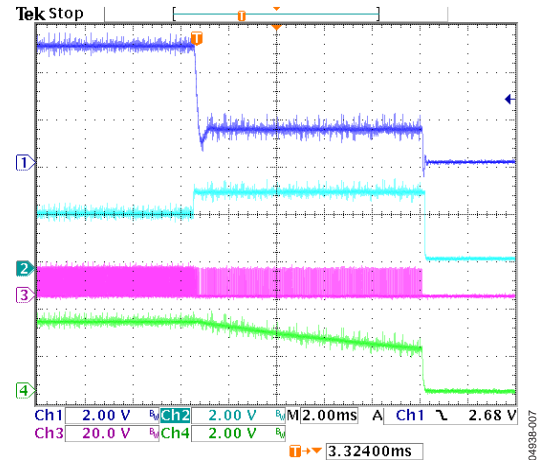

Figure 7. Overcurrent Latch-Off Waveforms
Channel 1: CSREF, Channel 2: COMP,
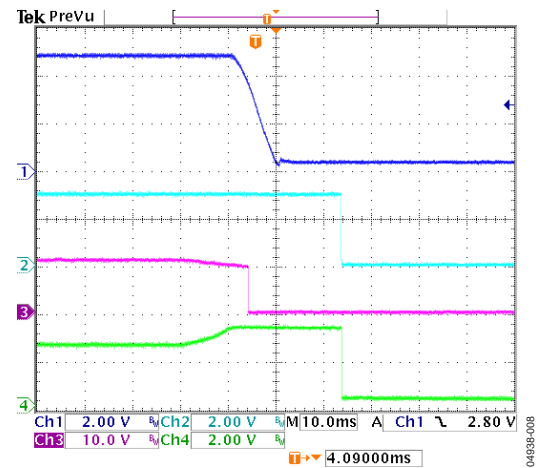*Channel 3: Phase 1 Switch Node, Channel 4: DELAY*

Figure 8. Shutdown Waveforms
Channel 1: CSREF, Channel 2: DELAY,
Channel 3: PWRGD, Channel 4: COMP

OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 650 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output over-voltage is due to a short in the high-side MOSFET, this action limits the current of the input supply or blows the fuse to protect the microprocessor from being destroyed.

OUTPUT ENABLE AND UVLO

For the ADP3182 to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold, and the EN pin must be higher than its logic threshold. If UVLO is less than the threshold or the EN pin is logic low, the ADP3182 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the ILIMIT pin at ground.

In the application circuit, the ILIMIT pin should be connected to the OD pins of the ADP3418 drivers. The ILIMIT being grounded disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs were not disabled, a negative voltage could be generated during output due to the high current discharge of the output capacitors through the inductors.
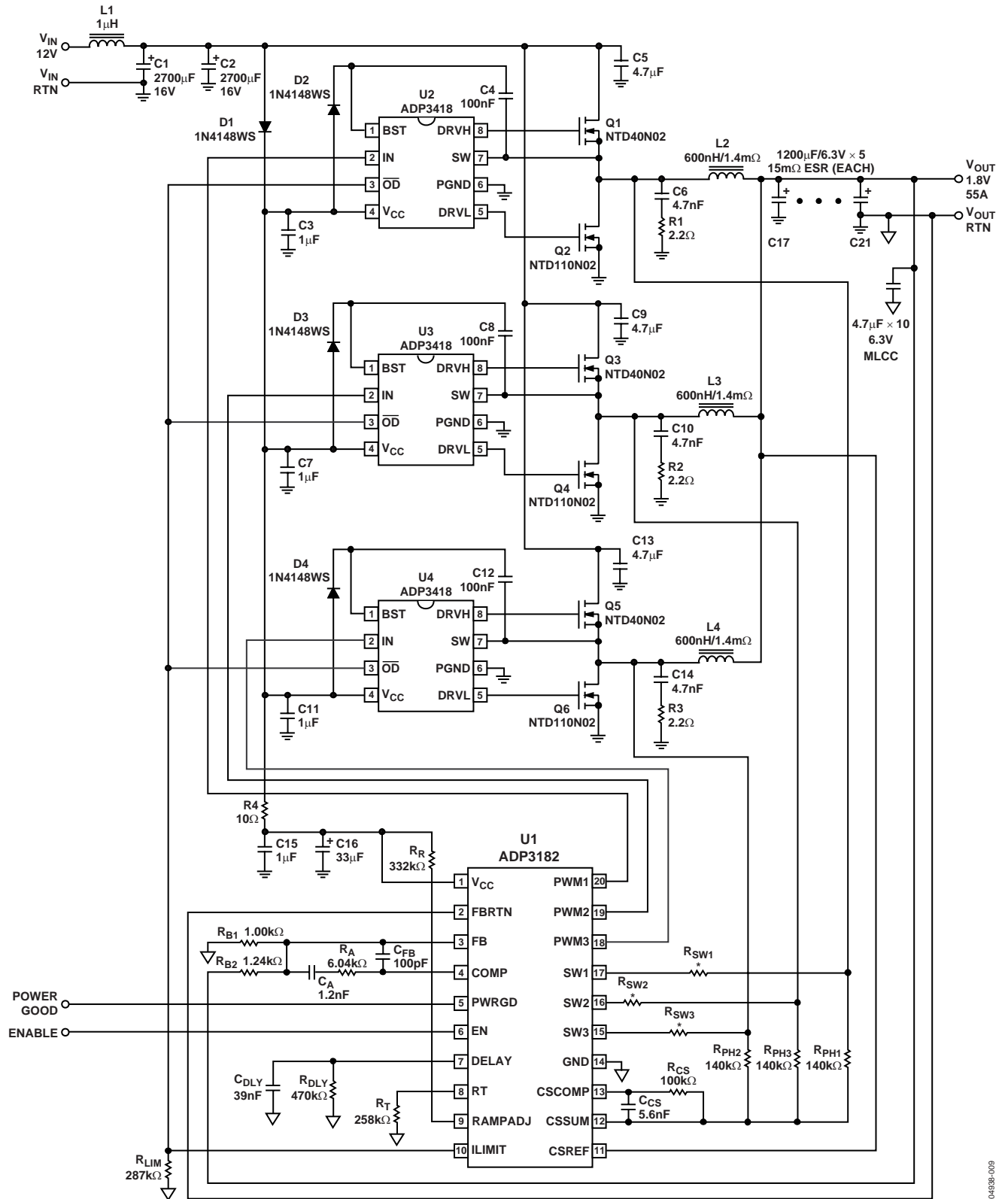
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Figure 9. 1.8 V, 55 A Application Circuit

APPLICATIONS

The design parameters for the typical high current point-of-load dc/dc buck converter shown in Figure 9 are as follows:

- Input voltage (V_{IN}) = 12 V

- VID setting voltage (V_{OUT}) = 1.8 V

- Duty cycle (D) = 0.15

- Output current I_O = 55 A

- Maximum output current (I_{LIM}) = 110 A

- Number of phases (n) = 3

- Switching frequency per phase (f_{SW}) = 250 kHz

SETTING THE CLOCK FREQUENCY

The ADP3182 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors and the input and output capacitors. With n = 3 for three phases, a clock frequency of 750 kHz sets the switching frequency (f_{SW}) of each phase to 250 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. Equation 1 shows that to achieve a 750 kHz oscillator frequency, the correct value for R_T is 256 kΩ. Alternatively, the value for R_T can be calculated using

$$R_T = \frac{1}{n \times f_{SW} \times 4.7\,\text{pF}} - 27\,\text{k}\Omega \tag{1}$$

$$R_T = \frac{1}{3 \times 250\,\text{kHz} \times 4.7\,\text{pF}} - 27\,\text{k}\Omega = 256\,\text{k}\Omega$$

where 4.7 pF and 27 kΩ are internal IC component values. For good initial accuracy and frequency stability, a 1% resistor is recommended. The closest standard 1% value for this design is 258 kΩ.

SOFT START AND CURRENT LIMIT LATCH-OFF DELAY TIME

Because the soft start and current limit latch-off delay functions share the DELAY pin, these two parameters must be considered together. The first step is to set C_{DLY} for the soft start ramp. This ramp is generated with a 20 μA internal current source. The value of R_{DLY} has a second-order impact on the soft start time because it sinks part of the current source to ground. However, as long as R_{DLY} is kept greater than 200 kΩ, this effect is minor.

The value for C_{DLY} can be approximated using

$$C_{DLY} = \left(20\,\mu\text{A} - \frac{V_{OUT}}{2 \times R_{DLY}}\right) \times \frac{t_{SS}}{V_{OUT}} \tag{2}$$

where:
t_{SS} is the desired soft start time.
Assuming an R_{DLY} of 390 kΩ and a desired soft start time of 3 ms, C_{DLY} is 36 nF.
The closest standard value for C_{DLY} is 39 nF.

Once C_{DLY} is chosen, R_{DLY} can be calculated for the current limit latch-off time using

$$R_{DLY} = \frac{1.96 \times t_{DELAY}}{C_{DLY}} \tag{3}$$

If the result for R_{DLY} is less than 200 kΩ, a smaller soft start time should be considered by recalculating the equation for C_{DLY}, or a longer latch-off time should be used. R_{DLY} should never be less than 200 kΩ. In this example, a delay time of 9 ms results in R_{DLY} = 452 kΩ. The closest standard 5% value is 470 kΩ.

INDUCTOR SELECTION

The amount of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs, but allows using smaller inductors and, for a specified peak- peak transient deviation, less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger inductors and more output capacitance for the same peak-peak transient deviation. In any multiphase converter, a practical value for the peak-peak inductor ripple current is less than 50% of the maximum dc current in the same inductor. Equation 4 shows the relationship between the inductance, oscillator frequency, and peak-peak ripple current in the inductor.

Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage.

$$I_R = \frac{V_{OUT} \times (1-D)}{f_{SW} \times L} \tag{4}$$

$$L \geq \frac{V_{OUT} \times R_x \times (1 - (n \times D))}{f_{SW} \times V_{RIPPLE}} \tag{5}$$

where:
R_X is ESR of output bulk capacitors.

Solving Equation 5 for a 20 mV p-p output ripple and an R_X of 3 mΩ voltage yields

$$L \geq \frac{1.8 \text{ V} \times 3 \text{ m}\Omega \times (1 - 3 \times 0.15)}{250 \text{ kHz} \times 20 \text{ mV}} = 594 \text{ nH}$$

If the resulting ripple voltage is too low, the level of inductance can be decreased until the desired ripple value is met. This allows optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. For this example, choosing a 600 nH inductor is a good starting point that produces a calculated ripple current of 6.6 A. The inductor should not saturate at the peak current of 21.6 A and should be able to handle the sum of the power dissipation caused by the average current of 18.3 A in the winding and core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the phase currents. A large DCR can cause excessive power losses, whereas too small a value can lead to increased measurement error. For this design, a DCR of 1.4 mΩ was chosen.

Designing an Inductor

Once the inductance and DCR are known, the next step is to either design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. The first decision in designing the inductor is to choose the core material. Several possibilities for providing low core loss at high frequencies include the powder cores (e.g., Kool-Mμ® from Magnetics, Inc., or from Micrometals) and the gapped soft ferrite cores (e.g., 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided, especially when the inductor value is relatively low and the ripple current is high, due to their high core loss.

The best choice for a core geometry is a closed-loop type such as a potentiometer core, a PQ, U, or E core, or a toroid core. A good compromise between price and performance is a core with a toroidal shape.

Many useful references for magnetics design are available for quickly designing a power inductor, such as

- Magnetic Designer Software
  Intusoft (www.intusoft.com)

- *Designing Magnetic Components for High-Frequency DC-DC Converters*, by William T. McLyman, Kg Magnetics, Inc., ISBN 1883107008

Selecting a Standard Inductor

The following power inductor manufacturers can provide design consultation and deliver power inductors optimized for high power applications upon request.

- Coilcraft
  (847) 639-6400
  www.coilcraft.com

- Coiltronics
  (561) 752-5000
  www.coiltronics.com

- Sumida Electric Company
  (510) 668-0660
  www.sumida.com

- Vishay Intertechnology
  (402) 563-6866
  www.vishay.com

OUTPUT CURRENT SENSE

The output current can be measured by summing the voltage across each inductor and passing the signal through a low-pass filter. The CS amplifier is configured with resistors $R_{PH(X)}$ (for summing the voltage), and R_{CS} and C_{CS} (for the low-pass filter). The output current I_O is set by the following equations:

$$I_O = \frac{R_{PH(x)}}{R_{CS}} \times \frac{V_{DRP}}{R_L} \tag{6}$$

$$C_{CS} \geq \frac{L}{R_L \times R_{CS}} \tag{7}$$

where:
R_L is the DCR of the output inductors.
V_{DRP} is the voltage drop from CSCOMP to CSREF.

When load current reaches its limit, V_{DRP} is at its maximum (V_{DRPMAX}). V_{DRPMAX} can be in the range of 100 to 200 mV. In this example, it is 110 mV.

One has the flexibility of choosing either R_{CS} or $R_{PH(X)}$. It is recommended to select R_{CS} equal to 100 kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 6.

$$R_{PH(x)} = R_L \times R_{CS} \times \frac{I_{LIM}}{V_{DRPMAX}}$$

$$R_{PH(x)} = 1.4 \text{ m}\Omega \times 100 \text{ k}\Omega \times \frac{110 \text{A}}{110 \text{ mV}} = 140 \text{ k}\Omega$$

The closest standard 1% value for $R_{PH(X)}$ is 140 kΩ. Next, use Equation 7 to solve for C_{CS}.

$$C_{CS} \geq \frac{600 \text{ nH}}{1.4 \text{ m}\Omega \times 100 \text{ k}\Omega} \geq 4.29 \text{ nF}$$

Choose the closest standard value that is greater than the result given by Equation 7. This example uses a C_{CS} value of 5.6 nF.

OUTPUT VOLTAGE

ADP3182 has an internal FBRTN voltage reference V_{REF} of 800 mV. The output voltage can be set up using a voltage divider made up of resistors R_{B1} and R_{B2}:

$$V_{OUT} = \frac{R_{B1} + R_{B2}}{R_{B1}} \times V_{REF} \qquad (8)$$

Rearranging Equation 8 to solve for R_{B2} using the ADP3182 with an internal FB voltage of 800 mV and assuming a 1%, 1 kΩ resistor for R_{B1} yields

$$R_{B2} = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_{B1} = \left(\frac{1.8 \text{ V}}{0.8 \text{ V}} - 1 \right) \times 1 \text{ k}\Omega = 1.25 \text{ k}\Omega$$

The closest standard 1% resistor value for R_{B2} is 1.24 kΩ.

POWER MOSFETS

For this example, one high-side, N-channel power MOSFET and two low-side, N-channel power MOSFETs per phase have been selected. The main selection parameters for the power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3418) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With V_{GATE} ~10 V, logic-level threshold MOSFETs ($V_{GS(TH)} < 2.5$ V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With the ADP3182, currents are balanced between phases, thus the current in each low-side MOSFET is the output current divided by the total number of MOSFETs (n_{SF}). With conduction losses being dominant, the following expression shows the total power being dissipated in each synchronous MOSFET in terms of the ripple current per phase (I_R) and the average total output current (I_O):

$$P_{SF} = (1-D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \, I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \qquad (9)$$

Knowing the maximum output current and the maximum allowed power dissipation, one can determine the required $R_{DS(ON)}$ for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for P_{SF} is 1 W to 1.5 W at 120°C junction temperature. Therefore, for this example,

$R_{DS(SF)}$ (per MOSFET) < 7.5 mΩ. This $R_{DS(SF)}$ is also at a junction temperature of about 120°C, so one must account for this when making this selection. This example uses a lower-side MOSFET with 4.8 mΩ at 120°C.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of feedback to input must be small (less than 10% is recommended) to prevent accidentally turning on the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the nonoverlap dead time of the MOSFET driver (40 ns typical for the ADP3418). The output impedance of the driver is approximately 2 Ω, and the typical MOSFET input gate resistances are about 1 Ω to 2 Ω; therefore, one should adhere to a total gate capacitance of less than 6000 pF. Because there are two MOSFETs in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000 pF.

The high-side (main) MOSFET must handle two main power dissipation components: conduction and switching losses. The switching loss is related to the amount of time for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \qquad (10)$$

where:
n_{MF} is the total number of main MOSFETs.
R_G is the total gate resistance (2 Ω for the ADP3418 and about 1 Ω for typical high speed switching MOSFETs, making $R_G = 3$ Ω).
C_{ISS} is the input capacitance of the main MOSFET.

Note that adding more main MOSFETs (n_{MF}) does not help the switching loss per MOSFET because the additional gate capacitance slows switching. The most efficient way to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following equation:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \qquad (11)$$

where:
$R_{DS(MF)}$ is the on resistance of the MOSFET.

Typically, for main MOSFETs, the highest speed (low C_{ISS}) device is preferred, but faster devices usually have higher on resistance. Select a device that meets the total power dissipation

ADP3182

(about 1.5 W for a single D-PAK) when combining the switching and conduction losses.

For this example, an NTD40N03L was selected as the main MOSFET (three total; n_{MF} = 3), with a C_{ISS} = 584 pF (max) and $R_{DS(MF)}$ = 19 mΩ (max at T_J = 120°C), and an NTD110N02L was selected as the synchronous MOSFET (three total; n_{SF} = 3), with C_{ISS} = 2710 pF (max) and $R_{DS(SF)}$ = 4.8 mΩ (max at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 3000 pF, satisfying that requirement. Solving for the power dissipation per MOSFET at I_O = 55 A and I_R = 6.6 A yields 894 mW for each synchronous MOSFET and 1.16 W for each main MOSFET. These numbers comply with the guideline to limit the power dissipation to around 1 W per MOSFET.

One last thing to consider is the power dissipation in the driver for each phase. This is best described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times \left(n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF} \right) + I_{CC} \right] \times V_{CC}$$

(12)

where:
Q_{GMF} is the total gate charge for each main MOSFET.
Q_{GSF} is the total gate charge for each synchronous MOSFET.

Also shown is the standby dissipation factor ($I_{CC} \times V_{CC}$) for the driver. For the ADP3418, the maximum dissipation should be less than 400 mW. In this example, with I_{CC} = 7 mA, Q_{GMF} = 9 nC, and Q_{GSF} = 46 nC, there is 165 mW in each driver, which is below the 400 mW dissipation limit. See the ADP3418 data sheet for more details.

RAMP RESISTOR SELECTION

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. The following expression is used to determine the optimum value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS(ON)(SF)} \times C_R}$$

(13)

$$R_R = \frac{0.2 \times 600 \text{ nH}}{3 \times 5 \times 4.8 \text{ mΩ} \times 5 \text{ pF}} = 333 \text{ kΩ}$$

where:
A_R is the internal ramp amplifier gain.
A_D is the current balancing amplifier gain.
$R_{DS(ON)(SF)}$ is the total low-side MOSFET on resistance.
C_R is the internal ramp capacitor value.
The closest standard 1% resistor value is 332 kΩ.

The internal ramp voltage magnitude can be calculated by using

$$V_R = \frac{A_R \times (1 - D) \times V_{OUT}}{R_R \times C_R \times f_{SW}}$$

(14)

$$V_R = \frac{0.2 \times (1 - 0.15) \times 1.8 \text{ V}}{332 \text{ kΩ} \times 5 \text{ pF} \times 250 \text{ kHz}} = 737 \text{ m V}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response improve, but thermal balance degrades. Likewise, if the ramp is made smaller, thermal balance improves but transient response and stability degrade. The factor of three in the denominator of Equation 13 sets a ramp size with optimal balance for good stability, transient response, and thermal balance.

CURRENT LIMIT SETPOINT

To select the current limit setpoint, first find the resistor value for R_{LIM}. The current limit threshold for the ADP3182 is set with a 3 V source (V_{LIM}) across R_{LIM} with a gain of 10.4 mV/μA (A_{LIM}). R_{LIM} can be found using

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{V_{DRPMAX}}$$

(15)

For values of R_{LIM} greater than 500 kΩ, the current limit may be lower than expected and therefore necessitate some adjustment of R_{LIM}. Here, I_{LIM} is the average current limit for the output of the supply. In this example, using the V_{DRPMAX} value of 110 mV from Equations 6 and 7 and choosing a peak current limit of 110 A for I_{LIM} results in R_{LIM} = 284 kΩ, for which 287 kΩ is chosen as the nearest 1% value.

The limit of the per phase current limit described earlier is determined by

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} + \frac{I_R}{2}$$

(16)

FEEDBACK LOOP COMPENSATION DESIGN

Optimized compensation of the ADP3182 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including dc.

With the multimode feedback structure of the ADP3182, the feedback compensation must be set so that the converter's output impedance, working in parallel with the output decoupling, will meet this goal. One will need to compensate for the several poles and zeros created by the output inductor and decoupling capacitors (output filter).

A type three compensator on the voltage feedback is adequate for proper compensation of the output filter. Equations 20 to 22 are intended to yield an optimal starting point for the design; some adjustments may be necessary to account for PCB and component parasitic effects.

$$C_A = \frac{C_X \times R_X}{4 \times R_{B2}} \times \frac{n \times R_X}{\dfrac{V_R}{V_{OUT}} \times R_L + A_D \times R_{DS}} \qquad (17)$$

$$R_A = \frac{4 \times R_{B2}}{n \times C_X \times R_X} \times \left(\frac{L \times V_R}{R_X \times V_{OUT}} - \frac{A_D \times R_{DS}}{2 \times f_{SW} \times R_X} \right) \qquad (18)$$

$$C_{FB} = \frac{1}{2 \times n \times f_{SW} \times R_A} \qquad (19)$$

If C_X is 6000 μF (five 1200 μF capacitors in parallel) with an equivalent ESR of 3 mΩ, the equations above give the following compensation values:

$C_A = 1.33$ nF

$R_A = 6.05$ kΩ

$C_{FB} = 110$ pF

Using the nearest standard value for each of these components yields $C_A = 1.2$ nF, $R_A = 6.04$ kΩ, and $C_{FB} = 100$ pF.

INPUT CAPACITOR SELECTION AND INPUT CURRENT di/dt

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to n × V_{OUT}/V_{IN} and an amplitude of one-nth the maximum output current. To prevent large voltage transients, a low ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{N \times D} - 1} \qquad (20)$$

$$I_{CRMS} = 0.15 \times 55\,\text{A} \times \sqrt{\frac{1}{3 \times 0.15} - 1} = 9.1\,\text{A}$$

Note that manufacturers often base capacitor ripple current rating on only 2,000 hours of life. Therefore, it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by two 2,700 μF, 16 V aluminum electrolytic capacitors and three 4.7 μF ceramic capacitors.

To reduce the input current di/dt to a level below the recommended maximum of 0.1 A/μs, an additional small inductor (L > 370 nH @ 10 A) can be inserted between the converter and the supply bus. That inductor also acts as a filter between the converter and the primary power source.

INDUCTOR DCR TEMPERATURE CORRECTION

With the inductor's DCR being used as the sense element and copper wire being the source of the DCR, one needs to compensate for temperature changes in the inductor's winding if a highly accurate safety current limit setpoint is desired. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage of change in resistance to that of the wire, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, resistors R_{CS1} and R_{CS2} are needed. See Figure 10 for instructions on how to linearize the NTC and produce the desired temperature tracking.
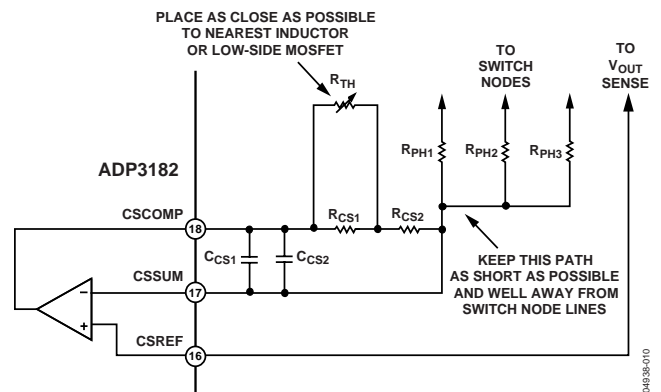

Figure 10. Temperature Compensation Circuit Values

The following procedures and expressions yield values to use for R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) for a given R_{CS} value.

1. Select an NTC based on type and value. Because we do not have a value yet, start with a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.

2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. These resistance values are called A ($R_{TH(50°C)}/R_{TH(25°C)}$) and B ($R_{TH(90°C)}/R_{TH(25°C)}$). Note that the NTC's relative value is always 1 at 25°C.

3. Find the relative value of R_{CS} required for each of these temperatures. This is based on the percentage of change needed, which in this example is initially 0.39%/°C. These are called r_1 (1/(1 + TC × (T_1 − 25))) and r_2 (1/(1 + TC × (T_2 − 25))), where TC = 0.0039 for copper. $T_1 = 50$°C and $T_2 = 90$°C are chosen. From this, one can calculate that $r_1 = 0.9112$ and $r_2 = 0.7978$.

4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using

$$r_{CS2} = \frac{(A-B) \times r_1 \times r_2 - A \times (1-B) \times r_2 + B \times (1-A) \times r_1}{A \times (1-B) \times r_1 - B \times (1-A) \times r_2 - (A-B)} \qquad (21)$$

$$r_{CS1} = \frac{(1-A)}{\dfrac{1}{1-r_{CS2}} - \dfrac{A}{r_1 - r_{CS2}}} \qquad (22)$$

$$r_{TH} = \frac{1}{\dfrac{1}{1-r_{CS2}} - \dfrac{1}{r_{CS1}}} \qquad (23)$$

5. Calculate $R_{TH} = r_{TH} \times R_{CS}$, then select the closest value of thermistor available. Also, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \qquad (24)$$

6. Calculate values for R_{CS1} and R_{CS2} using

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \qquad (25)$$

$$R_{CS2} = R_{CS} \times \left((1-k) + \left(k \times r_{CS2}\right)\right) \qquad (26)$$

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

For good results, a PCB with at least four layers is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

When high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3182) must cross through power circuitry, a signal ground plane should be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making the signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3182 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground, but it should not be tied to any other power circuitry to prevent power currents from flowing in it.

The components around the ADP3182 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins. The output capacitors should be connected as close as possible to the load or connector. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic. Avoid crossing any signal lines over the switching power path loop, described in the following section.

Power Circuitry Recommendations

To minimize radiated switching noise energy (i.e., EMI) and conduction losses in the board, the switching power path should be routed on the PCB to encompass the shortest possible length. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power-converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs, including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.

When a power-dissipating component, for example, a power MOSFET, is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias that extend to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. To optimize thermal dissipation, make a mirror image of the pads in use to heat sink the MOSFETs on the opposite side of the PCB. To further improve thermal performance, use the largest possible pad area.
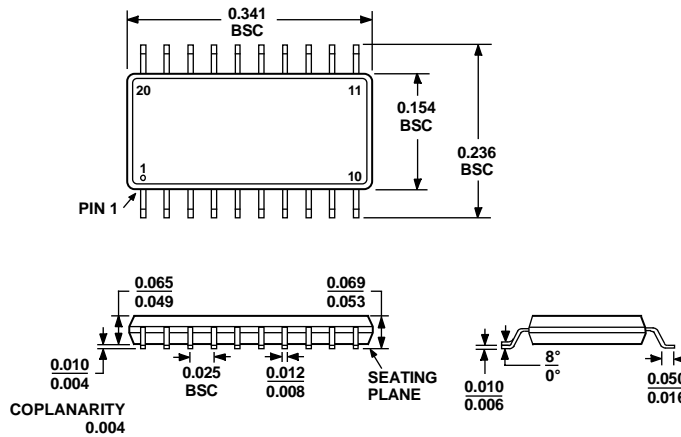
The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers, extending fully under all the power components.

Signal Circuitry Recommendations

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Therefore, the FB and FBRTN traces should be routed adjacent to each other on top of the power ground plane back to the controller. The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

OUTLINE DIMENSIONS

**0.341
BSC**

**0.154
BSC**

**0.236
BSC**

20   11

1   10

PIN 1

**0.065
0.049**

**0.069
0.053**

**0.010
0.004**

**COPLANARITY
0.004**

**0.025
BSC**

**0.012
0.008**

**SEATING
PLANE**

**0.010
0.006**

**8°
0°**

**0.050
0.016**

COMPLIANT TO JEDEC STANDARDS MO-137AD

*Figure 11. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in inches*

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Quantity per Reel
ADP3182JRQZ-RL[1]	0°C to 85°C	Shrink SOIC 13" Reel	RQ-20	2500

[1] Z = Pb-free part.

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