ANALOG DEVICES

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APPLICATION NOTE

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Asynchronous Clock Interfacing with the AD7878

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The AD7878 is a fast, complete, 12-bit A/D converter with a versatile DSP interface consisting of an 8-word, first-in, first-out (FIFO) memory and associated control logic. The FIFO memory allows up to eight samples to be digitized before the microprocessor is required to service the A/D converter. An on-chip status/control register allows the user to program the effective length of the FIFO and contains the FIFO out of range, FIFO empty and FIFO word count information.

Due to the complexity of the AD7878 internal logic, there are timing constraints which must be adhered to when performing read/write operations to the device. One method of abiding by these constraints is to use synchronous clock interfacing as recommended in the current data sheet. However, such interfacing is not suitable for every microprocessor. Another disadvantage is a possible reduction in throughput rate depending on the microprocessor clock frequency. This application note discusses the AD7878 timing constraints and shows an alternative interfacing method that is suitable for any microprocessor and will operate at any sampling frequency up to the maximum of 100 kHz.

The AD7878 is designed so that all internal logic operations are performed on a rising CLK IN edge, e.g., FIFO memory and control register updating and $\overline{\text{ALFL}}$ status output updating occur on a rising CLK IN edge. A read operation, an activity which is controlled external to the device, must be initiated around a falling CLK IN edge. Initiating a read operation (i.e., taking $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ low) on or near the rising edge of a CLK IN signal may cause the device to clock itself into an idle state with the only method of recovery being to reset the device.

There are two schemes which ensure correct timing operation when interfacing to microprocessors:

1. Synchronous clock operation.
2. Stopping the CLK IN input while reading/writing to the device.

Synchronous clock operation is covered extensively in the data sheet. Briefly, for synchronous clock operation the ADC clock must be the same as or an inverted version of the microprocessor clock out. As mentioned previously, $\overline{\text{CS}}$ and $\overline{\text{DMRD}}$ must not go low near a rising AD7878 CLK IN edge. Also, when writing to the device, the internal latch signal is the overlap between the CLK IN low signal and the $\overline{\text{CS}}$ and $\overline{\text{DMWR}}$ signals (see data sheet, page 7). To satisfy the above restrictions, the relative phase of the microprocessor CLK OUT signal and the memory control signals ($\overline{\text{CS}}$, $\overline{\text{DMRD}}$ and $\overline{\text{DMWR}}$) must be correct for synchronous operation. For example the ADSP-2100 CLK OUT can drive the AD7878 CLK IN directly; whereas, the TMS32010/32020 CLK OUT must be inverted before being applied to the AD7878.

A leading issue with synchronous interfacing is the processor CLK OUT frequency: frequencies greater than 8 MHz make synchronous interfacing impossible, e.g., ADSP-2100A and the TMS320C25 when operated at their maximum speed. Frequencies less than 8 MHz reduce the ADC's maximum throughput rate, examples of these are the TMS32010 and the TMS32020. Some processors such as the DSP56000 do not have a CLK OUT. The above issues can be avoided by using an alternative interfacing option as discussed below.

The second option is to "gate off" the ADC clock when reading/writing to the ADC. The following constraints apply when using this mode of interfacing:

1. $\overline{\text{DMRD}}$ cannot go low within 20 ns before a rising CLK IN edge or 5 ns after a rising CLK IN edge, see Figure 1.
2. When writing to the AD7878, the clock must be stopped in the low condition.
3. The clock must not be stopped during conversion or when $\overline{\text{CONVST}}$ is low.

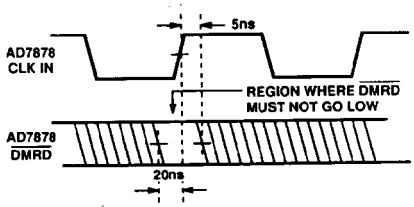

Figure 1. $\overline{\text{DMRD}}$ Asynchronous Timing Constraint

Figure 2 shows a general purpose asynchronous clock interface. The ADC clock is gated off with $\overline{CS}$ during read/write operations. To comply with constraint 1 above, the delay from $\overline{CS}$ to $\overline{DMRD}$ must be 5 ns plus the propagation through gate 1. A delay in series with the AD7878 $\overline{DMRD}$ input (shown in Figure 2) can be included to ensure a sufficient $\overline{CS}$ to $\overline{DMRD}$ setup time. The delay can be realized with a simple RC network or by inserting extra gates acting only as delays in the $\overline{DMRD}$ signal path.

The $\overline{CS}$ to $\overline{RD}$ (t_{CSRD}) delay for any processor may be found by making the following simple calculation:

$$t_{CSRD} = (t_{ADDR} - t_{RD}) - t_{PROP} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where: t_{ADDR} is the Address valid-time instant
t_{RD} is the processor $\overline{RD}$ output valid-time instant
t_{PROP} = Address decoder propagation delay

Assuming that the propagation delay of G1 is 5 ns, the $\overline{DMRD}$ delay (t_{DEL}) must be chosen such that $t_{CSRD} + t_{DEL} > 10$ ns. If t_{CSRD} is already greater than 10 ns, then the delay can be omitted. If t_{CSRD} is less than 10 ns, then $t_{DEL} = 10\text{ ns} - t_{CSRD}$.

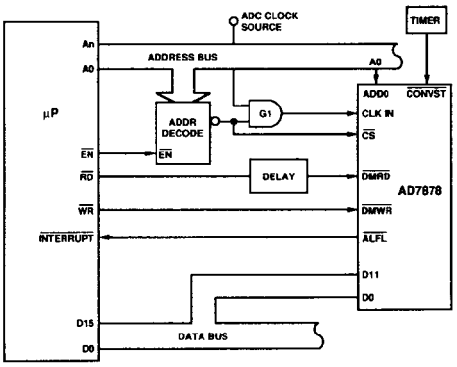

Figure 2. Asynchronous Clock Interfacing with the AD7878

INTERFACE EXAMPLES

Figures 3 to 5 show interfaces for the ADSP-2100A, TMS320C25 and the DSP56000. All three interfaces rely on a single wait state to relax the fast data access times and data setup times required by these DSP machines. The single wait state is hardware controlled for the ADSP-2100A and the TMS320C25. For the DSP56000 the wait state is software controlled by programming the bus control register.

The address valid to $\overline{RD}$ setup time ($t_{ADDR} - t_{RD}$ in Equation 1 above) can be calculated from the microprocessor timing specifications. Next, assuming an addresss decoder delay (t_{PROP}) of 10 ns and a gate propagation delay of 5 ns, it is possible to calculate the $\overline{DMRD}$ delay required for each processor interface. As an example take the ADSP-2100A, where the $t_{ADDR} - t_{RD}$ setup time is 4 ns, the $\overline{DMRD}$ delay required is 16 ns. The delay is realized with two gate propagation delays (2 × 5 ns) and a 6 ns, RC delay in Figure 3. Shown in Table I are the $t_{CSRD} - t_{RD}$ and the calculated t_{DEL} delays for the interfaces shown in this application note.

	ADSP-2100A	TMS320C25	DSP56000
$t_{ADDR} - t_{RD}$ (ns)	4	10	15
t_{DEL} (ns)	16	10	5

Table I. Processor Address Valid to $\overline{RD}$ Setup Times and AD7878 $\overline{DMRD}$ Delay Required

To the processor the interface is similar to synchronous interfacing. The ADC asserts the processor interrupt input when its internal FIFO memory has reached the preprogrammed word count, and then the conversion results are read from the ADC. Data transfers are not allowed during conversion.

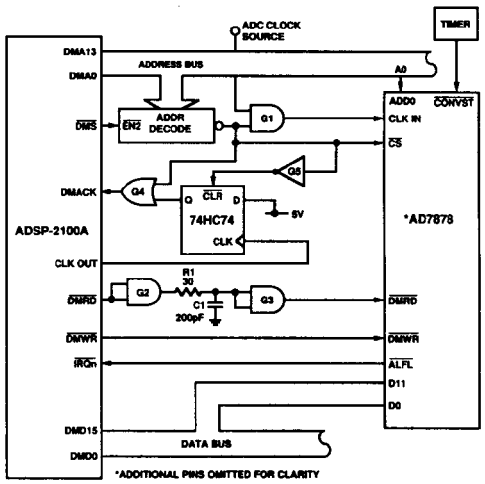

Figure 3. ADSP-2100A–AD7878 Asynchronous Clock Interface

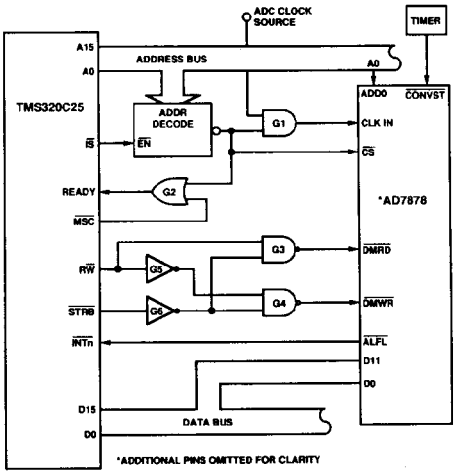

Figure 4. TMS320C25–AD7878 Asynchronous Clock Interface

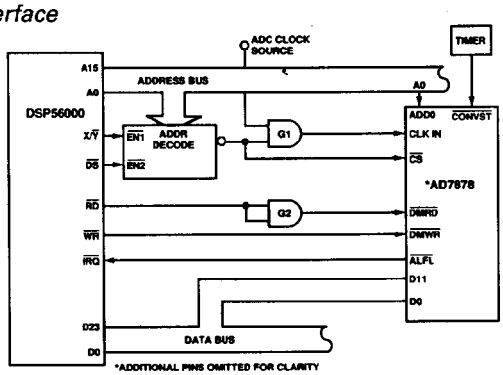

Figure 5. DSP56000–AD7878 Asynchronous Clock Interface