Ultracompact 4A, 15V, Full Bridge Driver with SPI

FEATURES

- **25-Bit Digital Output Voltage Control**
- **Wide Input Voltage Range: 3.1V to 15V**
- **±4A Output Current**
- **High Output Power: Up to 54W[1]**
- **High Efficiency at High Frequency**
  - **92.6% Efficiency at 4A, 15V_{IN}, f_{SW} = 3MHz**
- **SPI Interface Allows User to:**
  - **Set Output Regulation Voltage**
  - **Set Output Current Limits**
  - **Check Device Status**
  - **Enable/Disable Output**
- **Integrated 4A Power Switches**
- **Silent Switcher® Architecture**
- Analog Output for Diagnostics/Telemetry
- Adjustable and Synchronizable: 500kHz to 3MHz
- Small 3mm × 3mm 18-Lead LQFN

APPLICATIONS

- Driving a Thermo Electric Cooler (TEC) with Fine Control
- Transmit Optical Sub-Assembly (TOSA) Cooling
- Erbium Doped Fiber Amplifier (EDFA) Temperature Regulation
- Photonic Integrated Circuit (PIC) Cooling
- LiDAR Mirror Control
- Motor Control

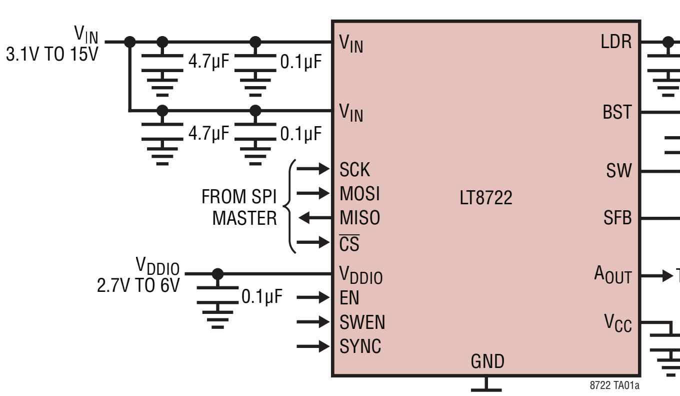
DESCRIPTION

The LT®8722 is a high performance, high efficiency, monolithic full bridge DC/DC converter. One side of the full bridge is driven by a pulse width modulation (PWM) buck power stage, while the other side of the full bridge is driven by a linear power stage. The LT8722 can deliver up to ±54W[1] of power to its load while only requiring a single inductor. An integrated 25-bit digital-to-analog converter (DAC) is used to control the LT8722 output voltage. Two additional 9-bit DACs control the positive and negative output current limits. An analog output telemetry pin can be used to monitor SPI selectable parameters such as V_{IN}, V_{OUT}, I_{OUT} or the LT8722 junction temperature. The serial peripheral interface (SPI) can be used to configure and control the LT8722 allowing for flexibility to set the desired output voltage, output current limits, voltage limits, switching frequency and control ON/OFF behavior. The SPI operates at up to 10MHz allowing for fast readback and control. The LT8722 operates from a single 3.1V to 15V supply. Silent Switcher techniques are used to minimize EMI/EMC emissions while delivering high efficiency at high switching frequencies. The LT8722 is available in a 3mm × 3mm LQFN package.

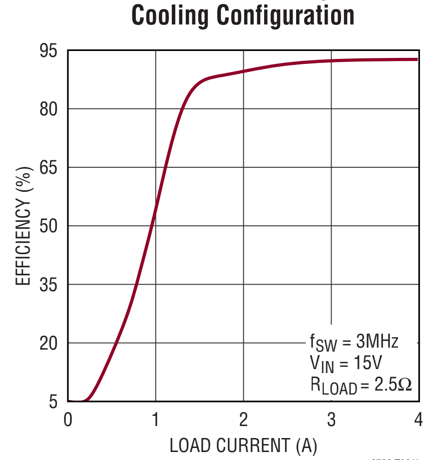
[1] V_{TEC} = ±13.5V/±4A with V_{IN} = 15V, f_{SW} = 1MHz

TYPICAL APPLICATION

±13.5V/±4A TEC Driver



Electrical Efficiency in Cooling Configuration



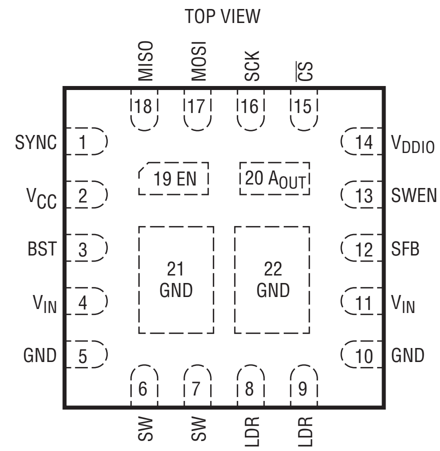
Rev. A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SFB, LDR, EN, SW .... –0.3V to 15V
SWEN, SYNC .... –0.3V to 6V
V_{CC} .... –0.3V to 3.8V
V_{DDIO}, SCK, MOSI, $\overline{CS}$ .... –0.3V to 6V
A_{OUT} .... –0.3V to 6V
MISO .... –0.3V to 6V
BST–SW .... –0.3V to 6V
Operating Junction Temperature Range (Note 2)
LT8722A .... –40°C to 125°C
ABSMAX T_J .... –40°C to +150°C
Storage Temperature Range .... –65°C to 150°C
Maximum Reflow (Package Body) Temperature ... 260°C

PIN CONFIGURATION



LQFN PACKAGE
18-LEAD (3mm × 3mm × 0.95mm)
J_A = 42°C/W, /J_B = 14°C/W
$J_{CBOTTOM}$ = 9°C/W, θJ_{CTOP} = 62°C/W, Ψ_{JT} = 1.25°C/W
AND Ψ VALUES DETERMINED PER JESD51-12
EXPOSED PADS (PINS 19-22) MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	PAD FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LT8722AV#PBF	Au (RoHS)	LHMC	e4	18 Lead (3mm × 3mm) LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

Rev. A

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supplies						
V_{IN} Supply Voltage		●	3.1		15	V
V_{IN} Quiescent Current	EN = 0V			15		µA
				2.8		mA
V_{DDIO} Supply Voltage	Linear Power Stage ON with LDR Floating	●	2.7		5.5	V
I_{VDDIO} Supply Shutdown Current	EN = 0V, V_{DDIO} = 2.7V, MOSI/$\overline{CS}$/SCK = 0V		0.1	0.21	0.35	mA
I_{VDDIO} Supply Shutdown Current	EN = 0V, V_{DDIO} = 5.5V, MOSI/$\overline{CS}$/SCK = 0V		0.1	0.27	0.45	mA
IV_{DDIO} Supply Current	EN = 15V, Linear Power Driver ON with V_{TEC} = 0, V_{DDIO} = 2.7V	●	1.1	2	3.2	mA
IV_{DDIO} Supply Current	EN = 15V, Linear Power Driver ON with V_{TEC} = 0, V_{DDIO} = 5.5V	●	1.7	2.8	4.2	mA
Internal Regulator (V_{CC} Pin)						
V_{CC} Regulator Output Voltage 1	SPIS_COMMAND[9] = 1			3.473		V
V_{CC} Regulator Output Voltage 2	SPIS_COMMAND[9] = 0			3.149		V
V_{CC} When Overdriven	If V_{CC} Driven from External Supply Set SPIS_COMMAND[9] = 0	●	3.4		3.8	V
V_{CC} Supply Current at 3.4V	If V_{CC} Driven from External Supply Set SPIS_COMMAND[9] = 0			3.1		mA
V_{CC} Supply Current at 3.8V	If V_{CC} Driven from External Supply Set SPIS_COMMAND[9] = 0			3.3		mA
V_{CC} Regulator Output Voltage 3	V_{IN} = 3.1V, External V_{CC} Load = 20mA	●	2.7	2.9	3.1	V
V_{CC} Current Limit	V_{IN} = 5V			66		mA
Enable Control						
EN Pin Threshold	EN Rising	●	0.475	0.66	0.82	V
EN Pin Hysteresis				52		mV
EN Pin Leakage Current	EN = 15V	●	–1	0	1	µA
Switching Enable Control						
SWEN Pin Threshold	SWEN Rising	●	1.14	1.2	1.26	V
SWEN Pin Hysteresis				21		mV
SWEN Pin Pull-Down Current	SWEN = 0.25V			406		µA
SWEN Pin Leakage Current	SWEN = 5.5V, SPIS_STATUS = 0	●	10	28	55	µA
Undervoltage Lockout (UVLO)						
V_{CC} UVLO Rising Threshold		●	1.9	2.36	2.65	V
Hysteresis				90		mV
V_{DDIO} UVLO Rising Threshold		●	2.25	2.425	2.7	V
Hysteresis				110		mV

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Linear Output Stage						
On-Resistance						
Top MOSFET (M1)	V_{IN} = 15V, I_{LDR} = 1.5A V_{IN} = 3.1V, I_{LDR} = 1.5A			38 40		mΩ mΩ
Bot MOSFET (M2)	V_{IN} = 15V, I_{LDR} = 1.5A V_{IN} = 3.1V, I_{LDR} = 1.5A			38 40		mΩ mΩ
LDR Pin Leakage Current	V_{IN} = 15V, LDR = 0V			13.6		µA
LDR Current Sink Limit		●	–6.7	–4.8	–4	A
LDR Current Source Limit		●	4	5.6	7.5	A
LDR Zero Voltage	SPIS_DAC = 0x0, SYS_DC[1:0] = 2b11, I_{TEC} = 0A, ENABLE_REQ = 1			7.5		V
Linear Power Loss Limit Regulation						
Regulation Power for 2W Option	M1 MOSFET, Sourcing Current			2.07		W
	M2 MOSFET, Sinking Current			2.225		W
Regulation Power for 3W Option	M1 MOSFET, Sourcing Current			2.7		W
	M2 MOSFET, Sinking Current			3.0		W
Regulation Power for 3.5W Option	M1 MOSFET, Sourcing Current			3.4		W
	M2 MOSFET, Sinking Current			3.8		W
PWM Output Stage						
On-Resistance	M3, I = 1.5A			38		mΩ
	M4, I = 1.5A			40		mΩ
SW Pin Leakage Current	V_{SW} = 15V		–1	0	1	µA
	V_{SW} = 0V			500		µA
Min SW On-Time	Internal Clock, I_{SW} = 4A			40		ns
Min SW Off-Time	Internal Clock, I_{SW} = 1A			37		ns
	External Clock, I_{SW} = 1A			37		ns
M3 Source Current Limit	V_C, Max		7	10	12	A
M3 Sink Current Limit	V_C, Min		–8	–6	–4.5	A
M4 Sink Current Limit	V_C, Min		–10.5	–8.2	–6.5	A
PWM Oscillator Frequency						
Internal Frequency Accuracy	f_{SW} = 500kHz	●	459	510	561	kHz
	f_{SW} = 3000kHz	●	2643	2936	3420	kHz
Internal Frequency Increment	f_{SW} = 500kHz, SW_FRQ_ADJ[1:0] = 2b01			+14.8		%
	f_{SW} = 3000kHz, SW_FRQ_ADJ[1:0] = 2b01			+12.7		%
Internal Frequency Decrement	f_{SW} = 500kHz, SW_FRQ_ADJ[1:0] = 2b10			–15.4		%
	f_{SW} = 3000kHz, SW_FRQ_ADJ[1:0] = 2b10			–13.7		%
SYNC Pin Logic Threshold	Logic High		1.6			V
	Logic Low				0.45	V
SYNC Pin Leakage Current	V_{SYNC} = 0V	●	–0.2	0	0.2	µA
	V_{SYNC} = V_{CC}	●	0	10	30	µA

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Duty Control						
20%~80% Duty Option						
Max V_{SFB}/V_{IN} Ratio		●		80	82.5	%
Min V_{SFB}/V_{IN} Ratio		●	17.5	20		%
15%~85% Duty Option						
Max V_{SFB}/V_{IN} Ratio		●		85	89	%
Min V_{SFB}/V_{IN} Ratio		●	13.5	15.6		%
10%~90% Duty Option						
Max VSFB/V_{IN} Ratio		●		89.6	93	%
Min VSFB/V_{IN} Ratio		●	8	10.9		%
Positive Current Limit DAC (Note 4)						
Resolution				9		Bits
LSB				13.3		mA
Minimum Code				0		Code
Maximum Code				462		Code
Positive Current Limit Accuracy 1	SPIS_DAC_ILIMP = 0x96, I_{LIMP} =150 • 13.3mA			2.157		A
Positive Current Limit Accuracy 2	SPIS_DAC_ILIMP = 0x12C, I_{LIMP} = 300 • 13.3mA			4.157		A
Negative Current Limit DAC (Note 4)						
Resolution				9		Bits
LSB				13.3		mA
Minimum Code				48		Code
Maximum Code				511		Code
Negative Current Limit Accuracy	SPIS_DAC_ILIMN = 0x169, I_{LIMN} = (361–511) • 13.3mA			–2.116		A
Negative Current Limit Accuracy	SPIS_DAC_ILIMN = 0xD3, I_{LIMN} = (211–511) • 13.3mA			–4.077		A
Output Voltage Setpoint DAC						
Resolution (No Missing Codes)	(Note 5)			25		Bits
VDAC INL			–900	105	900	µV
V_{OUT} Gain Adjust, Ga	$V_{OUT} = V_{LDR}–V_{SFB}$			0.969		V/V
V_{OUT} Regulation Accuracy	$V_{OUT} = V_{LDR}–V_{SFB}$, V_{IN} = 15V, I_{LDR} = 0A					
V_{OUT} < 0	SPIS_DAC = 0xFFB20000, V_{OUT} = –11927552/2^{24} • 1.25 • 16 • Ga			–13.818		V
V_{OUT} = 0	SPIS_DAC = 0x00000000, V_{OUT} = 0/2^{24} • 1.25 • 16 • Ga			0		V
V_{OUT} > 0	SPIS_DAC = 0x00E00000, V_{OUT} = 11927552/2^{24} • 1.25 • 16 • Ga			13.819		V

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{OUT} Analog Monitor						
V_{ILIMP_ZERO}	SPIS_DAC_ILIMP = 0x200, I_{LIMP} = (512–512) • 13.3mA = 0A. V_{ILIMP} = V_{1P65} + I_{LIMP}/8, SPIS_AMUX = 0x40			1.665		V
V_{ILIMP_MID}	SPIS_DAC_ILIMP = 0x294, I_{LIMP} = (660–512) • 13.3mA = 1.9684A. V_{ILIMP} = V_{1P65} + I_{LIMP}/8, SPIS_AMUX = 0x40			1.913		V
V_{ILIMP_HIGH}	SPIS_DAC_ILIMP = 0x318, I_{LIMP} = (792–512) • 13.3mA = 3.724A. V_{ILIMP} = V_{1P65} + I_{LIMP}/8, SPIS_AMUX = 0x40			2.135		V
V_{ILIMN_ZERO}	SPIS_DAC_ILIMN = 0x1FF, I_{LIMP} = (511–511) • 13.3mA = 0A. V_{ILIMP} = V_{1P65} + I_{LIMP}/8, SPIS_AMUX = 0x41			1.663		V
V_{ILIMN_MID}	SPIS_DAC_ILIMN = 0x174, I_{LIMP} = (372–511) • 13.3mA = –1.8487A. V_{ILIMP} = V_{1P65} + I_{LIMP}/8, SPIS_AMUX = 0x41			1.429		V
V_{ILIMN_HIGH}	SPIS_DAC_ILIMN = 0xF8, I_{LIMP} = (248–511) • 13.3mA = –3.4979A. V_{ILIMP} = V_{1P65} + I_{LIMP}/8, SPIS_AMUX = 0x41			1.221		V
$A_{OUT\_DAC\_NEG}$	SPIS_DAC = 0x00E00000, $A_{OUT\_DAC\_NEG}$ =1.8 • V_{1P25} - 0.8 • V_{DAC}, SPIS_AMUX=0x42			1.51		V
$A_{OUT\_DAC\_ZERO}$	SPIS_DAC = 0x00000000, $A_{OUT\_DAC\_ZERO}$ =1.8 • V_{1P25} - 0.8 • V_{DAC}, SPIS_AMUX=0x42			1.263		V
$A_{OUT\_DAC\_POS}$	SPIS_DAC = 0xFF100000, $A_{OUT\_DAC\_POS}$ =1.8 • V_{1P25} - 0.8 • V_{DAC}, SPIS_AMUX=0x42			0.991		V
A_{VOUT_NEG}	SPIS_DAC = 0xFFB20000, V_{OUT} = –11927552/224 • 1.25 • 16 • Ga = –13.792V A_{OUT} = V_{1P25}–V_{OUT}/16, SPIS_AMUX = 0x43			2.125		V
A_{VOUT_ZERO}	SPIS_DAC = 0x00000000, V_{OUT} = 0V, SPIS_AMUX = 0x43			1.259		V
$A_{OUT\_DAC\_POS}$	SPIS_DAC = 0x00E00000, V_{OUT} = +11927552/224 • 1.25 • 16 • Ga = 13.792V A_{OUT} = V_{1P25}–V_{TEC}/16, SPIS_AMUX = 0x43			0.394		V
Output Current, V_{IMON}	I_{LDR} = –1A. A_{OUT} = V_{1P65} + I_{LDR}/10, SPIS_AMUX = 0x44			1.538		V
	I_{LDR} = 0A. A_{OUT} = V_{1P65} + I_{LDR}/10, SPIS_AMUX = 0x44			1.666		V
	I_{LDR} = 1A. A_{OUT} = V_{1P65} + I_{LDR}/10, SPIS_AMUX = 0x44			1.799		V
A_{OUT_2P5V}	A_{OUT} = 0.6 • V_{2P5}, SPIS_AMUX = 0x45			1.5138		V
A_{OUT_1P25V}	A_{OUT} = V_{1P25}, SPIS_AMUX = 0x46			1.26		V
A_{OUT_1P65V}	A_{OUT} = V_{1P65}, SPIS_AMUX = 0x47			1.665		V
Temp Sense Voltage at 25°C	Die Temp = (A_{OUT} –1.4207)/0.0047148, SPIS_AMUX = 0x48			1.543		V
A_{OUT_VIN}	V_{IN} = 15V, A_{OUT} = 0.9 • V_{2P5}–V_{IN}/8, SPIS_AMUX = 0x49			0.3933		V
A_{OUT_VCC}	V_{CC} = 3.4V, A_{OUT_VCC} = 0.4 • V_{CC}, SPIS_AMUX = 0x4A			1.36		V
A_{OUT_VDDIO}	V_{DDIO} = 3.3V, SPIS_AMUX = 0x4B, A_{OUT} = 0.4 • V_{DDIO}			1.32		V
A_{OUT_VSFB}	V_{SFB} = 15V, SPIS_AMUX = 0x4C, A_{OUT} = (16/17) • V_{1P25} + $V_{SFB/17}$			2.072		V

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Serial Bus Interface and Timing Characteristics						
$\overline{CS}$, SCK, MOSI Input High Logic Level		●	0.7•V_{DDIO}			V
$\overline{CS}$, SCK, MOSI Input Low Logic Level		●			0.3•V_{DDIO}	V
MISO Output Low Level	I_{SINK} = 1mA, V_{DDIO} = 3.3V, 5V	●			0.4	V
MISO Output High Level	I_{SOURCE} = 1mA, V_{DDIO} = 3.3V, 5V	●	V_{DDIO}–0.4			V
SCK Clock Period		●	100			ns
SCK Pulse High Time		●	40			ns
SCK Pulse Low Time		●	40			ns
$\overline{CS}$ Falling to SCK Rising Delay Time		●	45			ns
SCK Falling to $\overline{CS}$ Rising Delay Time		●	45			ns
$\overline{CS}$ High Time		●	20			ns
MOSI to SCK	See T_{DS} in the timing diagram	●	12.5			ns
MOSI to SCK	See T_{DH} in the timing diagram	●	12.5			ns
SCK to MISO, 80pF Load		●			27.5	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: LT8722A is specified over the –40°C to 125°C operating junction temperature range. High Junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

Note 4: Current flow out of LDR and into SFB is regarded as being positive.

Note 5 : Guaranteed by design, not subject to test.

TIMING DIAGRAM

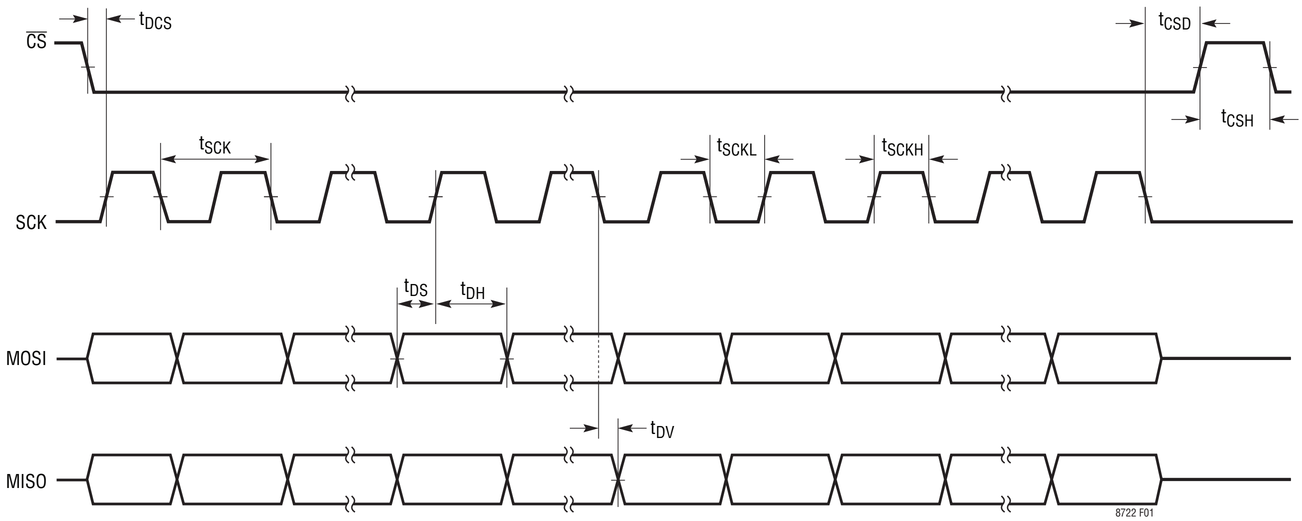
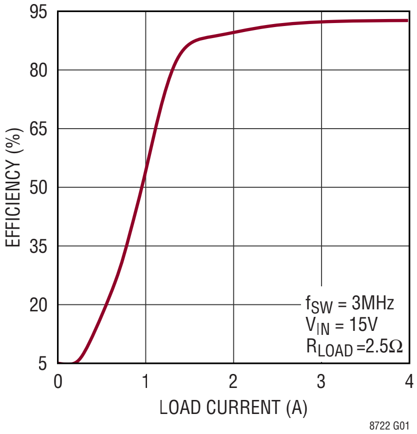


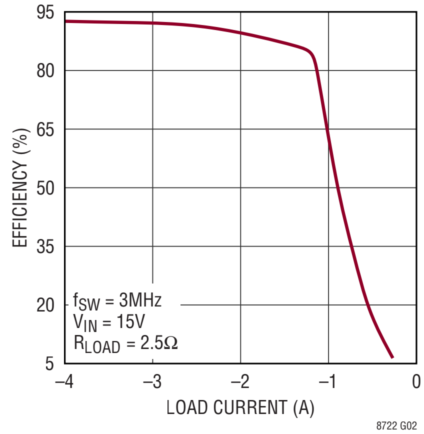
Figure 1. Timing Diagram for SPI

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

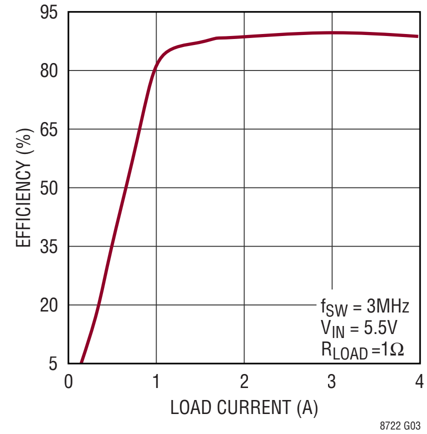
Electrical Efficiency in Cooling Configuration, V_{IN} = 15V



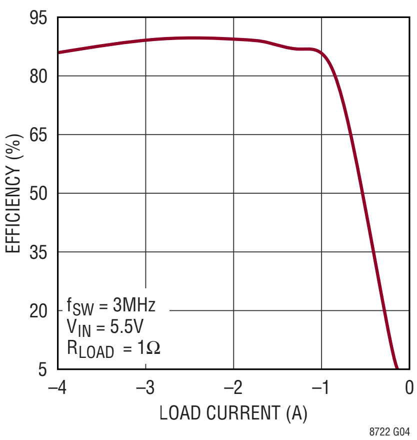
Electrical Efficiency in Heating Configuration, V_{IN} = 15V



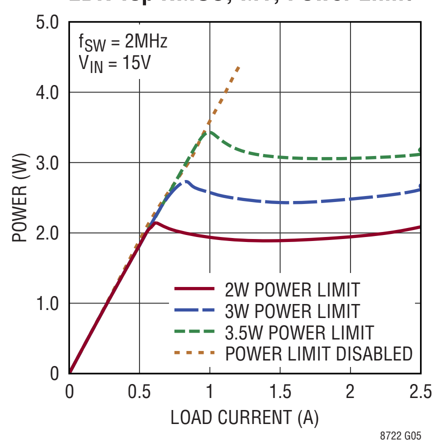
Electrical Efficiency in Cooling Configuration, V_{IN} = 5.5V



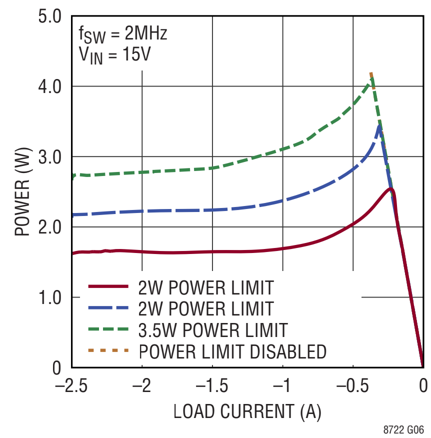
Electrical Efficiency in Heating Configuration, V_{IN} = 5.5V



LDR Top NMOS, M1, Power Limit



LDR Bottom NMOS, M2, Power Limit



PIN FUNCTIONS

V_{IN} (Pins 4 and 11): Input Supply Pins. The V_{IN} pins supply current to the LT8722 internal circuitry, the linear power stage as well as the buck power stage. Bypass these pins to ground with two 4.7µF capacitors and two 0.1µF capacitors as shown in Figure 15.

GND (Pins 5, 10, 21 and 22): Ground Pins. Tie directly to local ground plane.

SW (Pins 6 and 7): Switch Pins. The SW pins are the outputs of the buck stage's internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance and low EMI.

LDR (Pins 8 and 9): Linear Drive Pins. The LDR pins are the outputs of the linear stage's internal power switches. Tie these pins together.

V_{CC} (Pin 2): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. Do not load the V_{CC} pin with external circuitry.

SYNC (Pin 1): Synchronization Pin. Clocking Modes: 1) Drive this pin with a clock source to synchronize to an external frequency. 2) Tie this pin to GND to use the internal oscillator.

V_{DDIO} (Pin 14): Serial Interface Supply Pin. The range of V_{DDIO} is 2.7V to 5.5V. Use a minimum 0.1µF local bypass capacitor to GND on this pin.

EN (Pin 19): The LT8722 is in shutdown when both EN pin and ENABLE_REQ SPI bit are low. The LT8722 is active when either the EN pin is high or the ENABLE_REQ is high. The V_{CC} regulator is on when the LT8722 is active. The hysteretic threshold voltage is 0.66V going up and 0.61V going down. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the EN pin will be considered low. Tie EN to GND if the EN pin is not used. This option may allow a more substantial PCB ground connection under the LT8722, thereby keeping the LT8722 junction temperature cooler. Do not float this pin.

SWEN (Pin 13): The SWEN pin is an input/output pin. The LT8722 switching behavior can be enabled when this pin is high and is disabled when this pin is low. This pin is pulled low internally by the LT8722 when the LT8722 detects a fault. This pin can also be pulled low by an external circuit. See the Driving the SWEN Pin section for further information.

$\overline{CS}$ (Pin 15): Chip Select Input Pin. The serial data I/O bus is enabled when $\overline{CS}$ is low and disabled when $\overline{CS}$ is high.

MISO (Pin 18): Serial Data Output Pin. Output data formatting is described in the Applications Information section.

MOSI (Pin 17): Serial Data Input Pin. Drive this pin with the desired configuration as described in the Applications Information section.

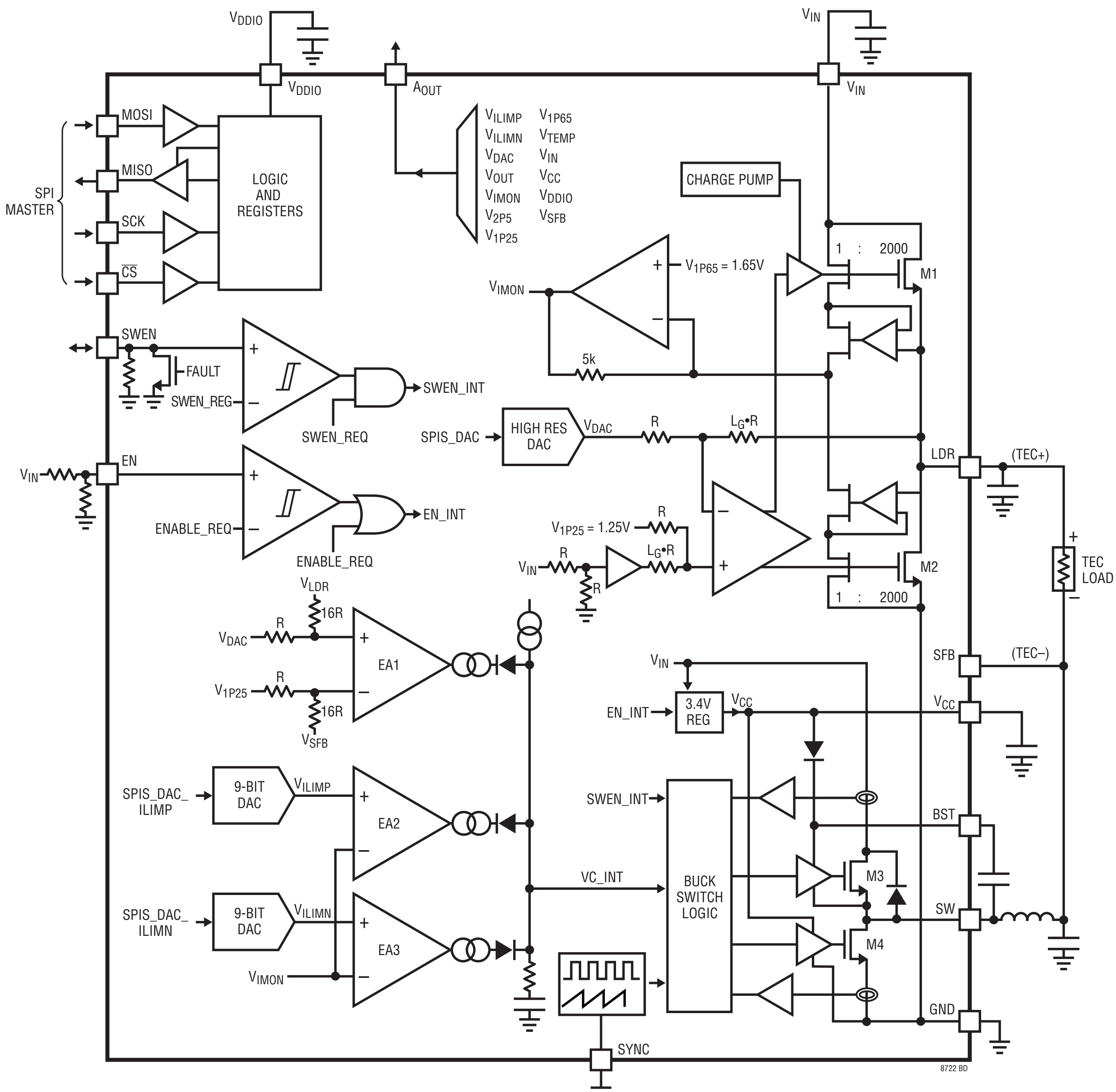
SCK (Pin 16): Serial Clock Input Pin. Drive SCK with the serial I/O clock. SCK rising edges latch serial data in on the MOSI. Capture output data from the MISO on rising edges of SCK.

BST (Pin 3): Boost Pin. This pin is used to provide a drive voltage, higher than the input voltage, to the buck stage's topside power switch (M3). Place a 0.1µF boost capacitor from this pin to the SW pin as close to the IC as possible.

SFB (Pin 12): Switcher Feedback Pin. This pin provides feedback to the buck stage for regulating the output voltage.

AOUT (Pin 20): Analog Output Pin. Internal analog signals can be buffered out to this pin by sending commands through the digital serial interface. See the Applications Information section for more information.

BLOCK DIAGRAM



OPERATION

The LT8722 is a monolithic, fixed-frequency, current-mode, full bridge DC/DC converter. Utilizing a hybrid drive system, where one side of the load employs a linear drive (LDR) while the other side of the load employs a traditional PWM switching drive (SFB). Due to this unique architecture, only a single inductor and output capacitor are required to achieve traditional full bridge drive capability.

The LT8722 comes equipped with a serial peripheral interface (SPI). Using the SPI, a 25-bit digital control word can be applied to the LT8722 to achieve a desired voltage at the converter output. Additional digital control information can be sent and received through the SPI to achieve the desired current limits, power limits as well as read back device status information. Setting the switching frequency of the LT8722 is also accomplished with sending of SPI commands. Alternatively, an external clock can be applied to the SYNC pin forcing the switching regulator drive to operate at the externally applied clock frequency.

If the EN pin is low and the ENABLE_REQ control bit is low, the LT8722 is shut down and draws ~15µA from the input. When the EN pin is above 0.74V or the ENABLE_REQ control bit is set high, the LT8722 will become powered on waiting for additional SPI commands to operate begin switching. When driving the SWEN pin above 1.25V and setting the SWEN_REQ control bit high, the LT8722 will begin a switching start-up sequence further detailed in the Applications Information section of this document.

Electrical efficiency for the LT8722 is given by Equation 1.

$$\text{Electrical Efficiency} = 100\% \bullet \frac{\text{Electrical Power Delivered to LT8722 } V_{OUT} \text{ Load}}{\text{LT8722 Electrical Input Power}} \quad (1)$$

To improve efficiency across all loads, supply current to the internal circuitry can be sourced through the V_{CC} pin by reducing the V_{CC} voltage output to 3.1V via SPI control and overdriving V_{CC} with 3.3V to 5.5V. Otherwise, the V_{CC} voltage should be programmed to 3.4V and internal circuity will draw current directly from V_{IN}.

The use of the analog output telemetry (AOUT) pin on the LT8722 is optional. This output pin can be used in conjunction with an external ADC to obtain information about various aspects of the LT8722 operation including V_{IN}, V_{LOAD}, I_{LOAD}, die temp, etc. These outputs and their scaling equations are included in the Applications Information section of this document.

ENABLE AND STARTUP SEQUENCE

The LT8722 is in shutdown mode with ultralow quiescent current when both the EN pin is low and the ENABLE_REQ register bit is low. The V_{CC} LDO regulator can be activated by either pulling the EN pin high or by setting the ENABLE_REQ bit high through the SPI. The rising threshold of the EN pin comparator is 0.74V with 30mV of hysteresis.

To enable the linear driver, the SPIS_STATUS register must be cleared. This is done by writing all SPIS_STATUS registers to a value of 0. The output current monitoring circuitry and integrated charge pump, which powers the linear power stage's top MOSFET, are enabled when the ENABLE_REQ bit is high. Clearing the latched CP_UVLO bit is required to enable the linear power driver.

Finally, the PWM driver is enabled by applying a logic high voltage to the SWEN pin (through a series 20k, or greater, resistor) and writing the SWEN_REQ register to a 1.

During LT8722 start-up, large inrush currents can occur. Using proper SPI commands and wait times, a software controlled soft-start function can be synthesized that keeps inrush current to a minimum. The following statements encompass the recommended start-up sequence:

- First, apply proper V_{IN} and V_{DDIO} voltages to the LT8722.
- Second, enable the V_{CC} LDO and other LT8722 circuitry by raising the EN pin above the 0.74V threshold and writing the ENABLE_REQ bit to a 1.
- Third, configure the output voltage control DAC (SPIS_DAC) to 0xFF000000. This code will force the LDR pin to GND when the linear power stage is later enabled.
- Fourth, write all SPIS_STATUS registers to 0. This clears all faults and allows the linear power stage to be enabled. Due to the actions in the prior step, when the linear power stage turns on in this step, the output load will be discharged to GND. Pause between this step and the next for ~1ms to allow any prebiased output condition to dissipate.

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- Fifth, ramp the output voltage control DAC (SPIS_DAC) from code 0xFF000000 to code 0x00000000 in a controlled manner so that the linear driver output (LDR) ramps from GND to $V_{IN}/2$. During this ramping period, both the PWM driver output (SFB) and linear driver output (LDR) move together to $V_{IN}/2$. The ramp time for this controlled movement to $V_{IN}/2$ should be a minimum of 5ms.
- Sixth, enable the PWM switching behavior by raising the SWEN pin above the 1.2V (typ) threshold and writing the SWEN_REQ bit to a 1. With both output terminals at $V_{IN}/2$, the inrush current through the output load is greatly minimized. After the PWM driver switching activity is enabled, keep the output voltage control DAC (SPIS_DAC) code unchanged for a minimum of 160µs.
- Finally, the output voltage control DAC (SPIS_DAC) code can be stepped in a controlled manner to the desired code. The LDR and SFB outputs will begin to diverge from one another until the desired differential voltage is developed across the output load, the differential output voltage reaches the preset voltage limit, or the output current reaches the preset current limit.

Figure 2 shows the flow chart of the enable sequence and Figure 3 shows an example of the soft-start profile where the instruction about soft-start guidance is followed.

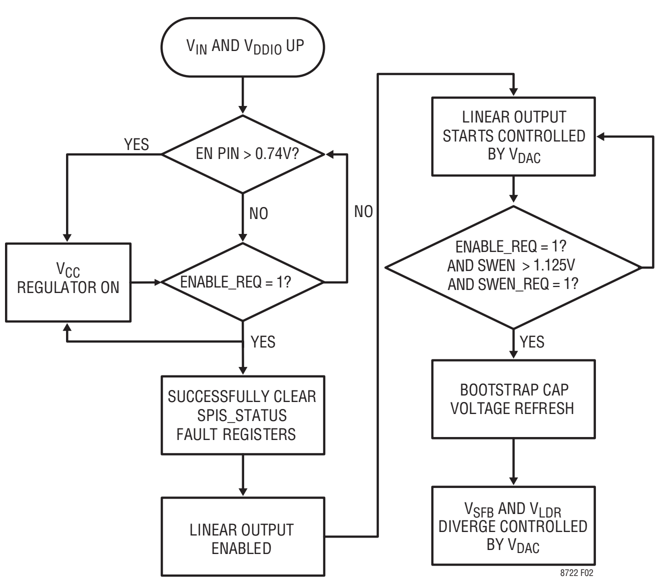

Figure 2. Flow Chart of Start-Up Sequence

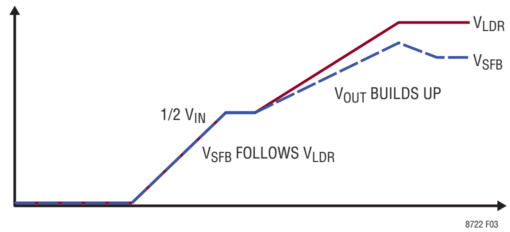

Figure 3. Soft-Start Profile in Cooling Mode

POWERING THE DRIVERS

The LT8722 operates at an input voltage range of 3.1V to 15V that is applied to the V_{IN} pin and an input range of 2.7V to 6V that is applied to the V_{DDIO} pin.

The V_{IN} pin is the power supply for the PWM driver and the linear power driver. When configuring the power supply to the V_{IN} pin keep in mind that, at high current loads, the input voltage may drop substantially due to a voltage drop in the wires between the front end power supply and the V_{IN} pin. Leave a proper voltage margin when designing the front-end power supply to maintain good performance. Minimize the trace length from the power supply to the V_{IN} pin to help mitigate the voltage drop.

SETTING THE SWITCHING FREQUENCY

The LT8722 uses a constant frequency PWM architecture that can be programmed to switch from 500kHz to 3MHz through the SW_FRQ_SET register bits and further be adjusted by ±15% through the SW_FRQ_ADJ register bits. Table 1 and Table 2 show the frequency setup summary.

Table 1. Switching Frequency Configuration

SW_FRQ_SET BITS	SWITCHING FREQUENCY
000	500kHz
001	1MHz
010	1.5MHz
011	2MHz
100	2.5MHz
101, 110, 11	3.0MHz

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Table 2. Switching Frequency Adjustment

SW_FRQ_ADJ BITS	CHANGE FROM NOMINAL
00	0%
01	+15%
10	–15%
11	0%

The operating frequency of the LT8722 PWM buck driver can also be synchronized to an external source automatically.

To synchronize to the external source, simply provide a digital clock signal into the SYNC pin and the LT8722 will operate at the SYNC clock frequency. The duty cycle of the SYNC clock must be between 20% and 80% for proper operation. And the SYNC frequency can always be higher than the free-running oscillator frequency but should not be less than 30% of the configured free-running oscillator frequency.

Selection of the operating frequency is a trade-off between efficiency, component size and PWM duty cycle range. The advantage of high frequency operation is that lower value and smaller size inductors and capacitors can be used. The disadvantages are lower efficiency and narrower duty cycle range as required by the min-on time and min-off time of the PWM driver.

BOOTSTRAP CIRCUITRY AND REFRESH PERIOD

The LT8722 integrates the bootstrap regulator to provide gate drive voltage for the top MOSFET of the PWM driver (M3). The regulator generates a bootstrap voltage between the BST pin and the SW pin, which is equal to the V_{CC} voltage.

It is recommended that an X7R or an X5R, 0.1µF ceramic capacitor is placed between the BST pin and the SW pin.

Immediately after enabling the PWM driver, the bootstrap capacitor voltage may not be high enough to drive the M3 gate. A total of 32 refresh cycles, with 5µs period, are required to charge the bootstrap capacitor before the PWM driver starts to work properly. During each refresh cycle, the M3 MOSFET is designed to be turned on first for 80ns (typ), and then the M4 MOSFET is turned on for 160ns (typ). After that, both the top and bottom MOSFETs are turned off for the rest of the refresh cycle. By doing this, the inrush load current is minimized. Figure 4 shows the typical waveforms during the bootstrap cap voltage refresh period.

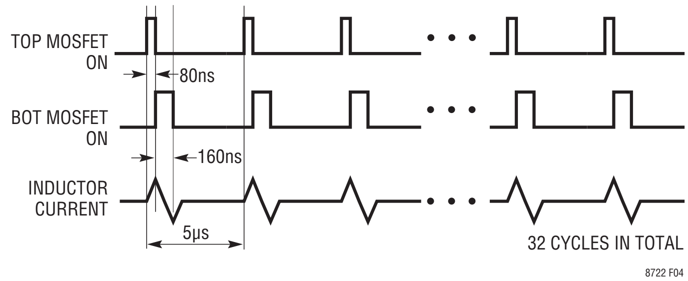

Figure 4. Bootstrap Capacitor Voltage Refresh Cycles

V_{CC} LDO REGULATOR

An internal low dropout (LDO) regulator produces a 3.4V supply to the V_{CC} pin from V_{IN} when the VCC_VREG register bit is 1. This LDO can supply enough current for the LT8722's circuitry and must be bypassed to ground with a minimum 1µF ceramic capacitor. This bypassing is necessary to supply the high transient currents required by the PWM power MOSFET drivers.

To improve overall efficiency, an external supply between 3.4V to 3.8V can be applied to the V_{CC} pin. When an external supply is used, the VCC_VREG register bit needs to be configured to 0. With this setting, the V_{CC} LDO's regulation voltage will be reduced to 3.1V. The V_{CC} pin can then be overdriven with an external supply between 3.4V and 3.8V. Because the V_{CC} target output voltage is 3.1V and because the V_{CC} LDO can only source current, only the external supply will control the V_{CC} pin in this situation.

SETTING INITIAL PEAK INDUCTOR CURRENT

When the PWM driver is enabled, the initial peak inductor current can cause some transient behavior to the output voltage and current for a short period of time. The optimal initial peak inductor current is different for different V_{IN}, switching frequency and inductor values. The SW_VC_INT register bits can be used to set this initial peak current. Table 3 shows the configuration summary. When the recommended startup sequence is followed, the optimal initial peak inductor current can be calculated with Equation 2.

$$I_{PEAK\_INIT} = \frac{V_{IN}}{4 \bullet L \bullet f_{SW}} \quad (2)$$

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Configure the SW_VC_INT bits so the initial peak inductor current is closest to the calculated optimal value.

Table 3. Initial Peak Inductor Current Control

SW_VC_INT BITS	DESCRIPTION, IPEAK_INIT
000	0.251A
001	0.594A
010	0.936A
011	1.278A
100	1.62A
101	1.962A
110	2.304A
111	2.646A

LDR DRIVER INTERNAL POWER MITIGATION

In some conditions, the power dissipation of the LDR driver can be quite high. The LT8722 integrates power dissipation feedback loops to limit the maximum power dissipation of the LDR driver's top (M1) and bottom (M2) power devices. This maximum power can be configured through the PWR_LIM_BOT and PWR_LIM_TOP registers. Table 4 shows the power limit setup summary.

Table 4. LDR Driver Power Limit Control for M2 MOSFET

PWR_LIM_BITS	APPROX. M1/M2 POWER DISSIPATION LIMIT
0000	2W
0101	No Limit
1010	3W
1111	3.5W

SETTING THE OUTPUT VOLTAGE

The LT8722 has two separate amplifiers to control the MOSFET (M1–M4) drivers: a switched output (or PWM) amplifier and a high gain linear amplifier. Each amplifier has a pair of outputs that drive the gates of the internal MOSFETs, which in turn drive the load as shown in Figure 5. A voltage across the load is monitored via the SFB and LDR pins. Although both MOSFET drivers achieve the same result of providing constant voltage and high current, their operation is different. The two outputs can be calculated with Equation 3 and Equation 4.

$$V_{LDR} = (1/2 \bullet V_{IN}) + L_G \bullet (V_{DAC} - V_{1P25}) \quad (3)$$

$$V_{SFB} = V_{LDR} + 16 \bullet (V_{DAC} - V_{1P25}) \quad (4)$$

Where LG is the linear amplifier gain as shown in Equation 5.

$$L_G = \frac{8}{Duty\_Cycle\_Max} \quad (5)$$

Where Duty_Cycle_Max is listed in Table 6.

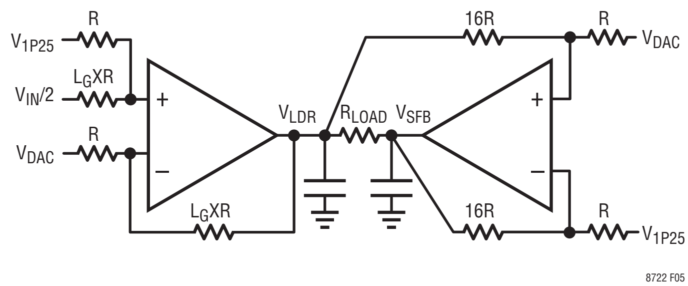

Figure 5. Switched (PWM) Amplifier and Linear Amplifier

Figure 6 shows how the output voltage changes as the V_{DAC} voltage setting is adjusted.

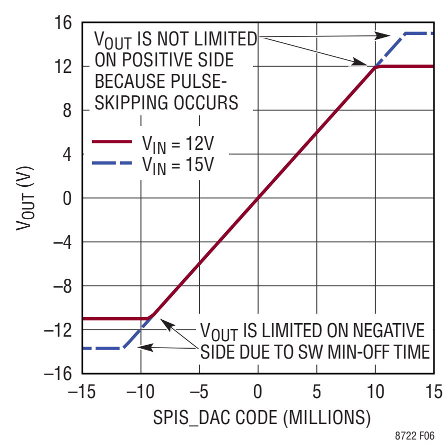

Figure 6. Output Voltage $V_{OUT} = V_{LDR} – V_{SFB}$ vs SPIS_DAC Code

V_{SFB} and V_{LDR} are individually driven as shown in Figure 7 and Figure 8 depending on the V_{DAC} setting and the SYS_DC register bits. The differential V_{OUT} voltage (V_{LDR}–V_{SFB})

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vs transfer function (Figure 6) is unaffected by SYS_DC. However, the SYS_DC register setting effects the LDR slope and the min/max duty cycle of the PWM driver as shown in Figure 7 and Figure 8.

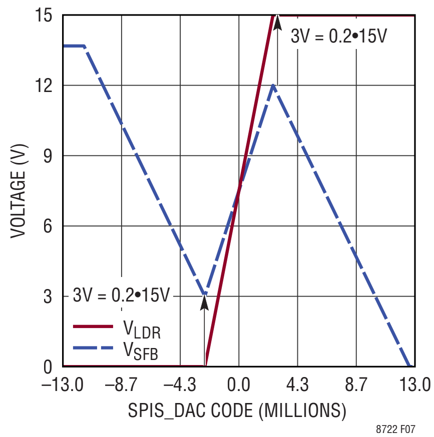

Figure 7. V_{LDR} and V_{SFB} vs SPIS_DAC Code when V_{IN} = 15V, SYS_DC[1:0] = 2b00, f_{SW} = 2MHz

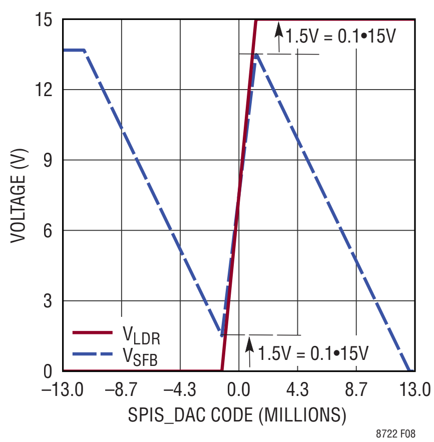

Figure 8. V_{LDR} and V_{SFB} vs SPIS_DAC Code when V_{IN} =15V, SYS_DC[1:0] = 2b10, f_{SW} = 2MHz

The integrated high resolution DAC is used to set LDR, SFB and the corresponding output voltage. In a regulation feedback loop, a software controlled PID loop measures a desired parameter, then adjusts the output voltage by configuring the SPIS_DAC register through SPI. SPIS_DAC is stored in 2's complement format. The 7MSB bits, SPIS_DAC[31:26] are sign-extended and are decided by the SPIS_DAC[25] bit. Table 5 shows how to set V_{DAC} through the SPIS_DAC register. Note that V_{DAC} is equal to V_{1P25} when SPIS_DAC is 0x00000000. The output voltage can be calculated by Equation 6 and Equation 7.

$$V_{OUT} = V_{LDR} - V_{SFB} = -16 \bullet (V_{DAC} - V_{1P25}) \quad (6)$$

$$V_{DAC} = V_{1P25} - SPIS\_DAC \bullet V_{2P5} \bullet 2^{-25} \quad (7)$$

The integrated 25-bit DAC is used to set the output differential voltage, V_{OUT}, as per Equation 8. V_{OUT} can be changed by setting the SPIS_DAC register through the SPI. SPIS_DAC is stored in 2's complement format. The 7MSB bits, SPIS_DAC[31:26] are sign-extended and are decided by the SPIS_DAC[25] bit. Table 5 shows how to set V_{DAC} through the SPIS_DAC register. Note that V_{OUT} is equal to zero when SPIS_DAC is 0x00000000. The output voltage V_{OUT} be calculated by Equation 8.

$$V_{OUT} = 16 \bullet SPIS\_DAC \bullet V_{2P5} \bullet 2^{-25} \quad (8)$$

Where 2^{-25} is approximately 29.802nV.

Table 5. V_{DAC} vs SPIS_DAC

SW_DAC_VTEC BITS	DESCRIPTION, V_{DAC}
0xFF000000	V_{1P25} + 16777216 • V_{2P5} • 2^{-25}V = 2.5V
0xFF000001	V_{1P25} + 16777215 • V_{2P5} • 2^{-25}V = 2.49999997V
•••	•••
0xFF999998	V_{1P25} + 6710888 • V_{2P5} • 2^{-25}V = 2.00000003V
0xFF999999	V_{1P25} + 6710887 • V_{2P5} • 2^{-25}V = 2.0V
0xFF99999A	V_{1P25} + 6710886 • V_{2P5} • 2^{-25}V = 1.99999997V
•••	•••
0xFFFFFFFF	V_{1P25} + 1 • V_{2P5} • 2^{-25}V = 1.25000003V
0x00000000	V_{1P25} + 0 • V_{2P5} • 2^{-25}V = 1.25V
0x00000001	V_{1P25} – 1 • V_{2P5} • 2^{-25}V = 1.24999997V
•••	•••
0x00666666	V_{1P25} – 6710886 • V_{2P5} • 2^{-25}V = 0.75000003V
0x00666667	V_{1P25} – 6710887 • V_{2P5} • 2^{-25}V = 0.75V
0x00666668	V_{1P25} – 6710888 • V_{2P5} • 2^{-25}V = 0.74999997V
•••	•••
0x00FFFFFE	V_{1P25} – 16777214 • V_{2P5} • 2^{-25}V = 0.00000006V
0x00FFFFFF	V_{1P25} – 16777215 • V_{2P5} • 2^{-25}V = 0.00000003V

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PWM DUTY CYCLE CONFIGURATION

The minimum and maximum output voltage can be achieved at operating points A and D as shown in Figure 7. At the operating point labeled A, the PWM driver is operating with a minimum on-time ($t_{ON,MIN}$) of 50ns (typ). If the PWM driver is commanded by the output voltage control DAC to output a voltage at the SFB pin that violates the minimum on-time, the PWM driver may begin pulse-skipping to achieve the desired output voltage. It's recommended to avoid these extreme operating points as the output voltage regulation may begin to degrade. Similarly, at the operating point labeled D, the PWM driver is operating with a minimum off-time ($t_{OFF,MIN}$) of 50ns (typ). If the PWM driver is commanded by the output voltage control DAC to output a voltage that violates the minimum off-time, the PWM driver may begin pulse-skipping to achieve the desired output voltage. It's recommended to avoid these extreme operating points as the output voltage regulation may begin to degrade.

For a given switching frequency, operating points labeled B and C need to be considered carefully to avoid $t_{ON,MIN}$ and $t_{OFF,MIN}$ violations. As an example, using a switching frequency of 3MHz, the typical $t_{ON,MIN}$ and $t_{OFF,MIN}$ are both 50ns. From this information, it can be calculated that the minimum and maximum operating duty cycle that can be tolerated by the PWM driver are 15% and 85%, respectively. Thus, the selected duty cycle range configuration, set by the SYS_DC register, should be within this range. According to Table 6, the SYS_DC register should be configured as [0,0].

Table 6. Duty Cycle Configuration

SYS_DC BITS	DUTY CYCLE RANGE	DUTY_CYCLE_MAX
00	20~80%	0.2
01	15~85%	0.15
10, 11	10~90%	0.1

For a given V_{IN} voltage and a switching frequency, the maximum achievable output voltage is decided by the minimum and maximum duty cycles. As an example, assuming V_{IN} = 8V and a switching frequency of 3MHz, the output voltage range is approximately –6.8V to +6.8V when excluding the small voltage drops across the monolithic power MOSFETs.

MAXIMUM TEC VOLTAGE LIMITS

The maximum positive and negative TEC voltages are set in the SPIS_OV_CLAMP and SPIS_UV_CLAMP registers respectively. These two registers set the maximum and minimum SPIS_DAC register values and, in turn, set the maximum positive and negative TEC voltages. Table 7 and Table 8 show how the SPIS_DAC register value is limited by SPIS_OV_CLAMP register and the SPIS_UV_CLAMP register, respectively.

Table 7. Max SPIS_DAC vs SPIS_OV_CLAMP

SPIS_OV_CLAMP BITS	MAX SPIS_DAC VALUE
4b0000	0x000FFFFF
4b0001	0x001FFFFF
•••	•••
4b1110	0x00EFFFFF
4b1111	0x00FFFFFF

Table 8. Min SPIS_DAC vs SPIS_UV_CLAMP

SPIS_OV_CLAMP BITS	MIN SPIS_DAC VALUE
4b0000	0xFF000000
4b0001	0xFF100000
•••	•••
4b1110	0xFFE00000
4b1111	0xFFF00000

OUTPUT CURRENT LIMITS

To protect the load, the LT8722 integrates two 9-bit DACs to limit the maximum output currents in both directions independently. Positive current refers to current flowing from LDR to SFB. The current limits can be set in the SPIS_DAC_ILIMP and SPIS_DAC_ILIMN registers. The current limits can be calculated with Equation 9 and Equation 10.

$$I_{LIMP} = 6.8A - (SPIS\_DAC\_ILIMP \bullet 13.28mA) \quad (9)$$

where SPIS_DAC_ILIMP is 0 to 462.

$$I_{LIMN} = SPIS\_DAC\_ILIMN \bullet -13.28mA \quad (10)$$

where SPIS_DAC_ILIMN is 48 to 511.

The two 9-bit DACs provide wide output current limit settings. When the output voltage is limited by I_{LIMP} or I_{LIMN}, and the PWM driver reaches the min-on or min-off

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time limitation, the PWM driver will pulse-skip cycles to maintain the desired output voltage. The purpose of this pulse-skipping is to protect the load from over current.

RESET

A reset can be triggered by system fault conditions like a V_{DDIO} UVLO fault or a thermal shutdown fault. The SPI_RST bit can be asserted to initiate a reset, via the SPI interface, if for example an external microcontroller needs to re-initiate the system. The reset brings all registers to their default values except for the SPIS_STATUS register.

STATUS MONITORING

LT8722 status is stored in the SPIS_STATUS register summarized in Table 9. There are six fault bits: OVER_CURRENT, TSD, VCC_UVLO, VDDIO_UVLO, CP_UVLO and V2P5_UVLO. To enable the PWM driver and/or the linear driver, all fault bits must be cleared by writing each register value to 0.

Table 9. SPIS_STATUS Register

BIT NAME	DESCRIPTION
SWEN	1 Indicates That the PWM is Switching
SRVO_ILIM	1 Indicates That the Output Current Limit is Active
SRVO_PLIM	1 Indicates That the Linear Regulator Power Dissipation Limiting Is Active
MIN_OT	1 Indicates That the PWM Switching Is Limited By Min-On Or Min-Off Time
POR_OCC	1 is a Latched Indicator That the Reset Has Happened Since Last Cleared
OVER_CURRENT	1 is a Latched Indicator That the Linear Driver Overcurrent Fault Has Happened Last Cleared
TSD	1 is a Latched Indicator That the Overtemperature Fault Has Happened Since Last Cleared
VCC_UVLO	1 is a Latched Indicator That the V_{CC} Regulator UVLO Fault Has Happened Since Last Cleared
VDDIO_UVLO	1 is a Latched Indicator That the V_{DDIO} Voltage UVLO Fault Has Happened Since Last Cleared
CP_UVLO	1 is a Latched Indicator That the Charge Pump UVLO Fault Has Happened Since Last Cleared
V2P5_UVLO	1 is a latched indicator That the 2.5V Reference UVLO Fault Has Happened Since Last Cleared

ANALOG MONITORING

Several analog signals can be monitored through the A_{OUT} pin. The signal selection is made in the SPIS_AMUX register and is summarized in Table 10. When AOUT_EN = 0, the A_{OUT} pin is tri-stated. The AMUX_TEST bits can be used to confirm the A_{OUT} signal integrity by changing the A_{OUT} pin voltage by a pre-defined amount for the selected signal. To ensure the most accurate A_{OUT} calculation from Table 10, be sure to use the most recently measured values for V_{1P25} and V_{1P65}.

Table 10. Analog Monitoring

AMUX[3:0]	FOR MONITORING
0000	9-bit DAC Voltage, V_{ILIMP} for Positive Output Current Limit
0001	9-bit DAC Voltage, V_{ILIMN} for Negative Output Current Limit
0010	25-bit DAC Voltage, V_{DAC}
0011	V_{OUT} Voltage Difference, V_{OUT}
0100	I_{OUT} Current Information
0101	Internal Voltage Reference, V_{2P5}
0110	Internal Voltage Reference, V_{1P25}
0111	Internal Voltage Reference, V_{1P65}. A_{OUT} is Equal to V_{1P65} when Output Current is 0 when this Channel is Selected
1000	Chip Temperature Monitor, V_{TEMP}
1001	V_{IN} Voltage
1010	V_{CC} Voltage
1011	V_{DDIO} Voltage
1100–1101, 1110–1111	V_{SFB} Voltage

The A_{OUT} pin output range is 0.2V to V_{DDIO}–0.2V. The analog MUX signal range can be beyond the A_{OUT} pin voltage range, so some voltage conversions are made. Output current is transformed to the voltage V_{IMON} which is ideally equal to V_{1P65} when the output current is 0. When temperature monitoring is selected, the A_{OUT} pin will output a voltage proportional to the die temperature with 1.498V (typ) at 25°C and a typical slope of 4.977mV/°C. Table 11 shows the A_{OUT} pin voltage for various analog mux signals. The AMUX_TEST bits can change the A_{OUT} pin output voltage for the same analog mux signal (see details in Table 12).

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Table 11. A_{OUT} Voltage vs AMUX[3:0] when AMUX_TEST = 0

AMUX[3:0]	VOLTAGE
0000	V_{ILIMP}
0001	V_{ILIMN}
0010	$V_{1P25} – 0.8 • V_{DAC}$
0011	$V_{1P25} – (V_{LDR} – V_{SFB})/16$
0100	$V_{1P65} – I_{OUT}/10$
0101	$0.6 • V_{2P5}$
0110	V_{1P25}
0111	V_{1P65}
1000	V_{TEMP}
1001	$0.9 • V_{2P5} – V_{IN}/8$
1010	$0.4 • V_{CC}$
1011	$0.4 • V_{DDIO}$
1100–1111	$(16/17) • V_{1P25} + V_{SFB}/17$

Table 12. A_{OUT} Voltage vs AMUX[3:0] when AMUX_TEST = 1

AMUX[3:0]	VOLTAGE
0000–0100, 1001, 1100–1111	See Table 12
0101	$(6/13) • V_{2P5}$
0110	$0.8 • V_{1P25} + 0.2 • V_{CC}$
0111	$(2/3) • V_{1P65}$
1000	$0.855 • V_{TEMP}$
1010	$(3/7) • V_{CC}$
1011	$(4/7) • V_{DDIO}$

DRIVING THE SWEN PIN

The SWEN pin is an input/output pin. When SWEN and SWEN_REQ are high, SWEN_INT is asserted, and the SW pin begins to switch. SWEN is pulled low internally by the LT8722 when the LT8722 detects a fault. This pin can also be pulled low by an external circuit to disable switching and put SW into a high impedance mode. The SWEN pin can be driven in an open-drain fashion as shown in Figure 9. The SWEN pin can be driven in a CMOS fashion as shown in Figure 10. Figure 11 shows the SWEN pin coupled to 3.3V through a 20k pull-up resistor. In this case SWEN will go high when the SPIS_STATUS[10:4] bits are cleared and FAULT goes low.

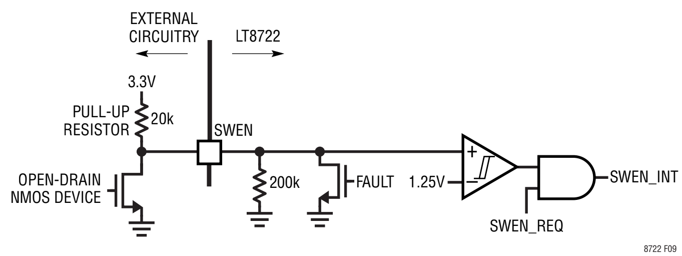


Figure 9. Open-Drain Drive of the SWEN Pin

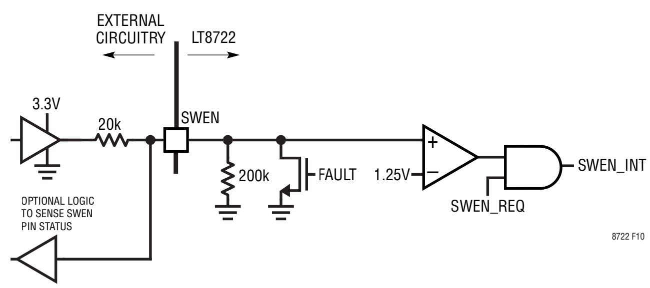


Figure 10. CMOS Drive of the SWEN Pin

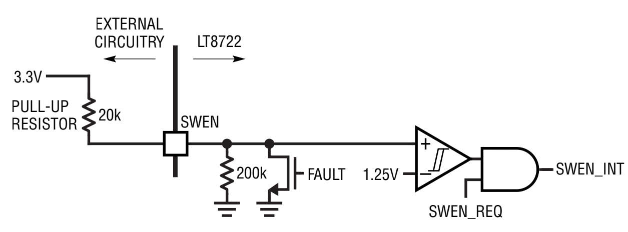


Figure 11. Simple Resistor Pull-Up on the SWEN Pin

SPI ARCHITECTURE

SERIAL PERIPHERAL INTERFACE

The LT8722 utilizes an SPI slave to communicate with an external microcontroller. Through SPI, the master can configure the LT8722 functions and set parameters. The master can also read back the status of the LT8722.

The LT8722 SPI is a full duplex protocol on 4-signal lines. A clock named SCK is sent from the master to synchronize MOSI and MISO data. A chip-select enable bar signal (active low) named $\overline{CS}$ is sent from the master to enable LT8722 SPI communication. A unidirectional data line named MOSI is sent from the master to the LT8722 and a unidirectional data line named MISO is driven from the LT8722 to the master. Bits are always sent or driven MSB first. SPI Mode 0 is supported in the LT8722. In Mode 0, the SCK is low when the clock is inactive, and bits are always sampled at the rising edge of SCK and driven at the falling edge of SCK.

SPI: Packet Format

A packet is a fundamental data element composed of individual bits encoding the command, address and/or data accompanied by a CRC/ACK. Different packet types contain different numbers of bits. There are 3 types of packets for the LT8722 SPI: Status Acquisition, Data Write, and Data Read.

Each packet accomplishes one complete transaction over the interface, whether a Status Acquisition, Data Write, or Data Read. Packets are always initiated by pulling $\overline{CS}$ down and always end by pulling $\overline{CS}$ up.

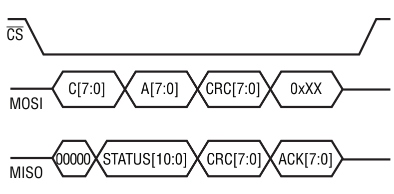


Figure 12. Status Acquisition Packet

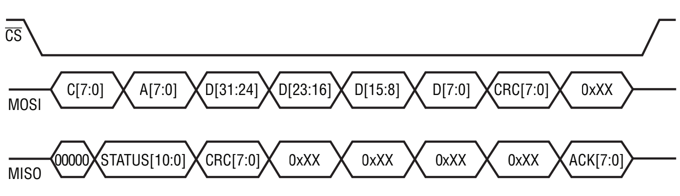


Figure 13. Data Write Packet

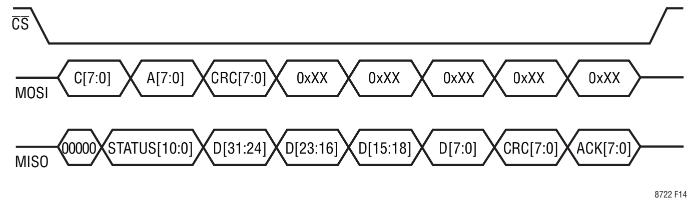


Figure 14. Data Read Packet

SPI: Command

C[7:0] is an 8-bit field indicating the action that the master wants to perform as shown in Table 13.

Table 13. Command Byte Description

NAME	C[7:0]	DESCRIPTION
SQ	0x00	Status Acquisition Command
DW	0x02	Data Write Command
DR	0x04	Data Read Command

SPI: ADDRESS

A[7:0] is an 8-bit field indicating the register address that the master wants to access. Table 14 is the register address summary and the address field duration is 8-SCK cycles. A[0] is always zero.

Table 14. Address Description, A[0] Is Always Zero

ADDRESS, A[7:1]	REGISTER NAME
0x00	SPIS_COMMAND
0x01	SPIS_STATUS
0x02	SPIS_DAC_ILIMN
0x03	SPIS_DAC_ILIMP
0x04	SPIS_DAC
0x05	SPIS_OV_CLAMP
0x06	SPIS_UV_CLAMP
0x07	SPIS_AMUX

SPI: DATA

D[31:0] is a 4-byte field containing the data to transfer. The data field duration is 32-SCK cycles.

SPI ARCHITECTURE

SPI: CRC

The LT8722 uses a cyclic redundancy check (CRC) to detect data communication errors in each SPI MOSI and MISO packet. The CRC in the SPI frame is an 8-bit field containing the computed CRC value spanning the command, address and data. The CRC is also sent MSB first.

The default polynomial equation used for calculating the CRC is CRC-8-CCITT: $X^8 + X^2 + X + 1$. The default initial seed value for calculating the CRC is 0xFF.

SPI: Status

LT8722 SPI packets always contain Status Flags (11 bits) which are identical to the bits in the SPIS_STATUS register.

SPI: Acknowledge

ACK[7:0] is an 8-bit field of 8-SCK cycles. Table 15 shows the acknowledge content.

Table 15. Acknowledge Content

ACK[7:0]	DESCRIPTION
0xA5	Acknowledge
0xC3	Non-Acknowledge
0x0F	Reject Due to Unsupported Register Address
0x00	Stuck at 0
0xFF	Stuck at 1
Others	Corruption

SPI REGISTER MAP

SUMMARY TABLE

REGISTER	DESCRIPTION	READ/WRITE	SIZE	ADDRESS	DEFAULT VALUE
MAIN					
SPIS_COMMAND	Device Control	R/W	22	0x0	0x08A214
SPIS_STATUS	Device Operation Summary	R/W	11	0x1	
DAC CONTROL					
SPIS_DAC_ILIMN	DAC Positive Current Limit Control Register	R/W	9	0x2	0x1FF
SPIS_DAC_ILIMP	DAC Negative Current Limit Control Register	R/W	9	0x3	0x000
SPIS_DAC	DAC Output Voltage Control Register	R/W	32	0x4	0xFF000000
OV/UV CLAMP					
SPIS_OV_CLAMP	DAC Output Positive Voltage Limit Control Register	R/W	4	0x5	0xF
SPIS_UV_CLAMP	DAC Output Negative Voltage Limit Control Register	R/W	4	0x6	0x0
AMUX					
SPIS_AMUX	Analog MUX Control Register	R/W	7	0x7	0x00

SPI REGISTER DESCRIPTIONS

SPIS_COMMAND Register

This register is used to enable and disable the device, set the switching frequency, control the PWM output duty cycle, set the VCC voltage, set initial peak inductor current, execute the software reset and set the linear driver's power loss regulation threshold.

BITS	SYMBOL	OPERATION
B[0]	ENABLE_REQ	V_{CC} LDO enable bit and linear power stage enable request bit. Default: 0x0 V_{CC} LDO is enabled when ENABLE_REQ = 1 OR the EN pin is high. Linear power stage is enabled when ENABLE_REQ = 1 and the SPIS_STATUS fault bits are cleared.
B[1]	SWEN_REQ	PWM switch enable request bit. Default: 0x0 1b1: Request PWM switching enable. PWM switching is enabled when SWEN_REQ = 1 and the SWEN pin is high and the V_{CC} LDO is enabled. 1b0: PWM switching is disabled.
B[4:2]	SW_FRQ_SET[2:0]	PWM switch frequency control bits. Default: 0x5 3b000: 0.5MHz 3b001: 1MHz 3b010: 1.5MHz 3b011: 2MHz 3b100: 2.5MHz 3b101, 3b110, 3b111: 3MHz
B[6:5]	SW_FRQ_ADJ[1:0]	PWM switch frequency adjustment bits. Default: 0x0 2b00: 0% 2b01: +15% 2b10: –15% 2b11: 0%
B[8:7]	SYS_DC[1:0]	PWM duty cycle control bits. Default: 0x0 2b00: 20%–80% duty cycle 2b01: 15%–85% duty cycle 2b10, 2b11: 10%–90% duty cycle

SPI REGISTER DESCRIPTIONS

BITS	SYMBOL	OPERATION
B[9]	VCC_VREG	V_{CC} LDO regulation control bit. Default: 0x1 1b1: V_{CC} LDO regulation voltage = 3.4V 1b0: V_{CC} LDO regulation voltage = 3.1V
B[10]	Unused	Must always be set to 0x0
B[13:11]	SW_VC_INT[2:0]	Typical peak inductor current after BST–SW refresh period control bits. Default: 0x2 3b000: 0.252A 3b001: 0.594A 3b010: 0.936A 3b011: 1.278A 3b100: 1.620A 3b101: 1.962A 3b110: 2.304A 3b111: 2.646A
B[14]	SPI_RST	Software reset request bit. Default: 0x0 (Active High) This register bit (write "1" to this register bit) is used to manually reset all registers (except SPIS_STATUS register) to default values
B[18:15]	PWR_LIM[3:0]	Linear power stage MOSFET power limit control bits. Default: 0x5 4b0000: 2W 4b0101: No Limit 4b1010: 3W 4b1111: 3.5W Other bit combinations not allowed.
B[31:19]	–	Ignored

SPIS_STATUS REGISTER

This register is used to store PWM out switching status, output current limit loop status, linear power loss regulation status, PWM output duty status, software reset event status, output over current failure status, overtemperature failure status, V_{CC} UVLO failure status, V_{DDIO} UVLO failure status, internal charge pump UVLO failure status and internal 2.5V voltage reference UVLO failure status.

BITS	SYMBOL	OPERATION
B[0]	SWEN	Real-time PWM switching status indicator bit. Default: 0x0 1b1: PWM switching enabled 1b0: PWM switching disabled
B[1]	SRVO_ILIM	Real-time current limit loop status indicator bit. Default: 0x0 1b1: Operating in current limit loop 1b0: Not operating in current limit loop
B[2]	SRVO_PLIM	Real-time linear power stage bottom MOSFET and top MOSFET power limit loop status indicator bit. Default: 0x0 1b1: Operating in power limit loop 1b0: Not operating in power limit loop
B[3]	MIN_OT	Real-time PWM duty cycle status indicator bit. Default: 0x0 1b1: Operating in min or max duty cycle, 1b0: Not operating in min or max duty cycle.
B[4]	POR_OCC	Latched soft reset event status indicator bit. Default: 0x0 1b1: Soft reset event by SPI_RST bit or hard reset by faults happened since last cleared 1b0: Soft reset event by SPI_RST bit has not happened since last cleared

SPI REGISTER DESCRIPTIONS

BITS	SYMBOL	OPERATION
B[5]	OVER_CURRENT	Latched Output over current event status indicator bit. Default: 0x0 1b1: Output overcurrent event happened since last cleared 1b0: Output overcurrent event has not happened since last cleared
B[6]	TSD	Latched overtemperature event status indicator bit. Default: 0x0 1b1: Overtemperature event happened since last cleared 1b0: Overtemperature event has not happened since last cleared
B[7]	VCC_UVLO	Latched V_{CC} LDO under voltage failure event status indicator bit. Default: 0x0 1b1: V_{CC} LDO under voltage failure event happened since last cleared 1b0: V_{CC} LDO under voltage failure event has not happened since last cleared
B[8]	VDDIO_UVLO	Latched V_{DDIO} voltage under voltage failure event status indicator bit. Default: 0x0 1b1: V_{DDIO} voltage under voltage failure event happened since last cleared 1b0: V_{DDIO} voltage under voltage failure event has not happened since last cleared
B[9]	CP_UVLO	Latched charge pump power good failure event status indicator bit. Default: 0x0 1b1: Charge pump power good status failure event happened since last cleared 1b0: Charge pump power good status failure event has not happened since last cleared
B[10]	V2P5_UVLO	Latched V_{2P5} good failure event status indicator bit. Default: 0x0 1b1: V_{2P5} good status failure event happened since last cleared 1b0: V_{2P5} good status failure event has not happened since last cleared
B[31:11]	–	Ignored

SPIS_DAC_ILIMN REGISTER

This register is used to set negative output current limit regulation level. LT8722 current is specified down to –4A.

BITS	SYMBOL	OPERATION
B[8:0]	SPIS_DAC_ILIMN[8:0]	9-bit DAC control register for negative output current limit. Default: 0x03FF Format: Unsigned Integer 9b000110000 = -637.44 mA [Minimum Code] 9b000110001 = -637.44 mA – 13.28 mA 9b….. 9b111111111 = -6.786 A [Maximum Code]
B[31:9]	–	Ignored

SPIS_DAC_ILIMP Register

This register is used to set positive output current limit regulation level. LT8722 current is specified up to 4A.

BITS	SYMBOL	OPERATION
B[8:0]	SPIS_DAC_ILIMP[8:0]	9-bit DAC control register for positive output current limit. Default: 0x0000 Format: Unsigned Integer 9b000000000 = 6.8 A [Minimum Code] 9b000000001 = 6.8 A – 13.28 mA 9b….. 9b111001110 = 637.44 mA [Maximum Code]
B[31:9]	–	Ignored

SPI REGISTER DESCRIPTIONS

SPIS_DAC Register

This register is used to set output voltage.

BITS	SYMBOL	OPERATION
B[31:0]	SPIS_DAC[31:0]	25-bit DAC control register for TEC voltage difference. Default: 0xFF000000 Format: 2's Complement. SPIS_DAC[31:25] are sign-extended bits determined by SPIS_DAC[24] and SPIS_DAC[24] is sign bit. Note: $2^{-25} = 29.8023\text{x}10^{-9}$ 0xFF000000 = 1.25V + 16777216 • 2.5 • 2^{-25}V = 2.5V 0xFF000001 = 1.25V + 16777215 • 2.5 • 2^{-25}V = 2.49999997V 0x…… 0xFF999998 = 1.25V + 6710888 • 2.5 • 2^{-25}V = 2.00000003V 0xFF999999 = 1.25V + 6710887 • 2.5 • 2^{-25}V = 2.0V 0xFF99999A = 1.25V + 6710886 • 2.5 • 2^{-25}V = 1.99999997 …… 0xFFFFFFFF = 1.25V + 1 • 2.5 • 2^{-25}V = 1.25000003V 0x00000000 = 1.25V + 0 • 2.5 • 2^{-25}V = 1.25V 0x00000001 = 1.25V – 1 • 2.5 • 2^{-25}V = 1.24999997V …… 0x00666666 = 1.25V – 6710886 • 2.5 • 2^{-25}V = 0.75000003V 0x00666667 = 1.25V – 6710887 • 2.5 • 2^{-25}V = 0.75V 0x00666668 = 1.25V – 6710888 • 2.5 • 2^{-25}V = 0.74999997V …… 0x00FFFFFE = 1.25V – 16777214 • 2.5 • 2^{-25}V = 0.00000006V 0x00FFFFFF = 1.25V – 16777215 • 2.5 • 2^{-25}V = 0.00000003V

SPIS_OV_CLAMP REGISTER

This register is used to set maximum positive output voltage (V_{LDR}–V_{SFB}).

BITS	SYMBOL	OPERATION
B[3:0]	SPIS_OV_CLAMP[3:0]	Positive Output voltage limit register. Default: 0xF 4b0000 = Max SPIS_DAC code value is 0x000FFFFF 4b0001 = Max SPIS_DAC code value is 0x001FFFFF 4b…… 4b1110 = Max SPIS_DAC code value is 0x00EFFFFF 4b1111 = Max SPIS_DAC code value is 0x00FFFFFF
[31:5]	–	Reserved

SPIS_UV_CLAMP Register

This register is used to set maximum negative output voltage (V_{LDR}–V_{SFB}).

BITS	SYMBOL	OPERATION
B[3:0]	SPIS_UV_CLAMP[3:0]	Negative Output voltage limit register Default: 0x0 4b0000 = Min SPIS_DAC code value is 0xFF000000 4b0001 = Min SPIS_DAC code value is 0xFF100000 4b…… 4b1110 = Min SPIS_DAC code value is 0xFFE00000 4b1111 = Min SPIS_DAC code value is 0xFFF00000
B[31:4]	–	Ignored

SPI REGISTER DESCRIPTIONS

SPIS_AMUX Register

This register is used to enable and disable analog monitor for internal signal monitoring.

BITS	SYMBOL	VALUE	SIGNAL	DESCRIPTION
B[3:0]	AMUX[3:0]	4b0000	V_{ILIMP}	The 9-bit internal DAC Voltage that controls the positive Output current limit
		4b0001	V_{ILIMN}	The 9-bit internal DAC Voltage that controls the negative Output current limit
		4b0010	$V_{1P25} – 0.8 • V_{DAC}$	Translation of the internal 25-bit DAC voltage that controls V_{OUT}
		4b0011	$V_{1P25} – V_{OUT}/16$	Translation of the V_{OUT} Voltage. V_{1P25} can be measured on channel 4b0110
		4b0100	$V_{1P65} – I_{OUT}/10$	Translation of the I_{OUT} Current. V_{1P65} can be measured on channel 4b0111
		4b0101	$0.6 • V_{2P5}$	Translation of the V_{2P5} Voltage when AMUX_TEST = 2b00 or 2b10
			(6/13) • V2P5	Translation of the V_{2P5} Voltage when AMUX_TEST = 2b01 or 2b11
		4b0110	V1P25	Translation of the V_{1P25} Voltage when AMUX_TEST = 2b00 or 2b10
			$0.8 • V_{1P25} + 0.2 • V_{CC}$	Translation of the V_{1P25} Voltage when AMUX_TEST = 2b01 or 2b11
		4b0111	V_{1P65}	Translation of the V_{1P65} Voltage when AMUX_TEST = 2b00 or 2b10
			$(2/3) • V_{1P65}$	Translation of the V_{1P65} Voltage when AMUX_TEST = 2b01 or 2b11
		4b1000	V_{TEMP}	Translation of the V_{TEMP} Voltage when AMUX_TEST = 2b00 or 2b10
			$0.855 • V_{TEMP}$	Translation of the V_{TEMP} Voltage when AMUX_TEST = 2b01 or 2b11
		4b1001	$0.9 • V_{2P5} – V_{IN}/8$	Translation of the V_{IN} Input Voltage. V_{2P5} Can Be Measured by Using Channel 4b0110
		4b1010	$0.4 • V_{CC}$	Translation of the V_{CC} LDO Voltage when AMUX_TEST = 2b00 or 2b10
			$(3/7) • V_{CC}$	Translation of the V_{CC} LDO Voltage when AMUX_TEST = 2b01 or 2b11
		4b1011	$0.4 • V_{DDIO}$	Translation of the V_{DDIO} input Voltage when AMUX_TEST = 2b00 or 2b10
			$(4/7) • V_{DDIO}$	Translation of the V_{DDIO} input Voltage when AMUX_TEST = 2b01 or 2b11
		4b1100	$(16/17) • V_{1P25} + V_{SFB}/17$	Translation of the V_{SFB} voltage. V_{1P25} Can Be Measured by Using Channel 4b0110
		4b1101		
		4b1110		
		4b1111		
B[5:4]	AMUX_TEST[1:0]	2b00	Affects Gain of AMUX[3:0] Channels 4b0101, 0110, 0111, 1000, 1010, 1011	
		2b10		
		2b01	Affects Gain of AMUX[3:0] Channels 4b0101, 0110, 0111, 1000, 1010, 1011	
		2b11		
B[6]	AOUT_EN	1b0	Analog Output Buffer Disabled	
		1b1	Analog Output Buffer Enabled	
B[31:7]	–	–	Ignored	

APPLICATIONS INFORMATION

INDUCTOR SELECTION

The inductor selection determines the inductor current ripple and loop dynamic responses. Larger inductance results in smaller current ripple and slower transient response as smaller inductance results in the opposite performance. To optimize the performance, trade-offs must be made between transient response speed, efficiency and component size. Normally the inductor current ripple is set to a value between 30% and 40% of the maximum load current (Equation 11).

$$L = \frac{V_{SFB} \bullet (V_{IN} - V_{SFB})}{(V_{IN} \bullet f_{SW} \bullet \Delta I_L)} \quad (11)$$

where ΔI_L is the desired inductor current ripple in Amps.

The equivalent DC resistance (DCR) inherent in the metal conductor of the inductor is also a critical factor for inductor selection. The DCR can account for much of the power loss in the inductor according to P_{LOSS} = DCR • I_{SFB2}. Using an inductor with high DCR degrades the overall efficiency significantly. In addition, there is a conducted voltage drop through the inductor because of the DCR. When the PWM amplifier is sinking current in cooling mode, this DCR voltage drop sets the minimum voltage of the amplifier a little higher by at least tens of millivolts. Similarly, the maximum PWM amplifier output voltage is a little lower by at least tens of millivolts. This voltage drop is proportional to the value of the DCR, and reduces the output voltage range across the TEC.

When selecting an inductor, ensure the saturation current rating is higher than the maximum current peak to prevent saturation. In general, ceramic multilayer inductors are suitable for low current applications due to small size and low DCR. When the noise level is critical, use a shielded ferrite inductor to reduce the electromagnetic interference (EMI).

SFB CAPACITOR SELECTION

The SFB capacitor determines the output voltage ripple, transient response, as well as the loop dynamic response of the PWM driver output. Use Equation 12 to select the capacitor.

$$C_{SFB} = \frac{\Delta I_L}{(8 \bullet f_{SW} \bullet \Delta f_{SFB})} \quad (12)$$

where ΔV_{SFB} is the desired maximum SFB pin voltage ripple.

Note that the voltage caused by the product of inductor current ripple, and the capacitor equivalent series resistance (ESR) also adds to the total output voltage ripple. Selecting a capacitor with low ESR can increase overall regulation and efficiency performance.

Place the SFB capacitor as close to the LT8722 as possible.

LDR CAPACITOR SELECTION

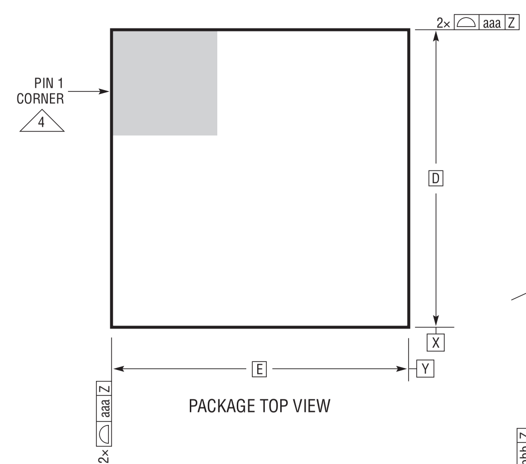
To further improve systematic noise at the output of the LT8722, additional ceramic capacitors can be added at the LDR pin. Each additional capacitor should range from 10nF – 47nF, depending on application, and have very low ESR and ESL characteristics. Capacitor positions are as follows 1) between LDR – GND close to the LT8722, 2) between LDR – SFB close to the load and 3) between LDR – GND close to the load. A lower cost, lower performance alternative would be to place a 150nF capacitor between LDR – SFB close to the primary SFB capacitor.

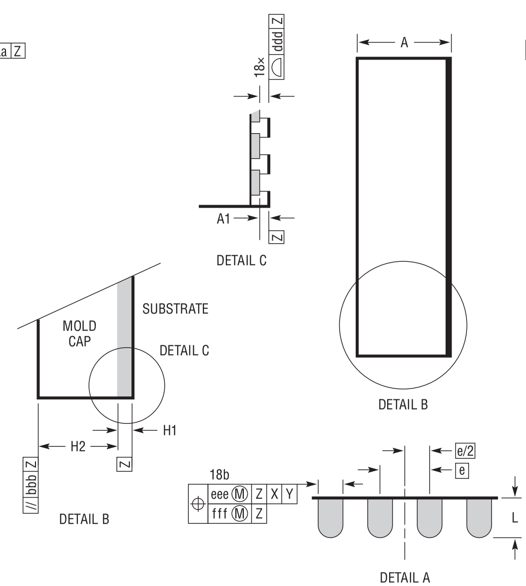
HIGH TEMPERATURE CONSIDERATIONS

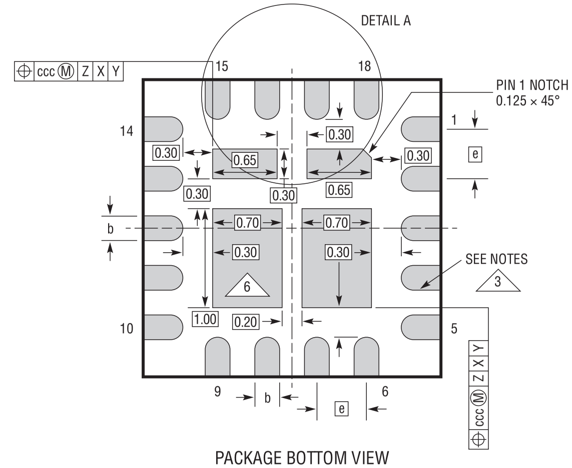
The LT8722 has two over temperature monitors. If the junction temperature exceeds ~170°C, mainly due to high V_{CC} regulator load current, the LT8722 will enter one thermal shutdown mode, and the V_{CC} regulator, linear driver and PWM driver are all disabled. Otherwise, an overtemperature event causes the SPI register values to reset to their default values and both drivers are disabled. Either overtemperature event is latched in the thermal shutdown (TSD) register bit. The TSD threshold has 15°C hysteresis so that the LT8722 does not recover from thermal shutdown until the on-chip temperature is below 155°C. Upon recovery, the LT8722 will enter a new start-up sequence.

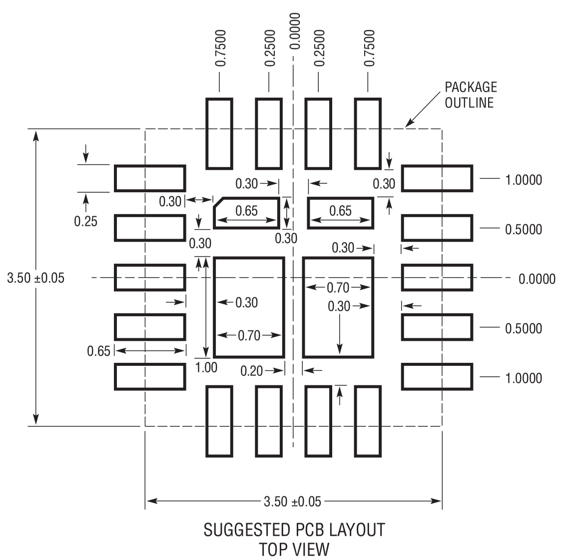
PACKAGE DESCRIPTION

LQFN Package
18-Lead (3mm × 3mm × 0.95mm)
(Reference LTC DWG # 05-08-1688 Rev A)



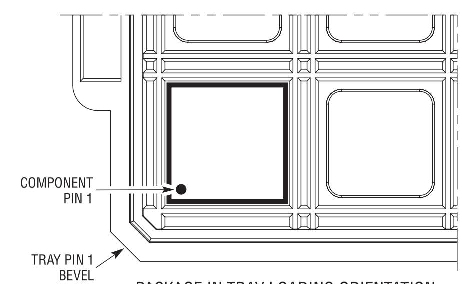






DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		3.00		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.08	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII



PACKAGE IN TRAY LOADING ORIENTATION

LQFN 18 0319 REV A

Rev. A

APPLICATIONS INFORMATION

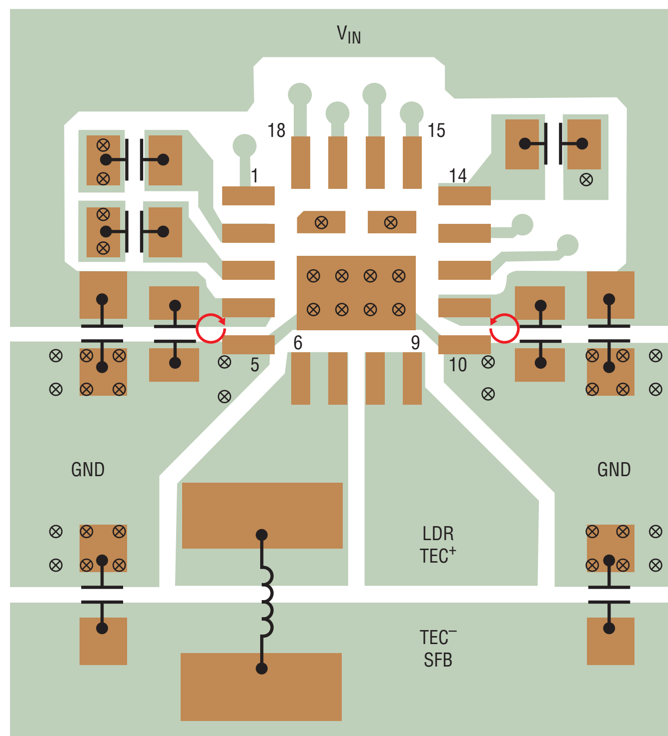
To ensure that the LT8722 operates below the maximum junction temperature, even at high load, careful attention must be paid to provide a lower θ_{JA} value for the device. Typical techniques for enhancing heat dissipation include using larger copper layers and more vias on the printed circuit board (PCB) and possibly adding a heat sink when needed.

The LT8722 LQFN package has a large exposed pad (EPAD) at the bottom that must be soldered to the analog ground plane on the board. Most of the device's heat dissipates through the EPAD. Therefore, the copper layer connected to the EPAD as well as the vias on it must be optimized to conduct the heat effectively. It is recommended to use a large via array and distribute them evenly on the EPAD. Generally, it is more effective to increase the number of vias than to increase the diameter of the via within a limited area.

LOW EMI PCB LAYOUT AND INPUT CAPACITOR SELECTION

The LT8722 is specifically designed to minimize EMI emissions and maximize efficiency when switching at high frequencies. For optimal performance the LT8722 requires the use of multiple V_{IN} bypass capacitors. Two small ceramic 0.1µF capacitors should be placed as close as possible to the LT8722: One of these capacitors should be tied to V_{IN}/GND (pins 4 and 5 respectively); a second capacitor should be tied to V_{IN}/GND (pins 11 and 10 respectively). Two ceramic 4.7µF capacitors should also be used as bypass capacitors—one of these capacitors should be placed close to pins 4 and 5 and one of these capacitors should be placed close to pins 11 and 10. See Figure 15 for a recommended PCB layout. For more detail and PCB design files refer to the demo board guide for the LT8722. Note that large, switched currents flow in the LT8722 V_{IN} and GND pins and the input bypass capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the V_{IN} and GND pins on either side of the LT8722.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8722 and to force this very high frequency switching current into a tight local loop, minimizing EMI. Capacitors with small case size such as 0402 and 0603 are optimal due to their low parasitic inductance. It is best to use ceramic capacitors of type X7R or X5R. Y5V types have poor performance over temperature and applied voltage and should not be used. The input capacitors should be placed on the same side of the circuit board, and their connections should be made on that layer. The SW and BOOST nodes should be as small as possible. To keep thermal resistance low, extend the ground plane from GND as much as possible, and add thermal vias to additional ground planes within the circuit board and on the bottom side.



AREA OF THE HOT LOOPS (SHOWN IN RED) SHOULD BE MINIMIZED BY PLACING THE CAPACITORS AS CLOSE TO V_{IN}/GND PINS AS POSSIBLE.

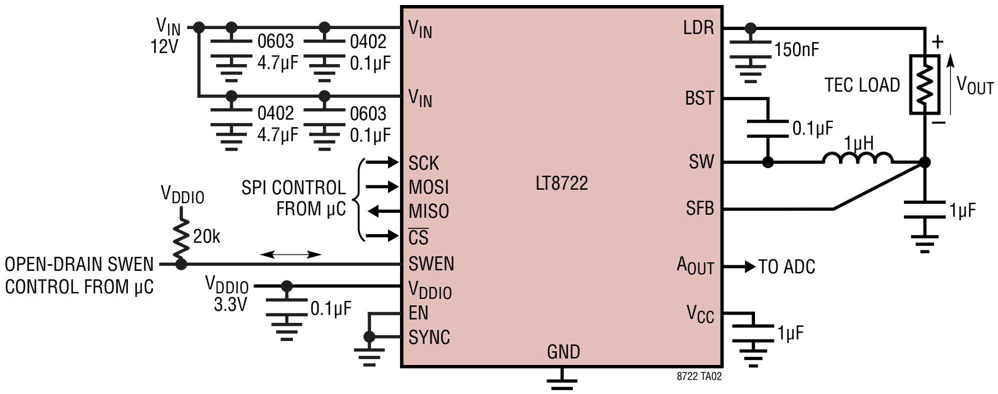
Figure 15. Recommended PCB Layout

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/22	Updated MOSI to SCK timing specifications	7
		Updated SWEN pin threshold from 1.25V to 1.2V (typ)	13

TYPICAL APPLICATION

12V Input Voltage, ±4A, –11V to 12V Output, 1.5MHz TEC Driver



f_{SW} = 1.5MHz
L: XGL4020-102MEC

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADN8830	Thermoelectric Cooler Controller	3.0V – 5.5V Input, External MOSFETs for High Current
ADN8831	Thermoelectric Cooler Controller	3.0V – 5.5V Input, External MOSFETs for High Current
ADN8833	Ultracompact, 1A Thermoelectric Cooler (TEC) Driver for Digital Control Systems	2.7V – 5.5V Input, Integrated MOSFETs, 2.5mm × 2.5mm WLCSP or 24-Lead 4mm × 4mm LFCSP
ADN8834	Ultracompact, 1.5A Thermoelectric Cooler (TEC) Controller	2.7V – 5.5V Input, Integrated MOSFETs, 2.5mm × 2.5mm WLCSP or 24-Lead 4mm × 4mm LFCSP
ADN8835	Ultracompact, 3A Thermoelectric Cooler (TEC) Controller	2.7V – 5.5V Input, Integrated MOSFETs, 36-Lead 6mm × 6mm LFCSP
LTM4663	Ultrathin 1.5A µModule Thermoelectric Cooler (TEC) Regulator	2.7V – 5.5V Input, 3.5mm × 4mm × 1.3mm LGA Package, Very Few External Components Required
LTC1923	High Efficiency Thermoelectric Cooler Controller	2.7V – 5.5V Input, External MOSFETs for High Current, 5mm × 5mm QFN or 28-Lead SSOP

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