*Click **here** to ask an associate for production status of specific part numbers.*

MAX20011E/MAX20011F/ MAX20011G

Automotive Single 8A/12A/16A Step-Down Converters

General Description

The MAX20011E/MAX20011F/MAX20011G are high-efficiency, synchronous step-down converters that operate with a 3.0V to 5.5V input voltage range and supply a 0.5V to 1.275V output voltage range. The wide input/output voltage range and ability to provide up to 16A peak output current make these devices ideal for on-board point-of-load and post-regulation applications. The MAX20011E/MAX20011F/MAX20011G achieve ±1.5% output error over load, line, and temperature ranges.

The MAX20011E/MAX20011F/MAX20011G feature a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response. The 2.2MHz frequency operation allows for the use of all ceramic capacitors and minimizes external components. The spread-spectrum frequency modulation option minimizes radiated electromagnetic emissions. Integrated low $R_{DS(on)}$ switches improve efficiency at heavy loads and make layout simpler than discrete solutions.

The MAX20011E/MAX20011F/MAX20011G are offered with factory-preset output voltage. The I^2C interface supports dynamic voltage adjustment with programmable slew rates. Other features include programmable soft-start, overcurrent, and overtemperature protections.

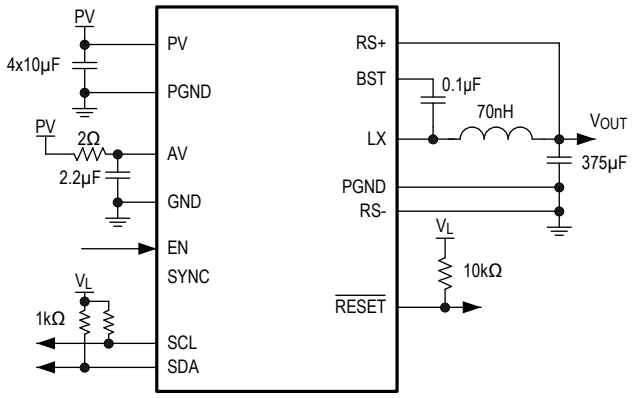
Applications

- Automotive ADAS Systems
- SoC Core Power

Benefits and Features

- High Efficiency DC-DC Converter
- Up to 16A Peak Output Current
  - MAX20011E: I_{MAX} = 8A
  - MAX20011F: I_{MAX} = 12A
  - MAX20011G: I_{MAX} = 16A
- Differential Remote Voltage Sensing
- 3.0V to 5.5V Operating Supply Voltage
- I^2C-Controlled Output Voltage:
  - 0.5V to 1.275V in 6.25mV Steps
- Excellent Load-Transient Performance
- Programmable Compensation
- 2.2MHz or 1.1MHz Operation
- ±1.5% Output Voltage Accuracy (Full Range)
- ±1% Output Voltage Accuracy (Fixed 1V)
- $\overline{\text{RESET}}$ Output
- Current-Mode, Forced PWM Operation
- ASIL D Compliant:
  - Redundant Reference
  - BIST Diagnostics
  - PEC on I^2C
  - Programmable OV/UV with ±1% Accuracy
- Overtemperature and Short-Circuit Protection
- 3.5mm x 4mm, 17-Pin Side-Wettable FC2QFN
- -40°C to +125°C Grade 1 Automotive Temperature Range

Simplified Block Diagram



Ordering Information appears at end of data sheet.

19-101225; Rev 0; 8/21

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Absolute Maximum Ratings

PV, AV, EN, $\overline{\text{RESET}}$ to GND ..... -0.3V to +6V
SYNC, RS+, RS- to GND ..... -0.3V to AV + 0.3V
SDA, SCL to GND ..... -0.3V to +6V
GND to PGND ..... -0.3V to +0.3V
BST to LX ..... -0.3V to +6V
LX to PGND ..... -0.3V to PV + 0.3V
Output Short Circuit Duration ..... Continuous

Continuous Power Dissipation 17-FC2QFN (T_A = +70°C)
4-Layer Board (derate 28.3mW/°C > 70°C) 2266mW
8-Layer Board (derate 43.4mW/°C > 70°C) 3478mW
Operating Junction Temperature (*Note 4*) .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to +125	°C

Note: These limits are not guaranteed.

Package Information

17 FC2QFN

PACKAGE CODE	F173A4FY+2
Outline Number	21-100538
Land Pattern Number	90-100190
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35.3°C/W
Junction to Case (θ_{JC})	7.9°C/W
Thermal Resistance, EV Kit (Eight-Layer Board):	
Junction to Ambient (θ_{JA})	23°C/W
Junction to Case (θ_{JC})	6.1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the EV-Kit, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{PV} = V_{AV} = 5V, T_J = -40°C to +150°C, unless otherwise noted, typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 1*, *Note 2*, and *Note 4*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
PV Supply Voltage	V_{PV}		3.0		5.5	V
AV Supply Voltage	V_{AV}	Fully Operational	3.0		5.5	V

Electrical Characteristics (continued)

(V_{PV} = V_{AV} = 5V, T_J = -40°C to +150°C, unless otherwise noted, typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 1*, *Note 2*, and *Note 4*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO		Rising		2.7	2.9	V
		Falling	2.45	2.6		
Supply Current	I_{IN}	EN = high, I_{OUT} = 0mA, no switching		2.5		mA
Shutdown Supply Current	I_{IN}	EN = low, T_A ≤ +125°C		3	30	µA
PWM FREQUENCY						
PWM Switching Frequency	F_{SW}	Internally generated, CONFIG.FSW = 0	2.0	2.2	2.4	MHz
		Internally generated, CONFIG.FSW = 1	1.0	1.1	1.2	
Spread Spectrum		CONFIG.SS = 1		+3		%
OUTPUT VOLTAGE						
Voltage Accuracy	V_{OUT}	I_{LOAD} = 0A to I_{MAX}, V_{PV} =3.3V, V_{OUT} = 1.0V	-1		+1	%
		I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, 0.80V to 1.275V	-1.5		+1.5	
		I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, 0.50V to 0.79V	-15		15	mV
OV Threshold Range			102.5		110	%
OV Threshold Accuracy		Percentage of nominal output, V_{OUT} = V_{SET} (0.8V - 1.275V)	-1		+1	%
		V_{OUT} = V_{SET} (0.5V - 0.79V)	-10		10	mV
UV Threshold Range			97.5		90	%
UV Threshold Accuracy		Percentage of nominal output, V_{OUT} = V_{SET} (0.8V - 1.275V)	-1		+1	%
		V_{OUT} = V_{SET} (0.5V - 0.79V)	-10		+10	mV
UV/OV Propagation Delay		V_{OUT} = V_{SET}		15		µs
Active Timeout Period		Option 1 (32768 clocks)		14.9		ms
		Option 2 (16384 clocks)		7.4		
		Option 3 (8192 clocks) (default)		3.7		
		Option 4 (1024 clocks)		0.5		
POWER FET						
HS nMOS Current-Limit Threshold		MAX20011E (8A) (*Note 3*)	11.8	15	18.2	A
		MAX20011G (16A) (*Note 3*)	20	24	28	
LX Leakage Current		V_{PV} = V_{AV} = 5V, LX = PGND or PV, T_A = +25°C		1		µA
LX Discharge Resistance		V_{EN} = 0V, I_{LOAD} = 10mA		11		Ω
THERMAL OVERLOAD						
Thermal Shutdown Temperature		T_J rising		165		°C
Hysteresis				15		°C

Electrical Characteristics (continued)

(V_{PV} = V_{AV} = 5V, T_J = -40°C to +150°C, unless otherwise noted, typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 1*, *Note 2*, and *Note 4*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUT ($\overline{RESET}$, SYNC, SDA)						
$\overline{RESET}$ Output Low Level		3.0V ≤ V_{PV} ≤ 5.5V, 3.0V ≤ V_{AV} ≤ 5.5V, I_{SINK} = 2mA			0.4	V
$\overline{RESET}$ High Leakage current				1		µA
SYNC Output High Level	V_{OH}	I_{SOURCE} = 3mA	4.2			V
SYNC Output Low Level	V_{OL}	I_{SINK} = 3mA			0.4	V
SDA Ouput Low Level	V_{OL_SDA}	I_{SINK} = 4mA			0.4	V
I^2C INTERFACE						
Clock Frequency					1.0	MHz
Setup Time (Repeated) START	$t_{SU:STA}$		260			ns
HOLD Time (Repeated) START	$t_{HD:STA}$		260			ns
SCL Low Time	t_{LOW}		500			ns
SCL High Time	t_{HIGH}		260			ns
DATA Setup Time	$t_{SU:DAT}$		50			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU:STO}$		260			ns
Spike Suppression				20		ns
DIGITAL INPUT (SYNC)						
Input High level	V_{IH}		1.8			V
Input Low level	V_{IL}				0.4	V
SYNC Input Pull-down				100		kΩ
SYNC Input Frequency Range		f_{OSC} = 2.2MHz	1.8		2.6	MHz
		f_{OSC} = 1.1MHz	0.9		1.3	
DIGITAL INPUT (EN, SDA, SCL)						
Input High Level			1.3			V
Input Low Level					0.5	V
Input Hysteresis				50		mV
Input Leakage Current				1		µA

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design and characterization.

Note 2: The device is designed to operate under in cabin automotive temperature profiles similar to *Typical Operating Characteristics* 1.

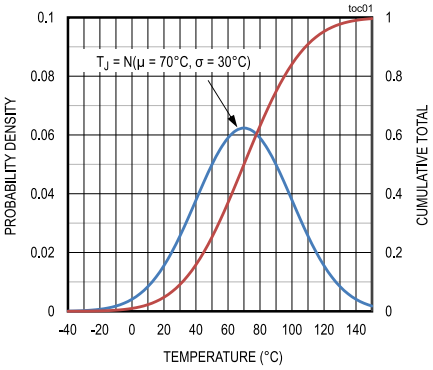
Note 3: Based on ATE measurements using scaled currents.

Note 4: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

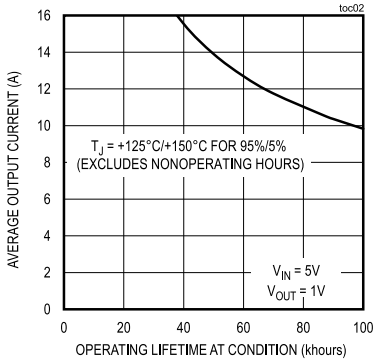
Typical Operating Characteristics

(V_{PV} = V_{AV} = 5V; T_A=25°C unless otherwise noted)

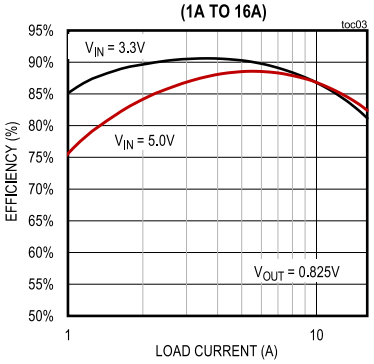
OPERATING TEMPERATURE PROFILE



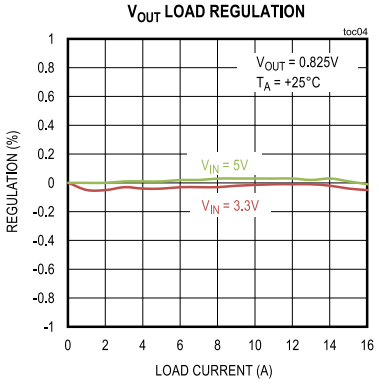
AVERAGE OUTPUT CURRENT vs. OPERATING LIFETIME



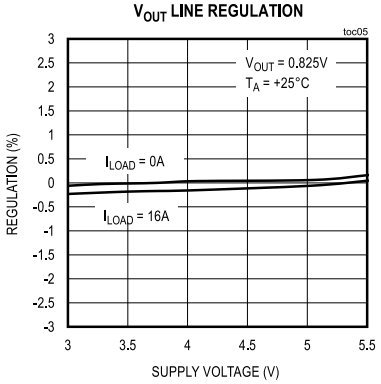
EFFICIENCY vs. LOAD CURRENT (1A TO 16A)



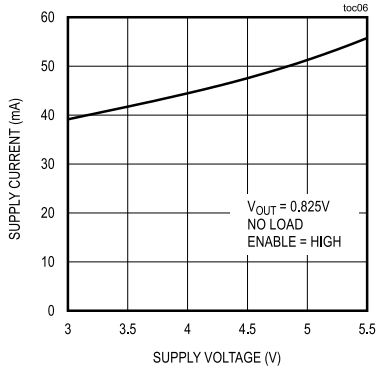
V_{OUT} LOAD REGULATION



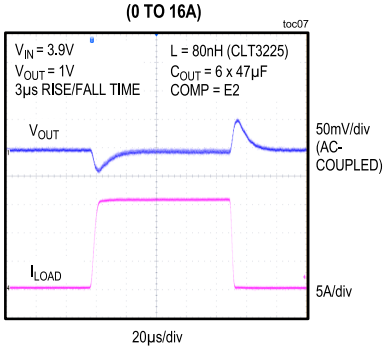
V_{OUT} LINE REGULATION



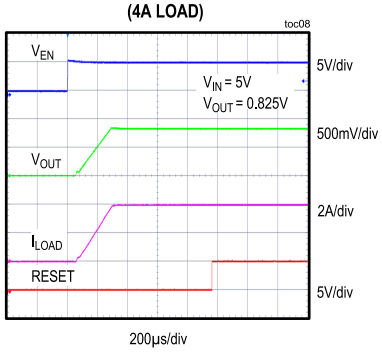
SUPPLY CURRENT vs. SUPPLY VOLTAGE



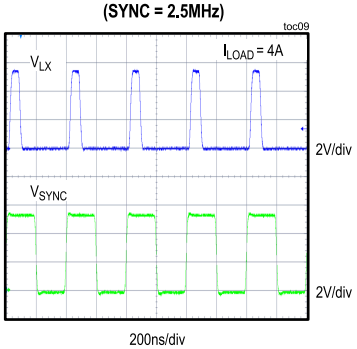
LOAD-TRANSIENT RESPONSE (0 TO 16A)



STARTUP BEHAVIOR (4A LOAD)

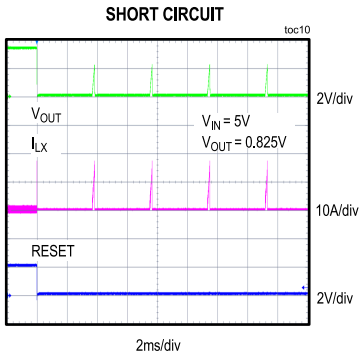


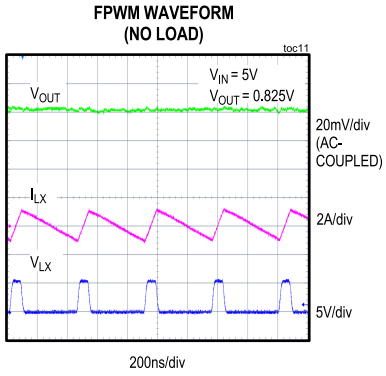
EXTERNAL SYNCHRONIZATION (SYNC = 2.5MHz)



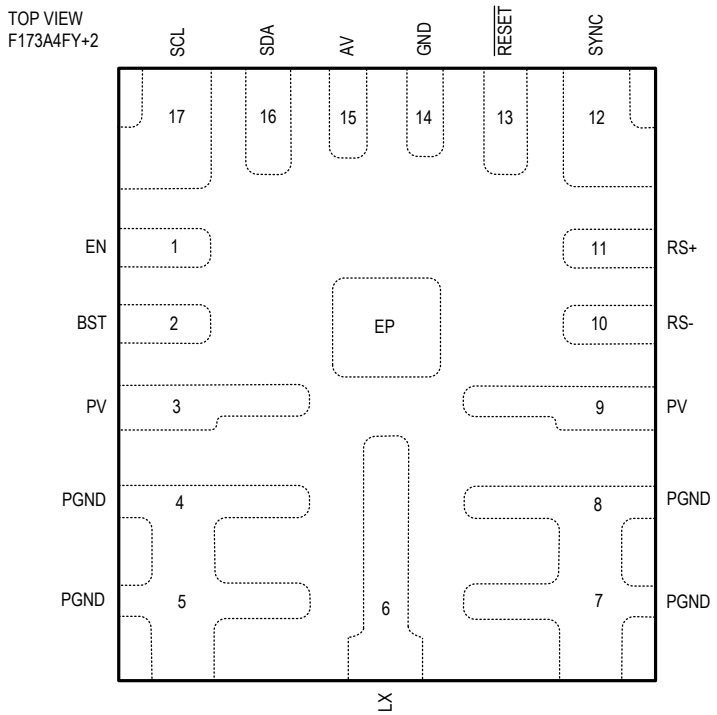
Typical Operating Characteristics (continued)

(V_{PV} = V_{AV} = 5V; T_A=25°C unless otherwise noted)





Pin Configuration

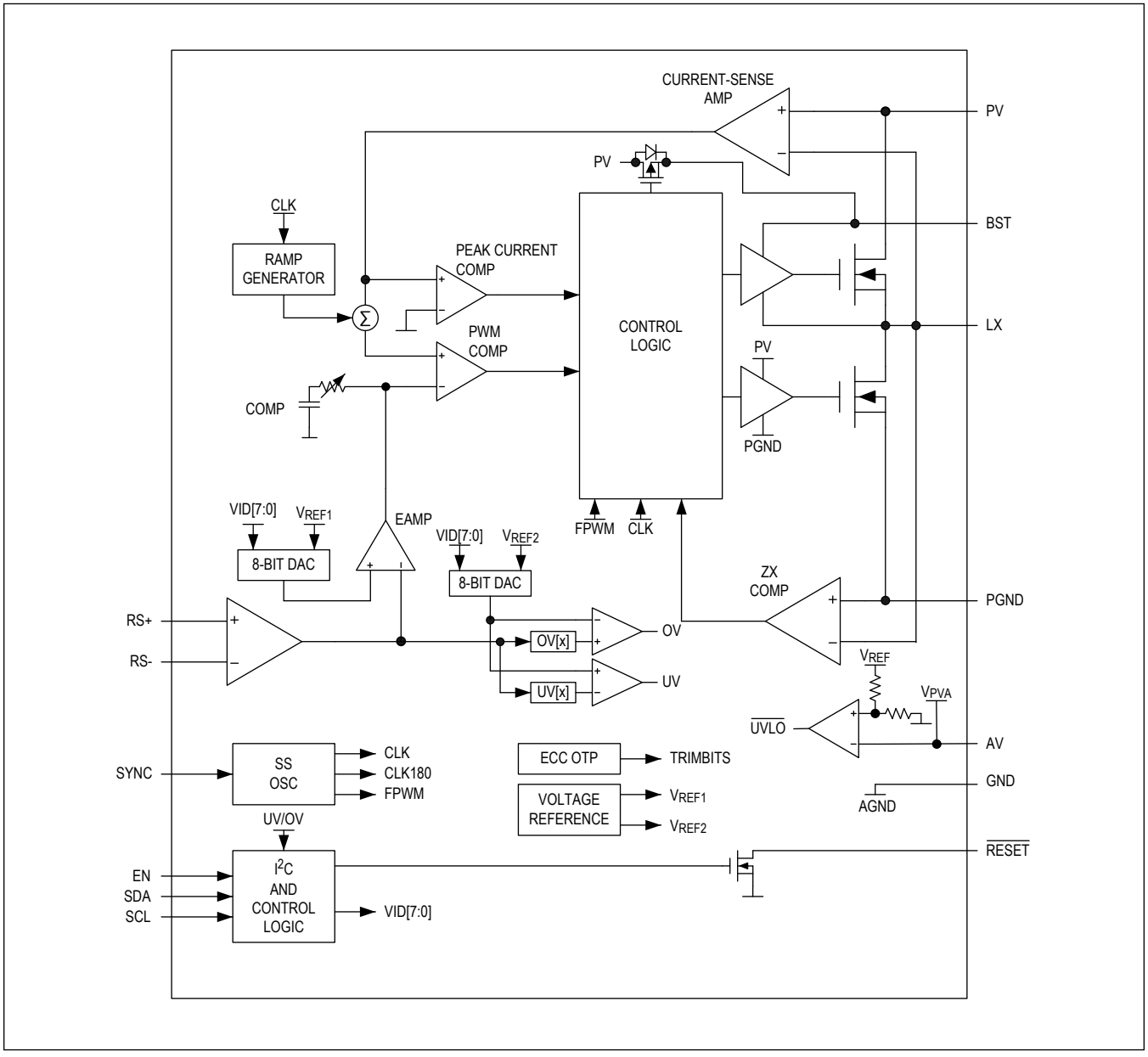


Pin Description

PIN	NAME	FUNCTION
1	EN	Active-High Enable Input. Drive EN HIGH for normal operation. On the rising edge the device enters soft-start, and on the falling edge the device enters soft-shutdown.
2	BST	Boost Supply
3, 9	PV	Power Input Supply. Connect two 10µF or larger ceramic capacitor from PV to PGND. Connect all PV pins together.
4, 5, 7, 8	PGND	Power Ground. Connect all PGND pins together.
6	LX	Inductor Connection. Connect LX to the switched side of the inductor. Connect all LX pins together.
10	RS-	Buck Regulator Remote Voltage Sense Negative Input. The common-mode range of this input is ±0.3V.
11	RS+	Buck Regulator Remote Voltage Sense Positive Input. The resistance from RS+ to the remote sense connection should be kept to 2Ω or less to prevent the input current from affecting the output accuracy. The input current is +100µA (typ).
12	SYNC	SYNC I/O. Connect SYNC to AV/GND or an external clock to enable fixed-frequency, forced-PWM-mode operation. When configured as an output (CONFIG.SO[1:0] = 2'b10) connect SYNC to other devices' SYNC inputs.
13	$\overline{\text{RESET}}$	Open–Drain $\overline{\text{RESET}}$ Output. This output remains low for the programmed hold time after the output has reached its regulation level (see the *Electrical Characteristics* table). To obtain a logic signal, pull up $\overline{\text{RESET}}$ with an external resistor.
14	GND	Analog Ground
15	AV	Analog Input Supply
16	SDA	I^2C Data I/O
17	SCL	I^2C Clock Input
—	EP	Internally Connected to PV. Connect EP to PV.

Functional Diagram

Internal Block Diagram



Detailed Description

The MAX20011E/MAX20011F/MAX20011G are high-efficiency, synchronous step-down converters that operate with a 3.0V to 5.5V input voltage range and provides a 0.50V to 1.275V output voltage range. The devices deliver up to 16A of load current and regulate the output voltage over load, line, and temperature ranges. Optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency. The I^2C programmable I/O (SYNC) enables system synchronization. Integrated low RDS_{ON} switches help improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions. The device is offered with a factory-preset output voltage that is dynamically adjustable through the I^2C interface. The output voltage can be set to any desired values between 0.5V to 1.275V in 6.25mV steps. Additional features include adjustable soft-start, power-good delay, DVS rate, overcurrent, and overtemperature protections. See the *Internal Block Diagram*.

$\overline{\text{RESET}}$ Output

The MAX20011E/MAX20011F/MAX20011G feature an open-drain $\overline{\text{RESET}}$ output that asserts when the output voltage deviates from the target regulated voltage by a programmed amount. $\overline{\text{RESET}}$ remains asserted for a fixed timeout period after the output is within the programmed regulation window. Connect $\overline{\text{RESET}}$ to a pullup resistor.

Soft-Start

The MAX20011E/MAX20011F/MAX20011G include a programmable soft-start feature to limit start-up inrush current by forcing the output voltage to slowly ramp up towards its regulation point. The soft-start slew rate is set in the SLEW register.

Dynamic Voltage Scaling

The step-down regulator features dynamic voltage scaling (DVS) to allow loads to margin their supply voltage. The output voltage is set with VID[7:0]. The slew rate during DVS is adjustable with SR[3:0] in the SLEW register. The OV/UV comparators are masked to prevent false $\overline{\text{RESET}}$ assertions during the DVS period.

Shutdown

During shutdown, the output voltage is ramped down at the programmed soft-start slew rate. After soft-shutdown is complete, a 11Ω pulldown resistor is enabled to discharge the remaining output voltage.

Spread-Spectrum Option

The MAX20011E/MAX20011F/MAX20011G feature spread-spectrum (SS) operation to vary the internal operating frequency by +3% relative to the internally generated operating frequency of 2.2MHz or 1.1MHz (typ). This function does not apply to an externally applied oscillation frequency.

Synchronization (SYNC)

SYNC is a factory-programmable I/O. When SYNC is configured as an input, a logic-high on PWM enables SYNC to accept a signal frequency in the range of 1.8MHz < f_{SYNC} < 2.6MHz (CONFIG.FSW = 0) or 0.9MHz < f_{SYNC} < 1.3MHz (CONFIG.FSW = 1). When SYNC is configured as an output, SYNC outputs the internal PWM switching frequency.

Current Limit/Short-Circuit Protection

The devices feature current limiting that protects the device against short-circuit and overload conditions at the output. In the event of an overload condition, the output falls out of regulation and is $V_{OUT} = I_{LIM} \times R_{LOAD}$. In this condition, if the junction temperature exceeds approximately +165°C (typ), a thermal overload circuit turns off the device. The IC turns on again after the junction temperature cools by approximately 15°C. In the event of a short-circuit condition, the high-side MOSFET will reach the high-side MOSFET's current-limit threshold and turn off. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current falls below the low-side MOSFET valley current-limit threshold, the converter allows the high-side MOSFET to turn on again. This cycle repeats until the short-circuit condition is removed.

Boost Refresh

When the device is enabled, the boost capacitor must be charged. This occurs by turning on the low-side FET before initiating soft-start.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the MAX20011E/MAX20011F/MAX20011G. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Applications Information

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}\left(V_{PV} - V_{OUT}\right)}}{V_{PV}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{PV} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)} / 2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge to be equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

Where,

$$\Delta I_L = \frac{\left(V_{PV} - V_{OUT}\right) \times V_{OUT}}{V_{PV} \times f_{SW} \times L}$$

And

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{PV}}$$

I_{OUT} is the maximum output current, and D is the duty cycle.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX20011E/MAX20011F/MAX20011G: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the maximum output current capability of the output. A lower inductor value minimizes size and cost, thus improving large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, a higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. The MAX20011E/MAX20011F/MAX20011G are designed for ΔI_{P_P} equal to 20% to 40% of the full load current. Use the following equation to calculate the inductance:

$$L_{MIN1} = \frac{\left(V_{PV} - V_{OUT}\right) \cdot V_{OUT}}{V_{PV} \cdot f_{SW} \cdot I_{MAX} \cdot 40\,\%}$$

V_{PV} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency is typically 2.2MHz or 1.1MHz. See the *Output Capacitor* section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during continuous output short circuit.

Table 1. Inductor Selection Parameters

PARAMETER	DESCRIPTION
V_{PV}	Nominal Input Voltage. Typically 3.3V or 5V.
V_{OUT}	Nominal Output Voltage
L_{TOL}	Inductor Tolerance. Typically ±20%.
I_{MAX}	8A, 12A, or 16A depending on part number.
f_{SW}	Operating Frequency. This value is 2.2MHz or 1.1MHz unless externally synchronized to a different frequency.

$L_{MIN} = (1 + L_{TOL}) \times L_{MIN1}$

The maximum inductor value recommended is 1.75 times the chosen value from the above formula.

$L_{MAX} = 2.0 \times L_{MIN}$

Select a nominal inductor value based on the following formula. For optimal load transient performance, select the first standard inductor value greater than L_{MIN}:

$L_{MIN} < L_{NOM} < L_{MAX}$

Table 2. Recommended Inductor Values

V_{PV} (V)	V_{OUT} (V)	I_{MAX} (A)	L_{MIN} (nH)	L_{MAX} (nH)	RECOMMENDED (nH)
3.3	1	8	100	200	100, 150
3.3	1	12	70	140	70, 80, 100
3.3	1	16	50	100	60, 70, 80

Inductors are rated for maximum saturation current. The maximum inductor current equals the maximum load current in addition to half of the peak-to-peak ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

The actual peak-to-peak inductor ripple current is calculated in the ΔI_L equation in the *Input Capacitor* section.

The saturation current should be larger than I_{PEAK} or at least in a range where the inductance does not degrade significantly.

Output Capacitor

The compensation is programmable to allow application specific optimization between output capacitance and AC performance. The typical output capacitor range is 150µF (typ) to 700µF (typ). Using the default COMP value of 0xE2 the following equation will provide a good starting point:

$$C_{OUTNOM} = 15 \times I_{MAX} \times \frac{R_{COMP}}{70K\Omega} \times \frac{\mu sec}{V}$$

where I_{MAX} is 8A, 12A, or 16A.

This will place the unity gain bandwidth at approximately 200kHz, which is at the peak of the phase boost resulting the the best phase margin. It is possible to trade-off phase margin for a lower output capacitor at this point. Always measure the phase margin with the fully derated output capacitance to ensure stability.

Programmable Compensation

The device has a programmable zero along with a programmable compensation resistor. In most cases, the zero should be enabled with the gm set to 113µS and resistance set at 300kΩ. This provides the largest phase boost possible, allowing the highest crossover frequency. This is done by setting the upper nibble of the COMP register to 0xE. The compensation resistor is set based on the application requirements. A higher value resistance results in increased AC performance and an increased output capacitor requirement, while a lower compensation resistance results in decreased AC performance with a lower output capacitance requirement.

It is recommended that the compensation optimization be completed on the application PCB to account for PCB

parasitics when trying to maximize AC performance and/or minimize the output capacitance.

Layout Recommendations

- Input Capacitors: Use low-ESR/ESL ceramic capacitors. Place input capacitors across the PV and PGND pins symmetrically on both sides of the IC to minimize the high di/dt input switching current loop area. Smaller (1µF) capacitors should be close to the PV pin, as shown in Figure 1. This provides a shorter low inductance path for the higher frequency component of the switching current.
- Output Capacitors: Use low-ESR/ESL ceramic capacitors. Connect the output capacitor return side to the PGND pin of the IC using a solid copper pour on the same layer or multiple plane/pour layers to minimize the impedance for the return path. For high-di/dt loads, some output capacitors must be placed close to the load. Connect all output capacitors to the V_{OUT} and GND side with copper pour/planes to minimize the impedance.
- RS+ (pin 11) and RS- (pin 10) are differential inputs. Route RS+/- sense lines differentially from the output capacitor to the IC pins. During layout, it is good practice to keep RS+/- traces in a different layer from the switching signal (for example, the LX and BST signals) and far away from other noisy signals to avoid noise-coupling issues with the RS+/- connection.
- The placement and layout of the input RC filter for the analog supply AV (pin 15) is shown in Figure 1. Place a 2.2µF ceramic capacitor across the AV (pin 15) and GND (pin 14). Do not put any GND via between the capacitor and the IC GND (pin 14). Make a reference star type connection from the capacitor GND to the ground plane.
- The BST capacitor trace from the LX pin to the BST pin should be as short as possible to minimize the inductance of the path carrying the BST charging current and high-side gate-drive current.

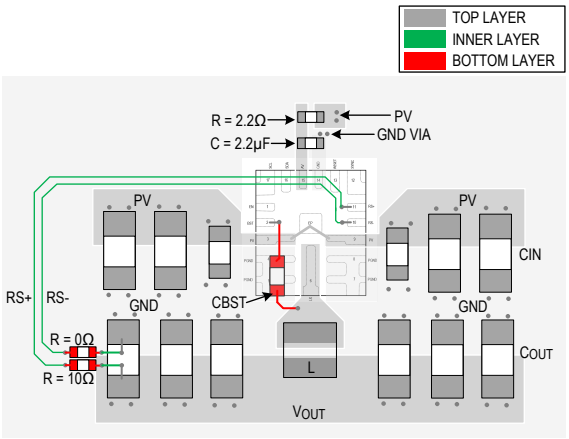
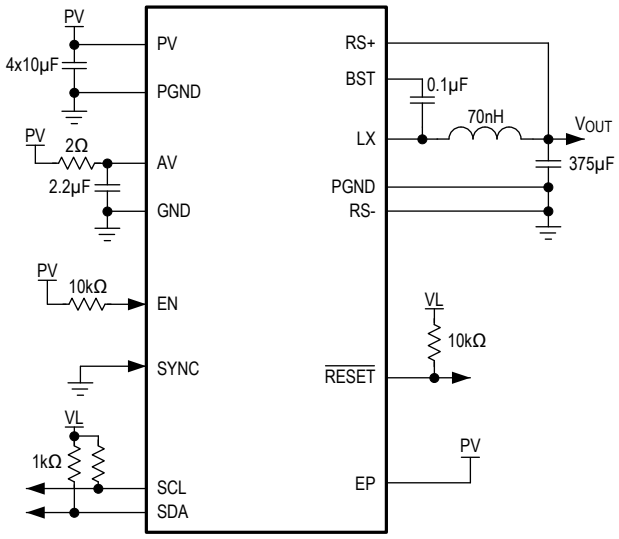


Figure 1. Layout Example

Typical Application Circuit



Ordering Information

PART	I_{OUT} (A)	V_{OUT} (V)	V_{MAX} (V)	SLEW	COMP	CONFIG	CONFIG2	OV/UV	RESET HOLD (ms)	I^2C
MAX20011GAFOA/VY+	16	0.825	1.025	0x09	0xE5	0x0C	0x00	0xFF	0.5	0x39

/VY Denotes side-wettable automotive-qualified parts.

+ Indicates a lead(Pb)-free/RoHS compliant package.

Note: Contact factory for additional part options and custom configurations. Refer to the I^2C register map for factory-selectable customer configurations.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Initial release	—