AK7744VT

24bit 3ch ADC + 24bit 4ch DAC with Audio DSP

1. General Description

The AK7744 is a highly integrated audio processing IC featuring four 24-bit D/A converters, a stereo and monaural input 24-bit A/D and on-chip DSP. The four D/A converters with 107dB dynamic range, and A/D with 97dB dynamic range provide high quality analog performance. These D/A and A/D support sampling frequencies from 8kHz to 48kHz. This device also includes 24kbit of SRAM for delayed audio effects. This programmable DSP is optimized for audio signal processing. The design allows up to 512 execution lines per audio sample cycle, with multiple functions per line. The AK7744 can be used to implement complete sound field control, such as surround control, 3D, parametric equalization, etc. It is packaged in a 64-pin LQFP package.

2. Features

DSP:

- **Word length: 24-bit (Data RAM)**
- **Instruction cycle time: 40ns (512fs, fs=48kHz)**
- **Multiplier: 24 x 16 → 40-bit**
- **Divider: 24 / 24 → 16-bit or 24-bit**
- **ALU: 34-bit arithmetic operation (Overflow margin: 4bit)**
- **24-bit arithmetic and logic operation**
- **Shift+Register: 1, 2, 3, 4, 6, 8 and 15 bits shifted left**
  1, 2, 3, 4, 8 , 14 and 15 bits shifted right
- **Other numbers in parentheses are restricted. Provided with indirect shift function**
- **Program RAM: 512 x 32-bit**
- **Coefficient RAM: 512 x 16-bit**
- **Data RAM: 256 x 24-bit**
- **Offset RAM: 48 x 11-bit**
- **(2048 x 24-bit / 1024 x 24-bit)**
- **Internal Memory: 24kbit SRAM**
- **Sampling frequency: 8kHz to 48kHz**
- **Serial interface port for micro-controller**
- **Master clock: 512fs**
- **Master/Slave operation**
- **Serial signal input port (2 ch): 16/20/24-bit : Output port (2 ch): 24-bit**

Input Selector

- **Normal stereo : 1 full-differential and 5 single-ended Input**
- **Interrupt monaural : 1 full-differential and 1 single-ended Input**

ADC: 2 channels

- **24-bit 64x Over-sampling delta sigma**
- **DR, S/N : 97dBA (Full-differential Input)**
- **S/(N+D) : 86dB**
- **Digital HPF (fc = 1Hz)**
- **Single-ended or Full-differential Input**

ADC: 1 channel (Interrupt input)

- **DR, S/N : 97dBA(Full-differential Input)**

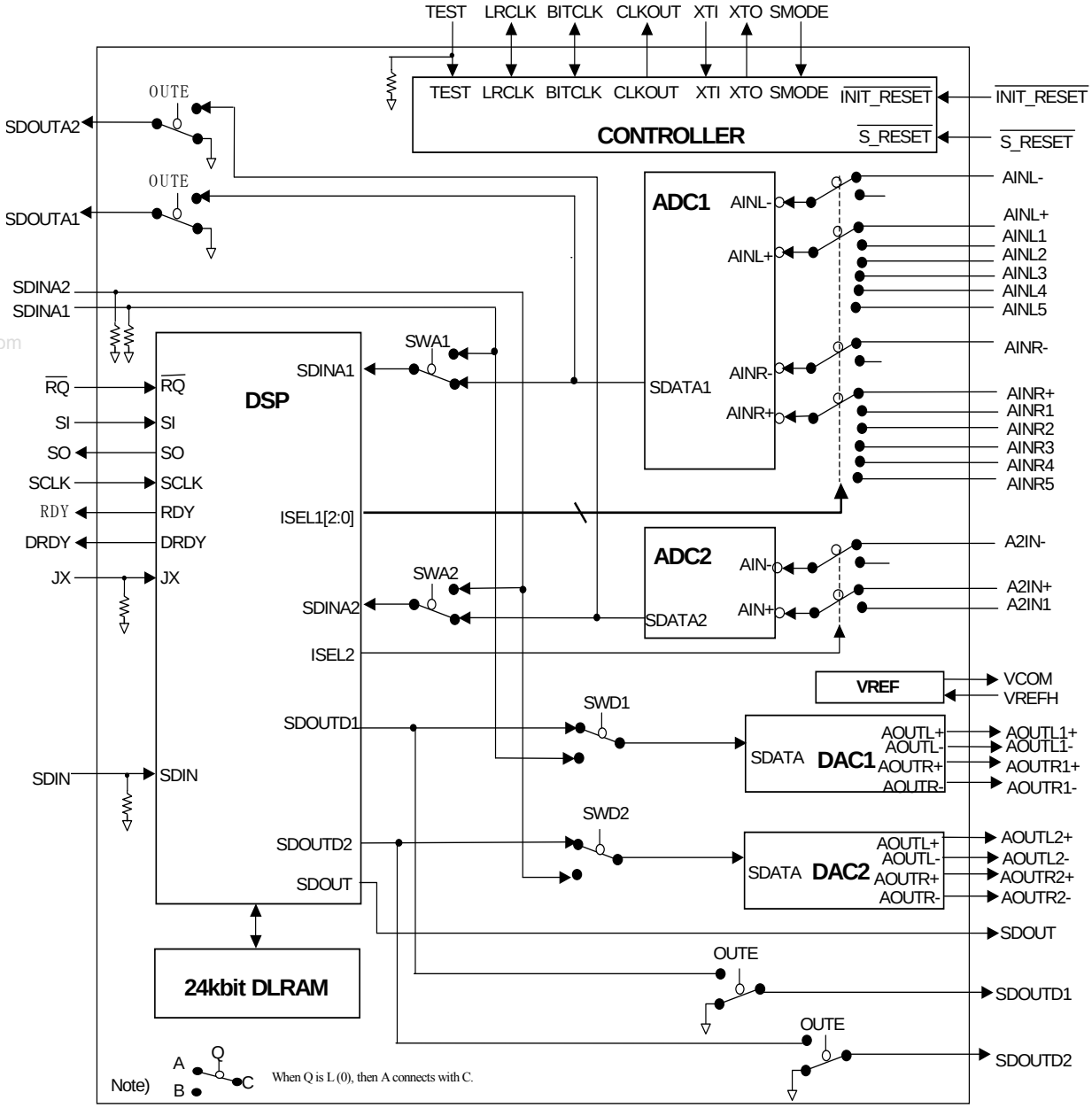
DAC: 4 channels

- **24-bit 128x Over-sampling advanced multi-bit**
- **DR, S/N : 107dBA**
- **S/(N+D) : 92dB**
- **Full-differential Output**

Other

- **Power supply: +3.3V±0.3V**
- **Operating temperature range: -40°C~85°C**
- **Package: 64pin LQFP (0.5mm pitch)**

3. Block diagram

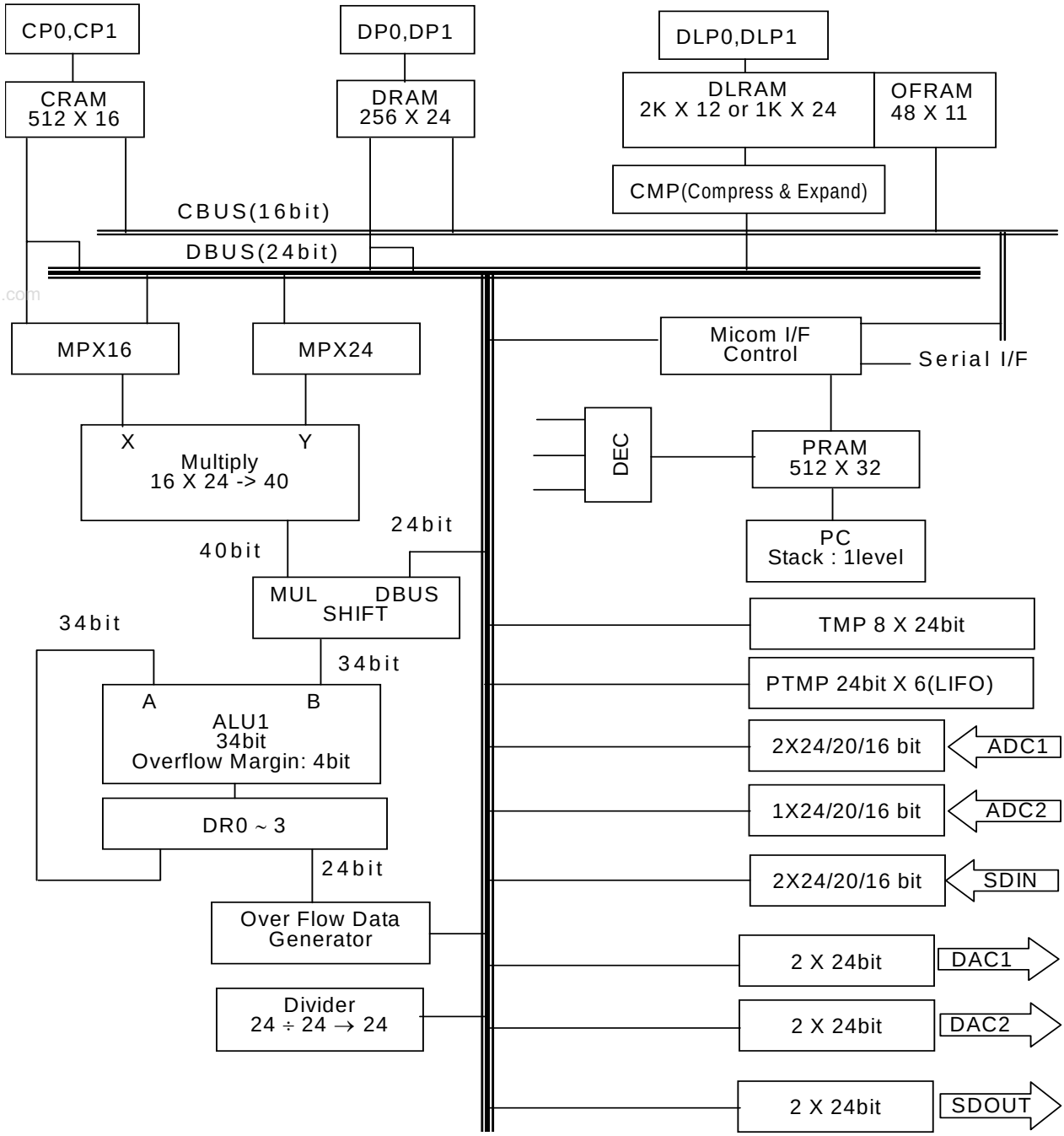


* SWA1,SWA2,SWD1,SWD2,ISEL1[2:0],ISEL2

OUTE [Control register]

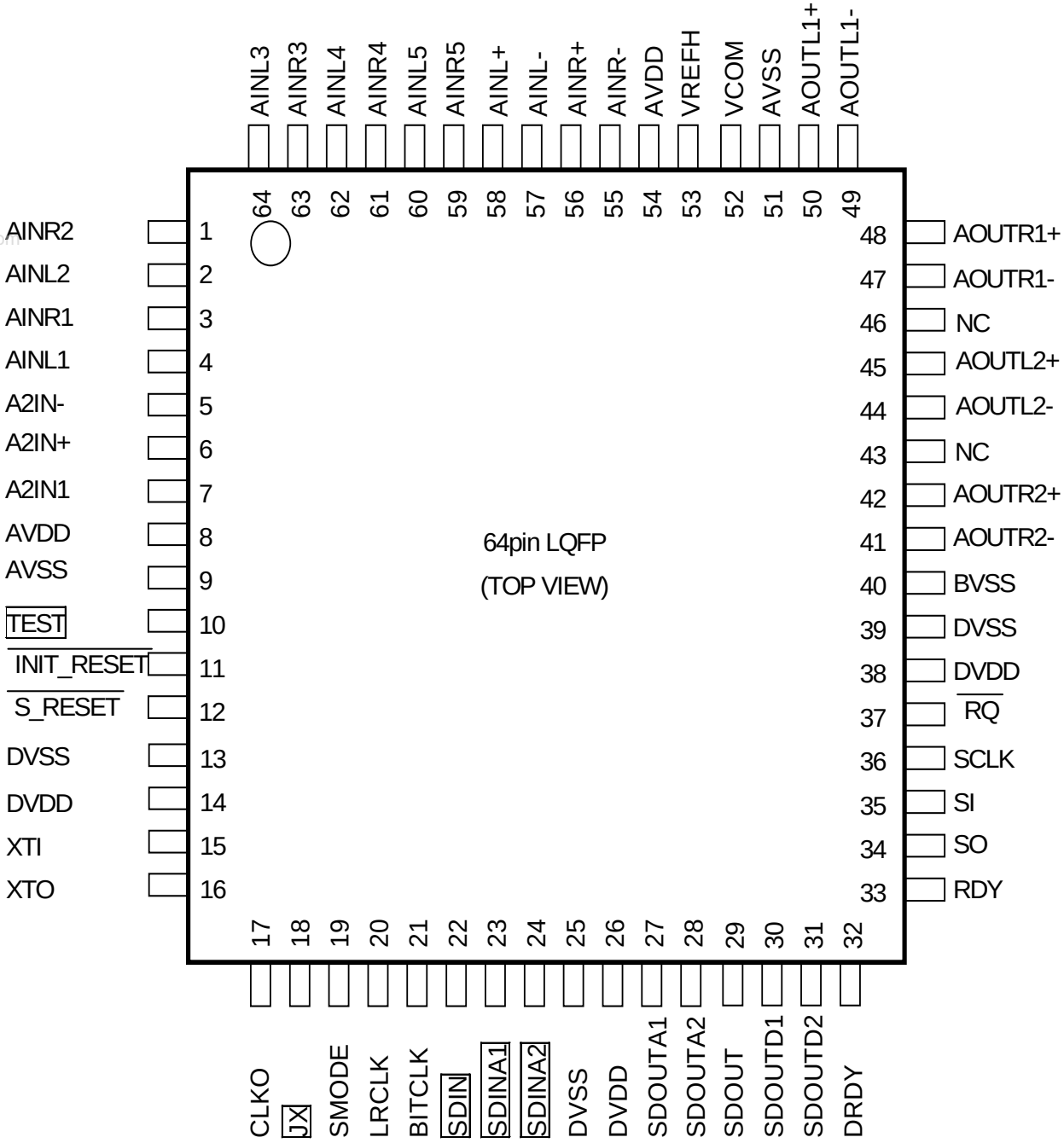
This block diagram is a simplified illustration of the AK7744; it is not a circuit diagram.

◆ **AK7744 DSP Block diagram**



4. Description of Input/Output Pins

(1) Pin layout



Note) JX, SDIN, SDINA1, SDINA2 and TEST are pull-down pins.

(2) Pin function

Pin No.	Pin name	I/O	Function	Classification
1	**AINR2**	I	**ADC1 single-ended analog Rch input pin No.2**	Analog section
2	**AINL2**	I	**ADC1 single-ended analog Lch input pin No.2**	
3	**AINR1**	I	**ADC1 single-ended analog Rch input pin No.1**	
4	**AINL1**	I	**ADC1 single-ended analog Lch input pin No.1**	
5	**A2IN-**	I	**ADC2 analog inverted input pin.**	
6	**A2IN+**	I	**ADC2 analog non-inverted input pin.**	
7	**A2IN1**	I	**ADC2 single-ended analog input pin.**	
8	**AVDD**	-	**Power supply pin for analog section 3.3V (typ)**	Analog Power Supply
9	**AVSS**	-	**Analog ground 0V**	
10	**TEST**	-	**TEST pin**	TEST pin
11	**$\overline{\text{INIT\_RESET}}$**	I	**Reset pin (for initialization)** Used to input "L" initialize the AK7744 at power-on	Reset
12	**$\overline{\text{S\_RESET}}$**	I	**System Reset pin.**	
13	**DVSS**	-	**Ground pin for digital section 0.0V**	Digital Power Supply
14	**DVDD**	-	**Power supply pin for digital section 3.3V(Typ).**	
15	**XTI**	I	**Master clock input pin** Connect a crystal oscillator between this pin and the XTO pin, or input the external CMOS clock signal XTI pin.	System clock
16	**XTO**	O	**Crystal oscillator output pin** When a crystal oscillator is used, it should be connected between XTI and XTO. When the external clock is used, keep this pin open	
17	**CLKO**	O	**Clock output pin** Outputs the XTI clock. Allows the output to be set to "L" by control register setting.	System clock
18	**JX**	I	**External condition jump pin (Pulldown)**	Condition input
19	**SMODE**	I	**Slave/master mode selector pin** Set LRCLK and BITCLK to input or output mode. SMODE="L": Slave mode (These are set to input mode.) SMODE="H": Master mode (These are set to output mode.)	Control
20	**LRCLK**	I/O	**LR channel select Clock pin** SMODE="L": Slave mode: Inputs the fs clock. SMODE="H": Master mode: Outputs the fs clock.	System clock
21	**BITCLK**	I/O	**Serial bit clock pin** SMODE="L": Slave mode: Inputs 64 fs or 48 fs clocks. SMODE="H": Master mode: Outputs 64 fs clocks.	

Pin No.	Pin name	I/O	Function	Classification
22	**SDIN**	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits.	Digital section Serial input data
23	**SDINA1**	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits. Allows the selectable input to SDINA1 port of DSP or DAC1 by control register setting	
24	**SDINA2**	I	**DSP Serial data input pin (Pulldown)** Compatible with MSB/LSB justified 24, 20 and 16 bits. Allows the selectable input to SDINA2 port of DSP or DAC2 by control register setting	
25	**DVSS**	-	**Ground pin for digital section**	Power supply
26	**DVDD**	-	**Power supply pin for digital section 3.3V(Typ).**	
27	**SDOUTA1**	O	**DSP Serial data output pin.** Normally “L” outputs. Allows outputs MSB justified 24-bit data from ADC1 by control register setting.	Digital section Serial output data
28	**SDOUTA2**	O	**DSP Serial data output pin.** Normally “L” outputs. Allows outputs MSB justified 24-bit data from ADC2 by control register setting.	
29	**SDOUT**	O	**DSP Serial data output pin.** Outputs MSB justified 24-bit data.	
30	**SDOUTD1**	O	**DSP Serial data output pin.** Normally “L” outputs. Allows outputs MSB justified 24-bit data to DAC 1 by control register setting.	
31	**SDOUTD2**	O	**DSP Serial data output pin.** Normally “L” outputs. Allows outputs MSB justified 24-bit data to DAC 2 by control register setting.	
32	**DRDY**	O	**Output data ready pin for Microcomputer interface.**	Microcomputer Interface
33	**RDY**	O	**Data write ready output pin for Microcomputer interface.**	
34	**SO**	O	**Serial data output pin for Microcomputer interfaces.**	
35	**SI**	I	**Microcomputer interface serial data input and serial data output control pin.** When SI does not use, leave SI=”L”.	
36	**SCLK**	I	**Microcomputer interface serial data clock pin.** When SCLK does not use, leave SCLK=”H”.	
37	**$\overline{\text{RQ}}$**	I	**Microcomputer interface writes request pin.** $\overline{\text{RQ}}$ =”L”: Microcomputer interface enable.	
38	**DVDD**	-	**Power supply pin for digital section 3.3V(Typ).**	Power supply
39	**DVSS**	-	**Ground pin for digital section**	
40	**BVSS**	-	**Silicon substrate potential 0V**	Power supply

Pin No.	Pin name	I/O	Function	Classification
41	**AOUTR2-**	O	**DAC2 Rch analog inverted output pin.**	Analog section
42	**AOUTR2+**	O	**DAC2 Rch analog non-inverted output pin.**	
43	**NC**	-	**Non connection pin (connect with AVSS pin)**	
44	**AOUTL2-**	O	**DAC2 Lch analog inverted output pin.**	
45	**AOUTL2+**	O	**DAC2 Lch analog non-inverted output pin.**	
46	**NC**	-	**Non connection pin (connect with AVSS pin)**	
47	**AOUTR1-**	O	**DAC1 Rch analog inverted output pin.**	
48	**AOUTR1+**	O	**DAC1 Rch analog non-inverted output pin.**	
49	**AOUTL1-**	O	**DAC1 Lch analog inverted output pin.**	
50	**AOUTL1+**	O	**DAC1 Lch analog non-inverted output pin.**	
51	**AVSS**	-	**Analog ground 0V**	Power supply
52	**VCOM**	O	**Common voltage** Normally, connect to 0.1uF and 10uF capacitors between this pin and AVSS. Don't connect outside cuircuit.)	Analog section
53	**VREFH**	I	**Analog Reference voltage input pin.** Normally, connect to AVDD (pin 54), and connect 0.1uF and 10uF capacitors between this pin and AVSS.	
54	**AVDD**	-	**Power supply pin for analog section 3.3V (typ)**	Power Supply
55	**AINR-**	I	**ADC1 Rch analog inverted input pin.**	Analog section
56	**AINR+**	I	**ADC1 Rch analog non-inverted input pin.**	
57	**AINL-**	I	**ADC1 Lch analog inverted input pin.**	
58	**AINL+**	I	**ADC1 Lch analog non-inverted input pin.**	
59	**AINR5**	I	**ADC1 single-ended analog Rch input pin No.5**	
60	**AINL5**	I	**ADC1 single-ended analog Lch input pin No.5**	
61	**AINR4**	I	**ADC1 single-ended analog Rch input pin No.4**	
62	**AINL4**	I	**ADC1 single-ended analog Lch input pin No.4**	
63	**AINR3**	I	**ADC1 single-ended analog Rch input pin No.3**	
64	**AINL3**	I	**ADC1 single-ended analog Lch input pin No.3**	

5. Absolute maximum rating

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Item	Symbol	min	max	Unit
Power supply voltage				
Analog(AVDD)	VA	-0.3	4.6	V
Digital(DVDD)	VD	-0.3	4.6	V
|AVSS(BVSS)-DVSS| Note 1)	ΔGND		0.3	V
Input current (except for power supply pin)	IIN	-	±10	mA
Analog input voltage AINL+,AINL-,AINR+,AINR-,AINL1, AINR1,AINL2,AINR2,AINL3,AINR3, AINL4,AINR4,AINL5,AINR5,A2IN+, A2IN-,A2IN1,VREFH	VINA	-0.3	VA+0.3	V
Digital input voltage	VIND	-0.3	VD+0.3	V
Operating ambient temperature	Ta	-40	85	°C
Storage temperature	Tstg	-65	150	°C

Note 1) AVSS(BVSS) should be the same level as DVSS.
WARNING: Operation at or beyond these limits may result in permanent damage of the device.
Normal operation is not guaranteed when these limits are exceeded.

6. Recommended operating conditions

(AVSS, BVSS, DVSS = 0 V: All voltages indicated are relative to the ground.)

Items	Symbol	min	typ	max	Unit
Power supply voltage					
AVDD	VA	3.0	3.3	3.6	V
DVDD	VD	3.0	3.3	VA	V
Reference voltage (VREF)					
VREFH Note 1)	VRH		VA		V

Note 1) VREFH normally connects with AVDD.

Note: The analog input and output voltages are proportional to the VREFH voltages.

7. Electric characteristics

(1) Analog characteristics

(Unless otherwise specified, Ta = 25°C; AVDD, DVDD = 3.3V; VREFH = AVDD;
BITCLK = 64 fs; Signal frequency 1 kHz;
Measuring frequency = 20 Hz to 20 kHz @48kHz;
DSP section in the reset state; ADC with all differential inputs)

	Parameter	min	typ	max	Unit
ADC1 Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (-1dB) (Note1)	76	86		dB
	Dynamic range fs = 48kHz (A filter) (Note2)	89	97		dB
	S/N fs = 48kHz (A filter)	89	97		dB
	Inter-channel isolation (f =1 kHz) (Note3)	90	120		dB
	DC accuracy				
	Inter-channel gain mismatching		0.1	0.3	dB
	Analog input				
	Input voltage(Differencial) (Note4)	±1.85	±2.00	±2.15	Vp-p
	Input Voltage(Single-ended) (Note5)	1.85	2.00	2.15	Vp-p
	Input impedance (Note6)	22	33		kΩ
ADC2 Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (-1dB) (Note1)	76	86		dB
	Dynamic range fs = 48kHz (A filter) (Note2)	89	97		dB
	S/N fs = 48kHz (A filter)	89	97		dB
	Analog input				
	Input voltage	1.85	2.00	2.15	Vp-p
	Input impedance	22	33		kΩ
DAC Section	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) fs = 48kHz (0dB)	80	92		dB
	Dynamic range fs = 48kHz (A filter) (Note2)	99	107		dB
	S/N fs = 48kHz (A filter)	99	107		dB
	Inter-channel isolation (f =1 kHz) (Note7)	90	115		dB
	DC accuracy				
	Inter-channel gain mismatching (Note7)		0.2	0.5	dB
	Analog output				
	Output voltage (AOUT+)-(AOUT-) (Note8)	3.36	3.66	3.96	Vp-p
	Load resistance	5			kΩ

Note:

1. In case of the using single-ended input this value does not guarantee.
2. Indicates S/(N+D) when a -60 dB signal is applied.
3. Specified for L and R of each input selector.
4. This applies to AINL+, AINL-, AINR+ , AINR-, A2IN+ and A2IN- pins.
   The fullscale (ΔAIN = (AIN+) - (AIN-)) can be represented by (±FS = ±(VREFH-AVSS)×(2.0/3.3)).
5. This applies to AINL1,AINR1,AINL2,AINR2,AINL3,AINR3,AINL4,AINR4,AINL5,AINR5 and A2IN1. The fullscale of single-ended input is (FS=(VREFH-AVSS) × (2.0/3.3)).
6. This applies to AINL1, AINR1, AINL2, AINR2, AINL3, AINR3, AINL4, AINR4, AINL5, AINR5 AINL+,AINL-,AINR+, AINR-,A2IN+,A2IN- and A2IN1.
7. Specified for L and R of each DAC.
8. The full-scale output voltage when VREFH=AVDD.

(2) DC characteristics

(VDD=AVDD=DVDD=3.0~3.6V,Ta=25°C)

Parameter	Symbol	min	typ	max	Unit
High level input voltage	VIH	80%VDD			V
Low level input voltage	VIL			20%VDD	V
High level output voltage Iout=-100μA	VOH	VDD-0.5			V
Low level output voltage Iout=100μA	VOL			0.5	V
Input leak current Note 1)	Iin			±10	μA
Input leak current (pull-down) Note 2)	Iid		22		μA
Input leak current (XTI pin)	Iix		26		μA

Note:

1. The pull-down and XTI pins are not included.
2. The pull-down pins are JX, SDIN, SDINA1 and SDINA2. The pull-down resistor value is 150kΩ.
3. Regarding the input/output levels in the text, the low level will be represented as "L" or 0, and the high level as "H" or 1. In principle, "0" and "1" will be used to represent the bus (serial/parallel) such as registers.

(3) Current consumption

(AVDD=DVDD=3.0V~3.6V, Ta=25°C; master clock (XTI)=24.576MHz=512fs[fs=48kHz];
When operating the DAC four channels with 1kHz sinusoidal waves and –1dBFS-scale input to each of ADC 2ch analog input pins)

Power supply					
Parameter		min	typ	max	Unit
Power supply current					
a) AVDD			60		mA
b) DVDD	Note 1)		40		mA
c) Total(a+b)			100	135	mA
2) $\overline{\text{INIT\_RESET}}$ ="L"	Note 2)		6.0		mA
Power consumption					
1) During operation					
a) AVDD			198		mW
b) DVDD	Note 1)		132		mW
c) Total(a+b)			330	486	mW
2) $\overline{\text{INIT\_RESET}}$ ="L"	Note 2)		19.8		mW

Note:

1) Varies slightly according to the frequency used and contents of the DSP program.
2) This is a reference value when using a crystal oscillator. Since most of the power current during a reset is pulled from the oscillator section, the value changes slightly depending on the crystal oscillators type and external circuits used. Therefore this is “reference value”.

(4) Digital filter characteristics

Values described below are design values cited as references.

4-1) ADC Section:

(Ta=25°C; AVDD,DVDD =3.0V~3.6V; fs=48kHz; HPF=off)

parameter	Symbol	min	typ	max	Unit
Pass band (-0.02dB)	PB	0		21.768	kHz
(-6.0dB)		0	24.00		kHz
Stop band (Note 1)	SB	26.5			kHz
Pass band ripple (Note 2)	PR			±0.005	dB
Stop band attenuation (Note3,4)	SA	80			dB
Group delay distortion	ΔGD			0	us
Group delay (Ts=1/fs)	GD		29.3		Ts

Note: : HPF response does not include.

1. The stop band is from 26.5kHz to 3.0455MHz when fs = 48kHz.
2. The pass band is from DC to 21.5kHz from DC when fs = 48kHz.
3. When fs = 48kHz, the analog modulator samples analog input at 3.072MHz. The digital filter does not attenuate the input signal in the multiple bands (n x 3.072MHz ± 21.99kHz; n=0, 1, 2, 3...) of the sampling frequency.

4-2) DAC section

(Ta=25°C; AVDD,DVDD =3.0V~3.6V; fs=48kHz)

parameter	Symbol	min	Typ	max	Unit
Digital filter					
Pass band ±0.07dB (Note 1)	PB	0		21.7	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 1)	SB	26.2			kHz
Pass band ripple	PR			±0.07	dB
Stop band attenuation	SA	47			dB
Group delay (Note 2)	GD	-	15		Ts
Digital filter+SCF					
Amplitude characteristics 0~20.0kHz			±0.5		dB

Note:

1. The pass band and stop band frequencies are proportional to "fs" (system sampling rate), and represent PB=0.4535fs(@-0.06dB) and SB=0.546fs, respectively.
2. This calculated delay time, which occurs in the digital filter, is from setting the 24-bit data of both channels on input register to the output of analog signal.

(5) Switching characteristics

5-1) System clock

(AVDD=DVDD=3.0V~3.6V,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Master clock (XTI)					
a) With a crystal oscillator					
512fs: frequency	fMCLK	16.384	24.576	24.576	MHz
1536fs: frequency 2048fs: frequency	fMCLK	22.5792	24.576	24.576	MHz
3072fs: frequency	fMCLK	24.576	24.576	24.576	MHz
b) With a external clock:					
Duty factor (≤18.432MHz) (>18.432MHz)		40 45	50 50	60 55	%
512fs: frequency	fMCLK	16	24.576	25	MHz
1536fs: frequency 2048fs: frequency	fMCLK	22	24.576	25	MHz
3072fs: frequency	fMCLK	24	24.576	25	MHz
: High level width : Low level width	tMCLKH tMCLKL	16 16			ns ns
Clock rise time Clock fall time	tCR tCF			6 6	ns ns
LRCLK Sampling frequency	fs	32	48	49	kHz
1536fs: frequency	fs	14.7	16	16.3	kHz
2048fs: frequency	fs	11.025	12	12.2	kHz
3072fs: frequency	fs	8	8	8.1	kHz
			1		fs
Slave mode :clock rise time Slave mode :clock fall time	tLR tLF			6 6	ns ns
BITCLK Note 1)	fBCLK	48	64		fs
Slave mode: High level width Slave mode: Low level width	tBCLKH tBCLKL	150 150			ns ns
Slave mode :clock rise time Slave mode :clock fall time	tBR tBF			6 6	ns ns

Note 1) 48fs mode can be use only in slave mode.

5-2) Reset

(AVDD=DVDD=3.0V~3.6V,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
$\overline{\text{INIT\_RESET}}$ Note 1)	tRST	150			ns
$\overline{\text{S\_RESET}}$	tRST	150			ns

Note 1) "L" is acceptable when power is turned on, but "H" needs a stable master clock input.

5-3) Audio interface

(AVDD=DVDD=3.0V~3.6V,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BITCLK frequency	fBCLK	48	64		fs
BITCLK low level width	tBCLKL	150			ns
BITCLK high level width	tBCLKH	150			ns
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK "↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			80	ns
Delay time from BITCLK to serial data output	tBSOD			80	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns
Master mode					
BITCLK frequency	fBCLK		64		fs
BITCLK duty factor			50		%
Delay time from BITCLK"↑" to LRCLK	tBLRD	40			ns
Delay time from LRCLK to BITCLK"↑"	tLRBD	40			ns
Delay time from LRCLK to serial data output	tLRD			80	ns
Delay time from BITCLK to serial data output	tBSOD			80	ns
Serial data input latch hold time	tBSIDS	40			ns
Serial data input latch setup time	tBSIDH	40			ns

5-4) Microcomputer interface

(AVDD=DVDD=3.0V~3.6V,Ta=-40~85°C,CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcomputer interface signal					
$\overline{RQ}$ Fall time	tWRF			8	ns
$\overline{RQ}$ Rise time	tWRR			8	ns
SCLK fall time	tSF			8	ns
SCLKrise time	tSR			8	ns
SCLK low level width	tSCLKL	30			ns
SCLK high level width	tSCLKH	30			ns
Microcomputer to AK7744					
Time from $\overline{RESET}$ "↓" to $\overline{RQ}$ "↓"	tREW	200			ns
Time from $\overline{RQ}$ "↑" to $\overline{RESET}$ "↑" Note 1)	tWRE	200			ns
$\overline{RQ}$ high level width	tWRQH	200			ns
Time from $\overline{RQ}$ "↓" to SCLK"↓"	tWSC	200			ns
Time from SCLK"↑" to $\overline{RQ}$ "↑"	tSCW	6×tMCLK			ns
SI latch setup time	tSIS	100			ns
SI latch hold time	tSIH	100			ns
AK7744 to microcomputer					
Time from SCLK"↑" to DRDY"↓"	tSDR			3×tMCLK	ns
Time from SI"↑"to DRDY"↓"	tSIDR			3×tMCLK	ns
SI high level width	tSIH	3×tMCLK			ns
Delay time from SCLK"↓" to SO output	tSOS			100	ns
AK7744 to microcomputer (RAM DATA read-out)					
SI latch setup time (SI="H")	tRSISH	30			ns
SI latch setup time (SI="L")	tRSISL	30			ns
SI latch hold time	tRSIH	30			ns
Time from SCLK"↓" to SO	tSOD			100	ns
AK7744 to microcomputer (CRC result output) Note 2)					
Delay time from $\overline{RQ}$ "↑" to SO output	tRSOC			150	ns
Delay time from $\overline{RQ}$ "↓" to SO output Note 3)	tFSOC	50			ns

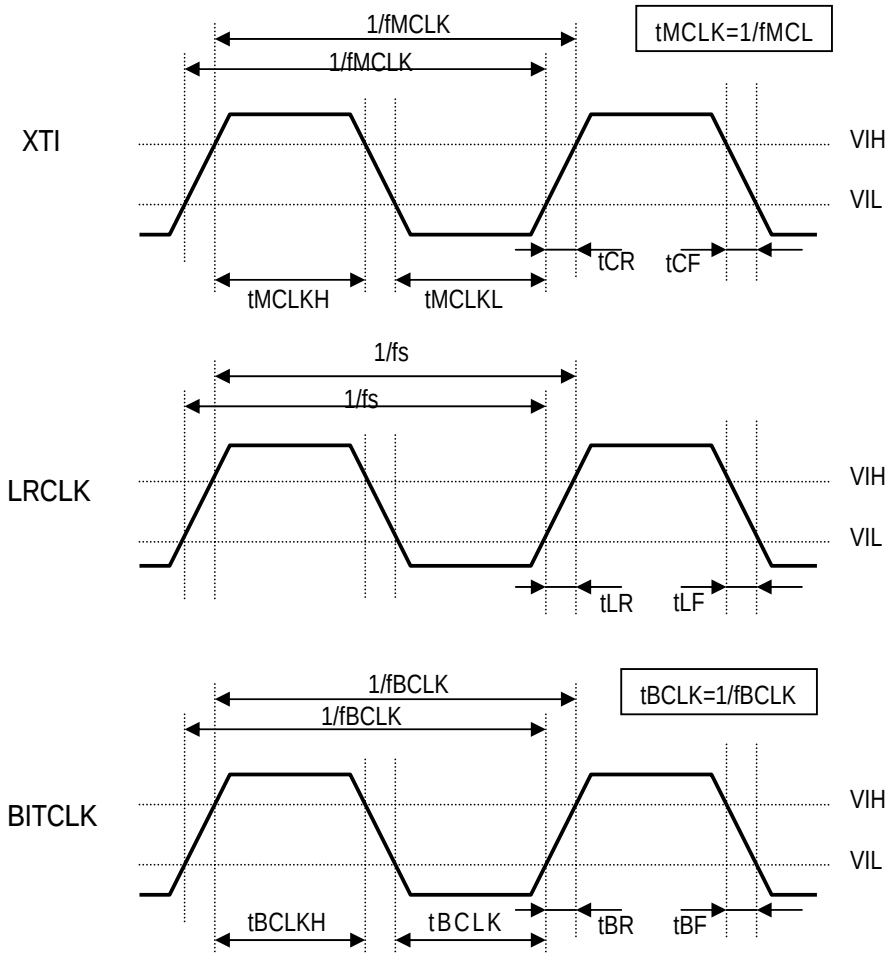
Note 1) Except for external jump code set at reset state.

Note 2) When a surplus of the serial data D(x) divided by the generated polynomials expression G(x) is equal to the R(x) then the SO indicates "H".

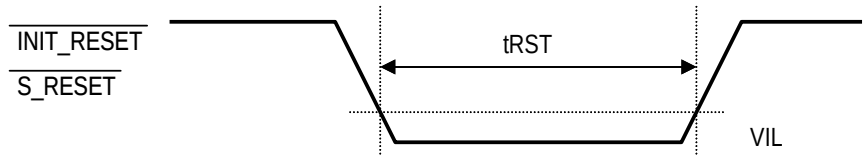
Note 3) The Microcontroller should read 50ns before falling the $\overline{RQ}$. (It does not use RUN time.)

(6) Timing waveform

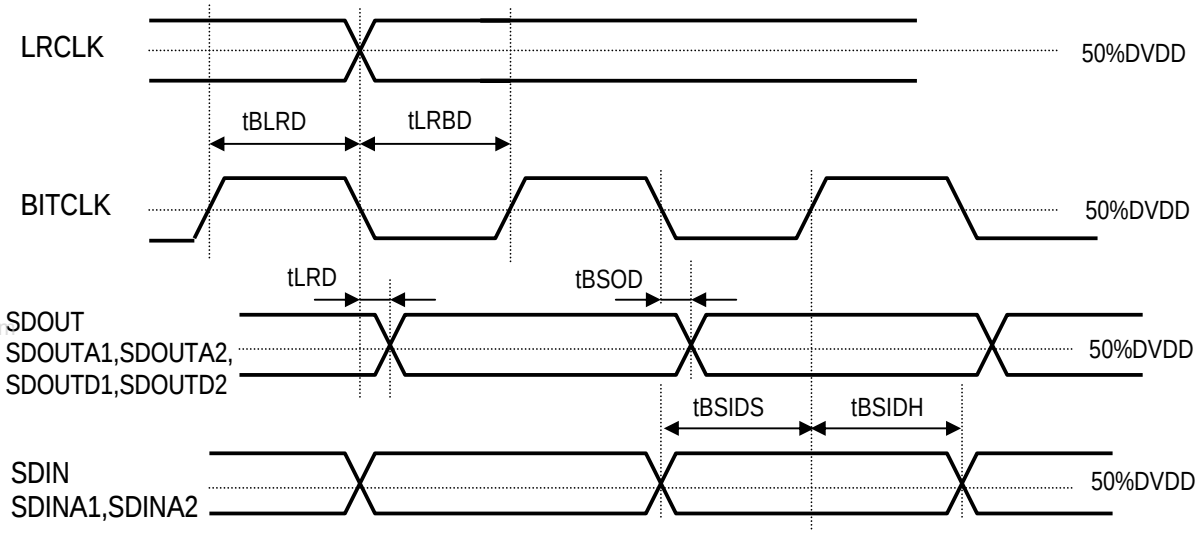
6-1) System clock



6-2)Reset signal

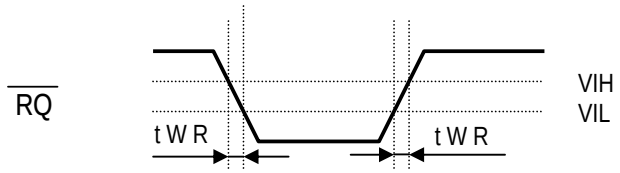


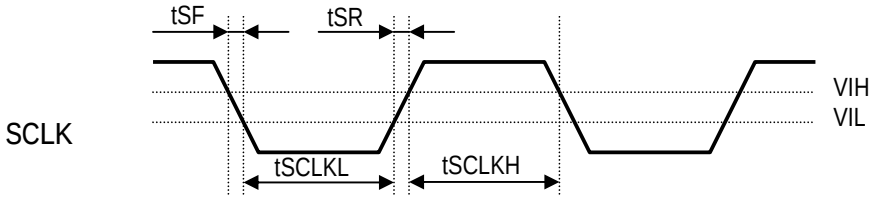
6-3) Audio interface



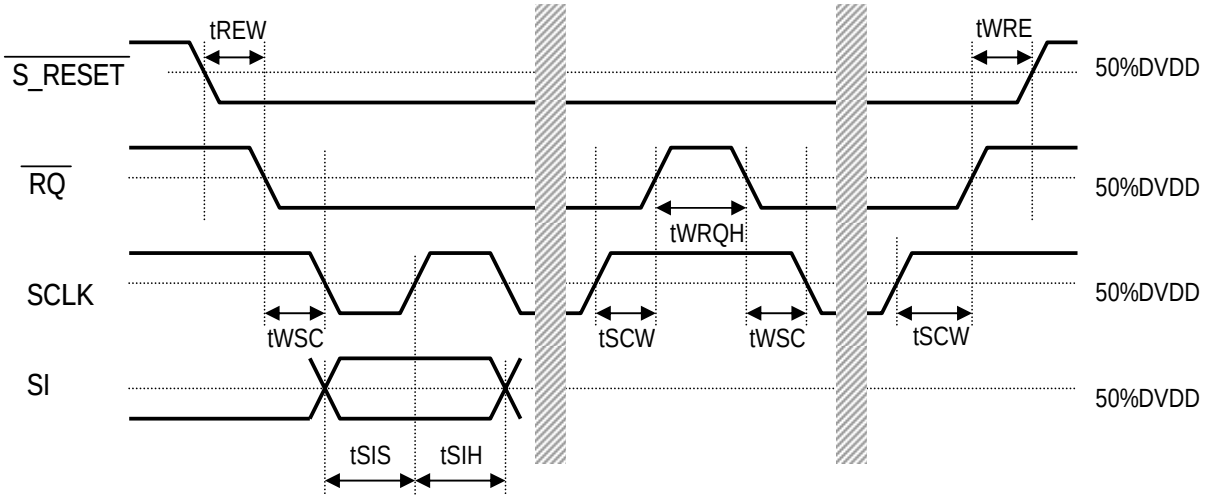
6-4) Microcomputer interface

* Microcomputer interface signals





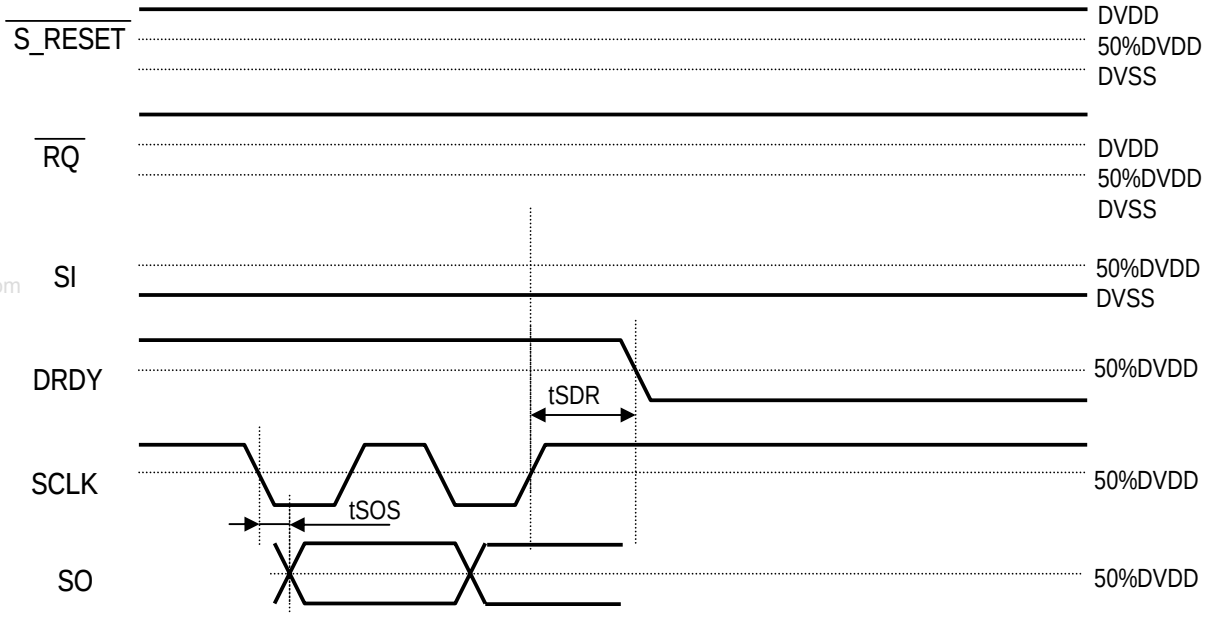
* Microcomputer to AK7744



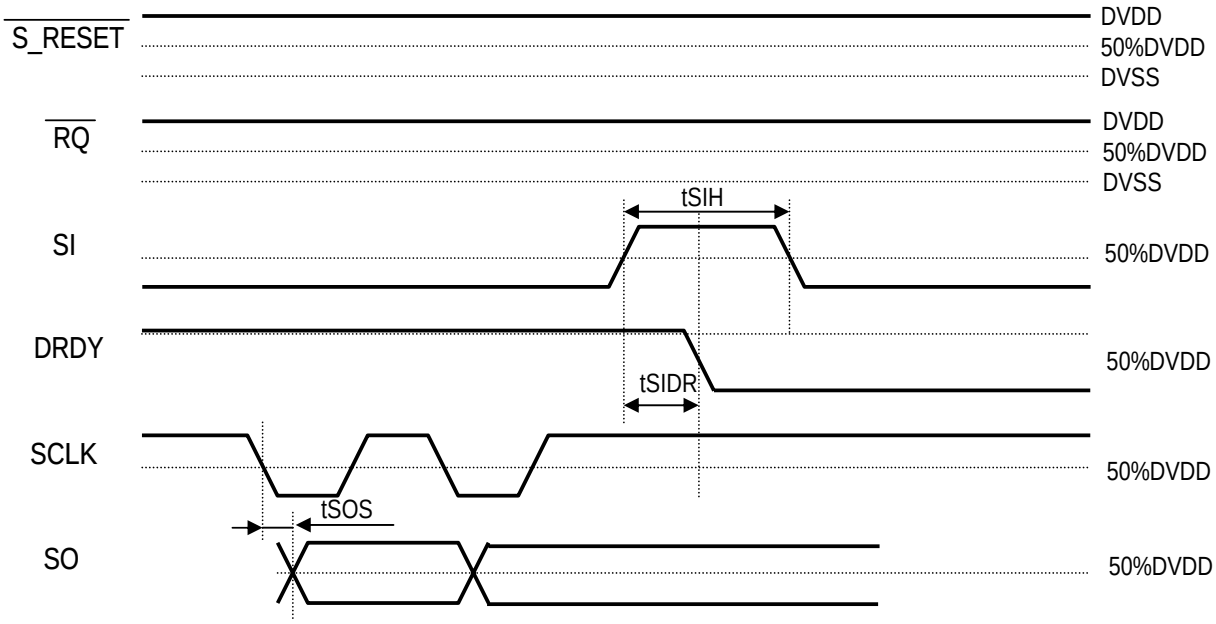
NOTE : Timing for RUN state is the same except that $\overline{\text{RESET}}$ is set to an "H"
$\overline{\text{RESET}}$ represents system reset in normal use.

* AK7744 to Microcomputer (DBUS data)

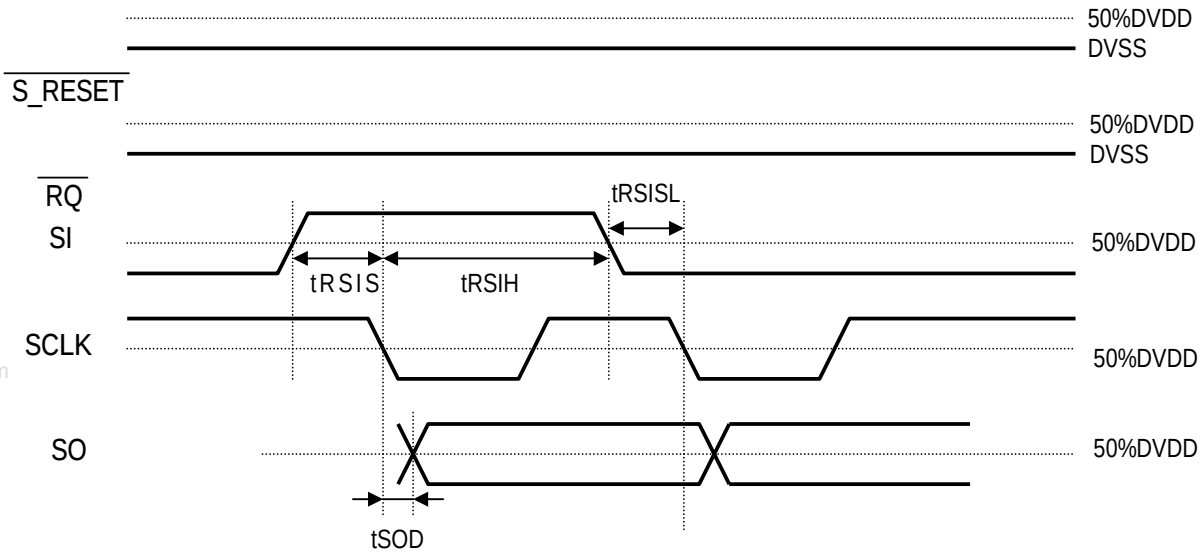
1) DBUS data in case of 24-bit data output.



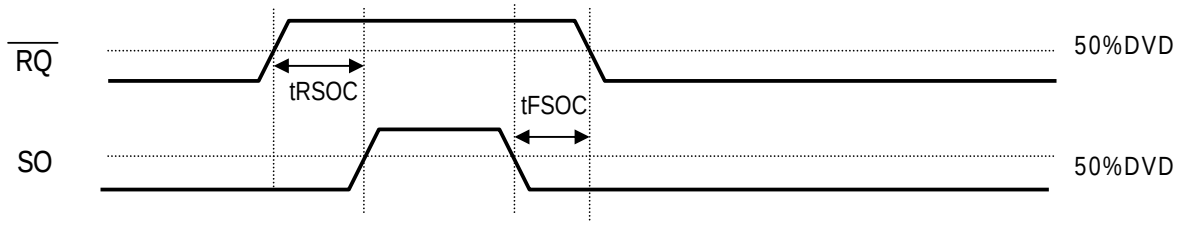
2) DBUS data less than 24 bits data output (in case of using SI)



* AK7744 to Microcomputer (RAM DATA Read-out)



* AK7744 to Microcomputer (RAM DATA Read-out) (CRC Check : the surplus of {D(x)/G(x)}=R(x))



8. Function Description

(1) Various setting

1-1) SMODE : slave and master mode selector pin

Sets LRCLK and BITCLK to either inputs or outputs.

a) Slave mode :SMODE="L" LRCLK(1fs) and BITCLK (64fs or 48fs) become inputs.

b) Master mode: SMODE="H" LRCLK (1fs) and BITCLK (64fs) become outputs.

Note) SMODE pin is to be fixed “L” or “H”. Therefore, after release an initial reset ($\overline{\text{INIT\_RESET}}$ =”L”→”H”) SMODE must change during the system reset state ($\overline{\text{S\_RESET}}$ ="L") . This is especiallty critical in slave mode, as phase matching between internal and external clocks begins when a system reset occurs (See (8.(4)) Resetting). DO NOT CHANGE SMODE during runtime, as this will cause an error.

(2) Control registers

The control registers can be set via the microcomputer interface or the control pins. These registers consist of 4 addresses and each register is 8-bits. For the value to be written in the control registers see the microcomputer interface description. The following describes the control register map.

TEST: for TEST (input 0,X: it ignore input data, but should input 0).

Command Code		Name	D7	D6	D5	D3	D4	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	CFS1	CFS0	DIF	DIF1	DIF0	DISCK	SELCKO	X	00h
64h	74h	CONT1	DATARAM	RM	BANK	CMP_N	SS[1]	SS[0]	TEST	X	00h
68h	78h	CONT2	SWA2	SWA1	SWD2	SWD1	PSDA2	OUTE	TEST	X	00h
6Ch	7Ch	CONT3	ISEL2	ISEL1[2]	ISEL1[1]	ISEL1[0]	PSAD2	PSAD1	TEST	X	00h

1. CONT0 can be set only at system reset ($\overline{\text{S\_RESET}}$ ="L").
2. CONT1~2 should be set at system reset ($\overline{\text{S\_RESET}}$ ="L"), otherwise some noise can come out.
3. The input selector (CONT3) can be changed “on the fly”. However it must change synchronously with the initialization of the ADC’s digital interface. For example: ADC1, the input selector (CONT3: ISEL1[2:0]) and CONT3:PSAD1=1 should change at the same time. After CONT3:PSAD1=0, then the ADC1 digital interface can be initialized. When changing CONT3 on the fly, some noise will occur, so an external mute circuit after the DAC output should be used. ADC2 can also cause some noise.
4. Default setting is the same value as an initial reset ($\overline{\text{INIT\_RESET}}$ =”L”).

2-1) CONT0 : clock and interface selector

This register is enabled only at system reset state ($\overline{\text{S\_RESET}}$ ="L").

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
60h	70h	CONT0	CFS1	CFS0	DIF	DIF1	DIF0	DISCK	SELCKO	X	00h

① D7,D6:CFS1 CFS0 Master clock select

Mode	CFS1(D7)	CFS0(D6)	Enable fs []: Master clock Note) It can use only as following frequency.
1	0	0	512fs(fs=48kHz[24.576MHz],44.1kHz[22.5792MHz],32kHz[16.384MHz])
2	0	1	1536fs(fs=16kHz[24.576MHz],14.7kHz[22.5792MHZ])
3	1	0	2048fs(fs=12kHz[24.576MHz],11.025kHz[22.5792MHz])
4	1	1	3072fs(fs=8kHz[24.576MHz])

② D5:DIF Audio interface selector

0:AKM method

1: I^2S compatible (In this case, all input / output pins are I^2S compatible.)

③ D4,D3:DIF1,DIF0 SDIN Input mode selector

Mode	D4	D3	
1	0	0	MSB justified (24bit)
2	0	1	LSB justified (24bit)
3	1	0	LSB justified (20bit)
4	1	1	LSB justified (16bit)

Note) When D5= 1, the state is I^2S compatible independently of mode setting. In this case, set D4 and D3 to Mode 1.

④ D2:DISCK LRCLK,BITCLKOutput control

0: Normal Operation

1: In MASTER mode, this setting can fix BITCLK="L" and LRCLK="H". (Note In case of I^2S compatible setting, it become LRCLK="L".) This setting is available only when using the AK7744's analog inputs and analog outputs. When this mode is selected, SDIN and SDOUT are not available.

⑤ D1:SELCKO CLKO Output selector.

0:CLKO outputs the same frequency as XTI.

1:CLKO outputs "L" level.

Note) When CLKO="1", after setting CONT0 (when the last clock of SCLK rise up) CLKO will change its frequency.

⑥ D0: Always 0

Note) Underlined settings of ①~⑤ = default setting.

2-2) CONT1: RAM control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
64h	74h	CONT1	DATARAM	RM	BANK	CMP_N	SS[1]	SS[0]	TEST	X	00h

① D7:DATARAM DATARAM addressing mode selector

0:Ring addressing mode

1:Linear addressing mode

DATARAM has 256-word x 24-bit and has 2 addressing pointers (DP0, DP1).

In Ring addressing mode: Starting address increments by 1 every sampling period.

In Linear addressing mode: Starting address is always the same, DP0 = 00h and DP1 = 80h.

② D6:RM: Depress bit mode

0: SIGN bit

1: Random data

When it selects Compress & Depress mode (D3:CMP_N = 0), this bit decides depressed LSB bits.

③ D5:BANK DLRAM Setting

0:24bit 1kword

1:12bit 2kword

④ D3:CMP_N 12-bitDLRAM Compress & Depress selector

When BANK[D5]=1 is selected, this register can set up ON or OFF of its compress/depress function.

0: Compress & Depress function ON

When it writes to DLRAM the DBUS data is compressed to 12-bit and when it read from DLRAM, the data. is depressed to 16-bit.

1: Compress & Depress function OFF

It always writes to DLRAM MSB 12-bit of DBUS data and it reads from the MSB 12-bit of DLRAM and ad d to 000h for LSB bits.

⑤ D2,D1:SS[1:0] DLRAM setting of sampling timing.

Mode	D2	D1	RAM mode
0	0	0	Update every sampling time
1	0	1	Update every 2 sampling time
2	1	0	Update every 4 sampling time
3	1	1	Update every 8 sampling time

Note) When the mode 1,2 or 3 is selected, it comes out aliasing.

⑥ D0: Input always 0

Note) Underlined settings of ①~⑤ = default setting.

2-3) CONT2 : DA,DSP control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
68h	78h	CONT2	SWA2	SWA1	SWD2	SWD1	PSDA2	OUTE	TEST	X	00h

① D7:SWA2 internal path setting (see p.2 Block diagram)
0:Normal operation (SDINA2 of DSP is input from ADC2)
1:SDINA2 pin connects with SDINA2 of DSP block. Its format is same as SDIN.

② D6:SWA1 internal path setting (see p.2 Block diagram)
0:Normal operation (SDINA1 of DSP is input from ADC1)
1:SDINA1 pin connects with SDINA2 of DSP block. Its format is same as SDIN.

③ D5:SWD2 internal path setting (see p.2 Block diagram)
0:Normal operation (SDOUTD2 of DSP outputs to DAC2)
1:SDINA2 pin connects with SDATA of DAC2. Its format is 24bit MSB first or I^2S.

④ D4:SWD1 internal path setting (see p.2 Block diagram)
0:Normal operation (SDOUTD1 of DSP outputs to DAC1)
1:SDINA1 pin connects with SDATA of DAC1. Its format is 24bit MSB first or I^2S.

⑤ D3:PSDA2 DA2 power save control
0:Normal operation
1:DA2 power save
In the case of not using DA2, set this value to "1" and DA2 will RESET.
This can be useful for reducing power consumption.
When changing to normal operation, set this value to "0" at system reset.

⑥ D2:OUTE Output enable (see Block-diagram)
0:Normal operation (SDOUTA1,SDOUTA2,SDOUTD1,SDOUTD2="L")
1: SDOUTA1,SDOUTA2,SDOUTD1 and SDOUTD2 are enable to output.

⑦ D1:TEST
0:Normal operation
1:Test mode (Do NOT use this mode)

⑧ : Always input 0
Note): Underlined settings of ①~⑤ = default setting.

2-4) CONT3: ADC control

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
6Ch	7Ch	CONT3	ISEL2	ISEL1[2]	ISEL1[1]	ISEL1[0]	PSAD2	PSAD1	TEST	X	00h

① D7: ISEL2 ADC2 Analog input selector setting

0:A2IN-,A2IN+
1:A2IN1

② D6,D5,D4:ISEL1[2:0] ADC1 Analog input selector setting

ISEL1[2](D6)	ISEL1[1](D5)	ISEL1[0](D4)	Analog input pin
0	0	0	AINL-,AINL+,AINR-,AINR+
0	0	1	AINL1,AINR1
0	1	0	AINL2,AINR2
0	1	1	AINL3,AINR3
1	0	0	AINL4,AINR4
1	0	1	AINL5,AINR5

③ D3:PSAD2 ADC2 power save

0:Normal operation
1:ADC2 power save

In the case of not using ADC2, set this value to "1" and ADC2 will be in RESET.
This is useful for reducing power consumption.
The digital output signals of ADC2 will 00000h.
When changing to normal operation, set this value to "0" at system reset.

④ D2:PSAD1 ADC1 power save

0:Normal operation
1:ADC1 power save

In the case of not using ADC1, set this value to "1" and ADC1 will be in RESET.
This is useful for reducing power consumption.
The digital output signals of ADC1 will 00000h.
When changing to normal operation, set this value to "0" at system reset.

⑤ D1:TEST

0:Normal operation
1:TESTmode (Do NOT use this mode)

⑥ D0: Always input 0

Note) Un Underlined settings of ①~⑤ = default setting.

(3) Power supply startup sequence

Turn on the power and reset the AK7744 by setting the $\overline{\text{INIT\_RESET}}$ = "L" and $\overline{\text{S\_RESET}}$ = "L". The VREF (Analog reference level) of the AK7744 is set and its control registers are initialized by setting the $\overline{\text{INIT\_RESET}}$ = "H". The time for the VREF to become stable depends on the external capacitance on the VCOM pin. For example, connecting a 10uF and a 0.1uF capacitor takes about 300ms before VREF is stable. Additional capacitance will increase this time, and this rise time is the MINIMUM amount of time for a stable VREF. You can guarantee a stable VREF by waiting longer than this minimum time after $\overline{\text{INIT\_RESET}}$ ="H" to $\overline{\text{S\_RESET}}$ ="H" (ADC and DAC start to work.).

Normally, $\overline{\text{INIT\_RESET}}$ sequence is executed when power is applied to the device.

Note 1): Set $\overline{\text{INIT\_RESET}}$ = "H" after setting the oscillation when a crystal oscillator is used.
This setting time may differ depending on the crystal oscillator and its external circuit.

NOTE: Do not stop the system clock (slave mode: XTI, LRCLK, BITCLK, master mode: XTI) except when $\overline{\text{S\_RESET}}$ = "L". If these clock signals are not supplied, excess current will flow due to dynamic logic that is used internally, and an operation failure may result.

Don't set $\overline{\text{S\_RESET}}$ ="H" during $\overline{\text{INIT\_RESET}}$ ="L", or else the the crystal oscillator will stop or become unstable.

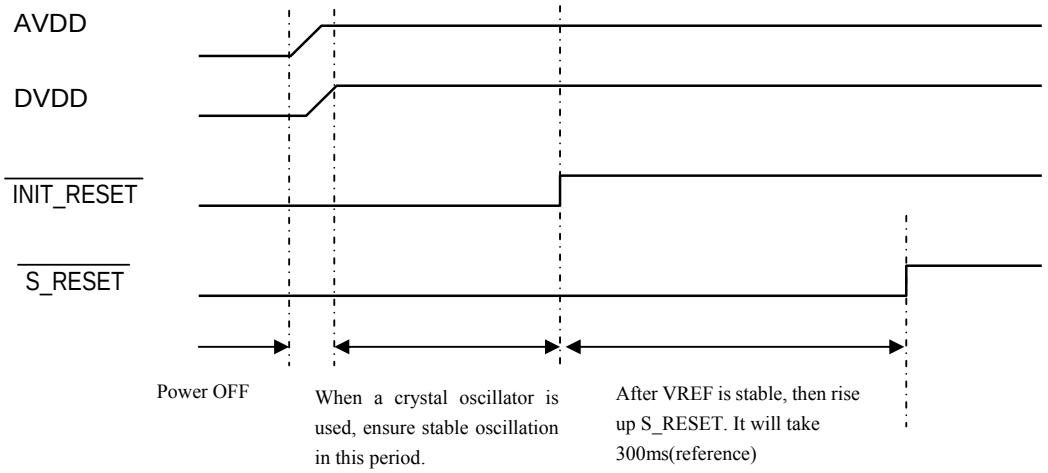


Fig. Power supply startup sequence

(4) Resetting

The AK7744 has two reset pins: $\overline{\text{INIT\_RESET}}$ and $\overline{\text{S\_RESET}}$.

The $\overline{\text{INIT\_RESET}}$ pin is used to set up VREF and initialize the AK7744, as shown in "Power supply startup sequence section 3)."

The system is reset when $\overline{\text{S\_RESET}}$ ="L". (Description of "reset" is for "system reset".)

During a system reset, a program write operation is normally performed (except for write operation during running).

During the system reset phase, the ADC and DAC sections are also reset. (The digital section of ADC output is MSB first 00000h and the analog section of DAC output is AVDD/2). However, VREF will be active, LRCLK and BITCLK in the master mode will be inactive

The system reset is released by setting $\overline{\text{S\_RESET}}$ to "H", whichl activates the internal counter. This counter generates LRCLK and BITCLK in the master mode: however, a problem may occur when a clock signal is generated. When the system reset is released in slave mode, internal timing will be actuated in synchronization with rising edge "↑" of LRCLK (when the standard input format is used). Timing between the external and internal clocks is adjusted at this time. If the phase difference in LRCLK and internal timing is within about -1/16 to 1/16 of the input sampling cycle (1/fs) during the operation, the operation is performed with internal timing remaining unchanged. If the phase difference exceeds the above range, the phase is adjusted by synchronizing the "↑" of LRCLK (when the standard input format is used). This prevents synchronization failure with the external circuit. For some time after returning to the normal state after loss of synchronization, normal data will not be valid. It should change the frequency of clock, SMODE or Analog input selector, while the system is in reset.

When $\overline{\text{S\_RESET}}$ is set to "H", the reset state is cancelled, and an internal DRAM clear is executed on the rising edge of LRCLK. It takes 8Fs (167usec at fs=48kHz) to clear the internal DRAM.

The ADC section can output 516-LRCLK after its internal counter has started. (The internal counter starts at the first rising edge of LRCLK in master mode. In slave mode, it starts 2 LRCLKs after the release of system reset.)

The AK7744 performs normal operation when $\overline{\text{S\_RESET}}$ is set to "H".

When $\overline{\text{INIT\_RESET}}$ or $\overline{\text{S\_RESET}}$ changes, the status of the DAC section also changes to Power down or Release mode, and it causes a click noise on the output. In this case, the SMUTE function is not effective; an external mute circuit is necessary to avoid any click noise.

(5) System clock

The required system clock is XTI (384fs/512fs), LRCLK (fs) and BITCLK (64 fs) in the slave mode, and is XTI (384 fs/512 fs) in the master mode. LRCLK corresponds to the standard digital audio rate (32 kHz, 44.1 kHz, and 48 kHz).

Fs	XTI(Master Clock)		BITCLK
	512fs	384fs	64fs
32.0kHz	16.3840MHz	12.2880MHz	2.0480MHz
44.1kHz	22.5792MHz	16.9344MHz	2.8224MHz
48.0kHz	24.576MHz	18.4320MHz	3.0720MHz

5-1) Master clock (XTI pin)

The master clock is obtained by connecting a crystal oscillator between the XTI pin and XTO pin or by inputting an external clock into the XTI pin while the XTO pin is left open.

5-2) Slave mode

The required system clock is XTI, LRCLK (1 fs) and BITCLK (48/64 fs).
The master clock (XTI) and LRCLK must be synchronized, but the phase is not critical.

5-3) Master mode

The required system clock is XTI (384fs/512fs). When the master clock (XTI) is input, LRCLK (1 fs) and BITCLK (64 fs) will be outputted from the internal counter synchronized with the XTI. LRCLK and BITCLK will not be active during initial reset ($\overline{\text{INIT\_RESET}}$ ="L") and system reset ($\overline{\text{S\_RESET}}$ ="L").

(6) Audio data interface (internal connection mode)

The serial audio data pins SDIN,SDINA1,SDINA2,SDOUT,SDOUTA1,SDOUTA2,SDOUTD1 and SDOUTD2 are interfaced with the external system, using LRCLK and BITCLK. The ports SDINA1, SDINA2, SDOUTA1, SDOUTA2, SDOUTD1 and SDOUTD2 are not normally used. These ports are controlled via registers. (See the block diagram on page.2 and the control register setting section at page 28.)

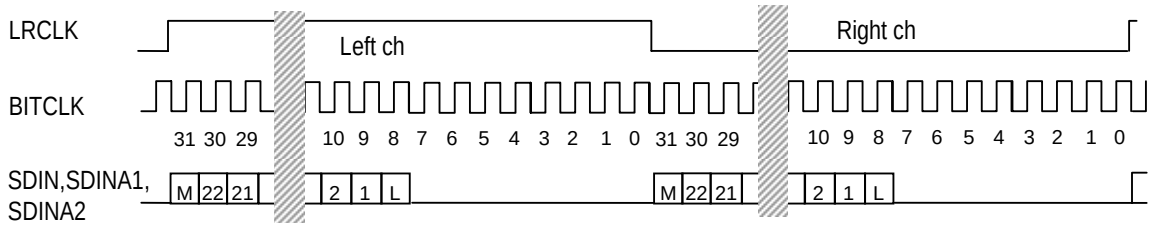
The data format is MSB-first 2's complement. Normally, the input/output format, in addition to the standard format used by AKM, can be changed to the I^2S compatible mode by setting the control register "CONT0 DIF (D5) to 1". (In this case, all input/output audio data pin interface are in the I^2S compatible mode.)

The input SDIN,SDINA1 and SDINA2 formats are MSB justified 24-bit at initialization. Setting the control registers CONT0: DIF1 (D4), DIF0(D3) will cause these ports to be compatible with LSB justified 24-bit, 20-bit and 16-bit. (SDINA is fixed at 24-bit MSB justified only.) (Note: CONT0 DIF(D5)=0). However, individual setting of SDIN, SDINA1 and SDINA2 is not allowed. The output SDOUT, SDOUTA1, SDOUTA2, SDOUTD1 and SDOUTD2 are fixed at 24-bit MSB justified only.

In slave mode BITCLK corresponds to not only 64fs but also 48fs. 64fs is the recommended mode. Following form ats describe 64fs examples.

6-1) Standard input format (DIF = 0: default set value)

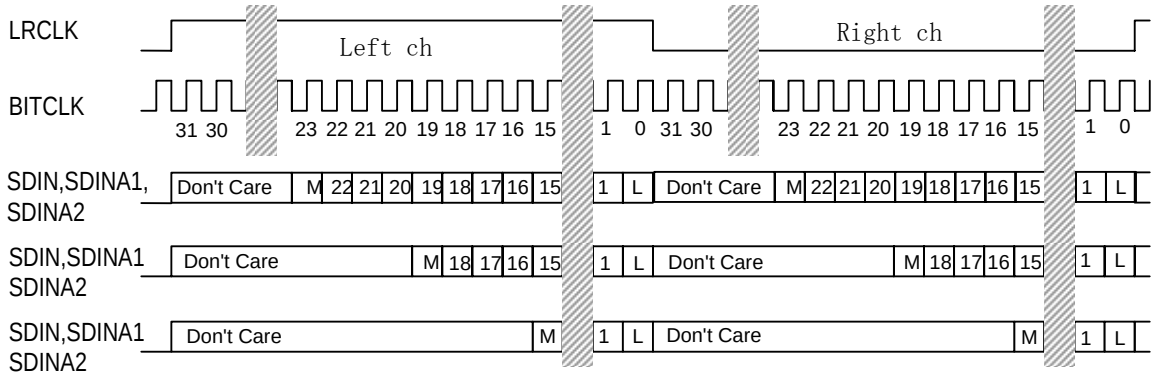
a) Mode 1 (DIF1, DIF0 = 0,0: default set value)



M : MSB, L : LSB

* When you want to input the MSB-justified 20-bit data into SDIN, SDINA input four "0" following the LSB.

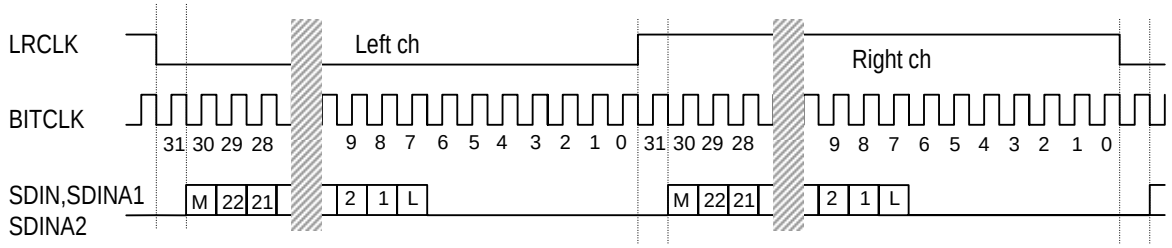
b) Mode 2, Mode 3, Mode 4



M : MSB, L : LSB

SDIN,SDINA1,SDINA2 Mode2 : (DIF1,DIF0)=(0,1) LSB justified 24-bit
SDIN,SDINA1,SDINA2 Mode3 : (DIF1,DIF0)=(1,0) LSB justified 20-bit
SDIN,SDINA1,SDINA2 Mode4 : (DIF1,DIF0)=(1,1) LSB justified 16-bit

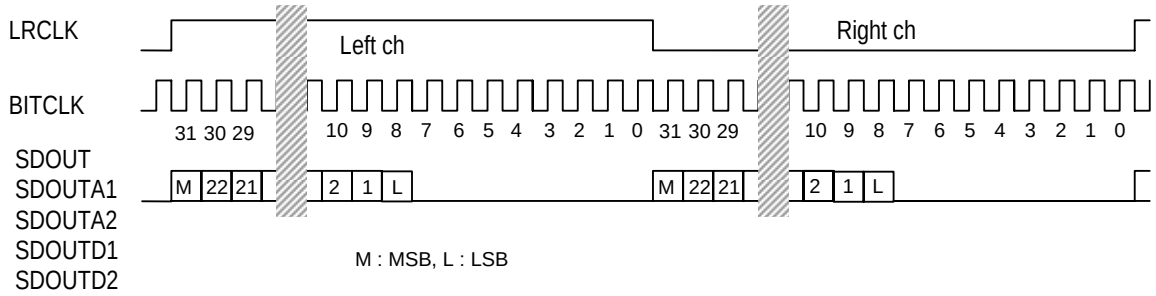
6-2) I²S compatible input format (DIF=1)



M : MSB, L : LSB

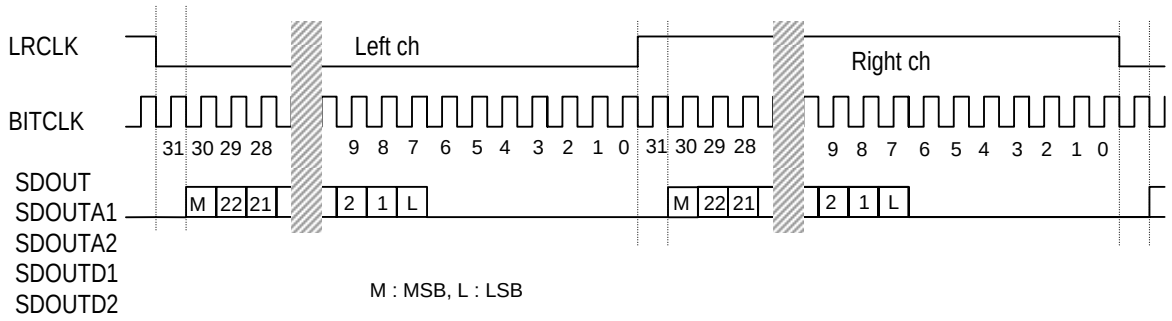
Mode 1: (DIF1(D4), DIF0(D3)) = (0, 0) must be set.

6-3) Standard output format (DIF=0: default set value)



M : MSB, L : LSB

6-4) I²S compatible output format (DIF=1)



M : MSB, L : LSB

(7) Interface with microcomputer

The microcomputer interface uses 6 control pins; $\overline{RQ}$ (ReQuest Bar), SCLK (Serial data input Clock), SI (Serial data Input), SO (Serial data Output), RDY (ReaDY) and DRDY (Data ReaDY).

In the AK7744, two types of operations are provided; writing and reading during the reset phase (namely, system reset) and R/W during the run phase.

During the reset phase, writing of the control register, program RAM, coefficient RAM, offset RAM, external conditional jump code, and reading of the program RAM, coefficient RAM and offset RAM, are enabled.

During the run phase, writing of coefficient RAM, offset RAM and external conditional jump code, and reading of data on the DBUS (data bus) from the SO, are enabled. Its data is MSB first serial I/O.

When the AK7744 needs to transfer data to the microcomputer, it starts by $\overline{RQ}$ going "L" expects reading of data on the DBUS. The AK7744 reads SI data at the rising point of SCLK, and outputs to SO at the falling point of SCLK. The AK7744 accepts first data as command then address data or some kinds of data input / output starts.

When $\overline{RQ}$ changes to "H", one command has finished. New command requests must set $\overline{RQ}$ to "L" again. For DBUS data reads, leave $\overline{RQ}$ ="H". (It does not need command code input.)

When it needs to clear the output buffer (MICR), the SI pin uses for control. (In this case, it is necessary to protect against a noise as SCLK.)

Command code table is as follow.

Command code list

Conditions for use	Code name	Command code		Remark:
		WRITE	READ	
RESET phase	CONT0	60h	70h	For the function of each bit, See the description of Control Registers.
	CONT1	64h	74h	
	CONT2	68h	78h	
	CONT3	6Ch	7Ch	
	PRAM	C0h	C1h	
	CRAM	A0h	A1h	
	OFRAM	90h	91h	
	External condition jump	C4h	-	
	CRC check (R(x))	B6h	D6h	
RUN phase	CRAM rewrite preparation	A8h	-	It needs to do before CRAM rewrite
	CRAM rewrite	A4h	-	
	OFRAM rewrite preparation	98h	-	It needs to do before OFRAM rewrite
	OFRAM rewrite	94h	-	
	External condition jump	C4h	-	Same code as RESET
	CRC check (R(x))	B6h	D6h	Same code as RESET

NOTE: Do not send other than the above command codes. Otherwise an operation error may occur.
If there is no communication with the microcomputer, set the SCLK to "H" and the SI to "L" for use.

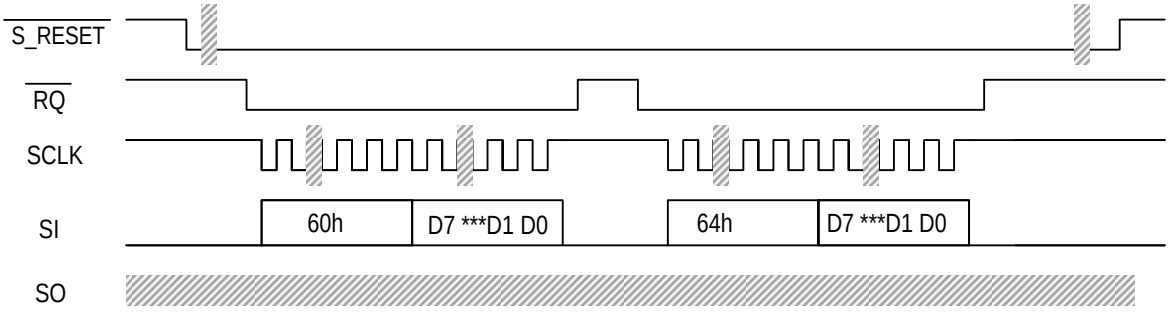
7-1) Write during reset phase

7-1-a) Control register write (during reset phase)

The data comprises a set of 2 bytes used to perform control register write operations (during reset phase). When all data has been entered, the new data is sent at the rising edge of the 16th count of SCLK.

Data transfer procedure	
① Command code	60h,64h,68h,6Ch
② Control data	(D7 D6 D5 D4 D3 D2 D1 D0)

For the function of each bit, see the description of Control registers, (section 2).



Note) It must be set always 0 to D0.

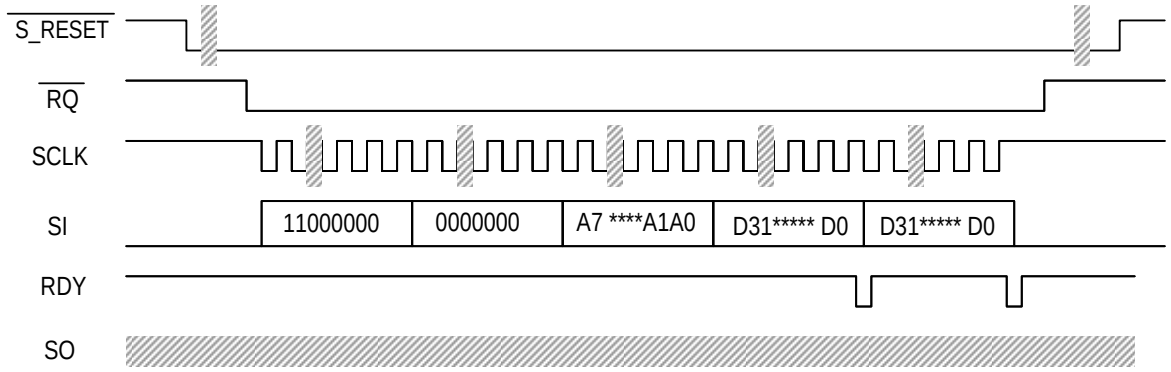
Control Registers write operation

7-1-b) Program RAM writes (during reset phase)

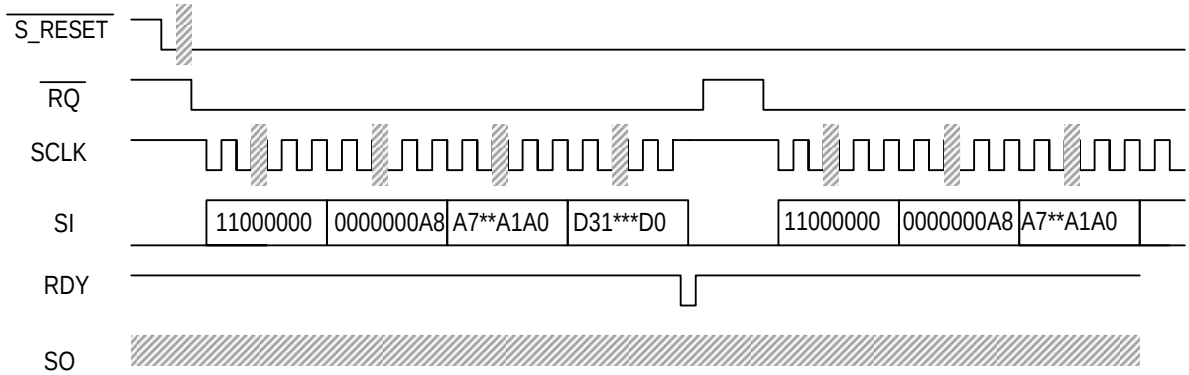
Program RAM write operations are performed during the reset phase using 7-bytes of data. When all data have been transferred, the RDY terminal is set to "L". Upon completion of writing into the PRAM, RDY returns "H" to allow the next data bit input. When writing to sequential addresses, input the data without a command code or address. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" again and then input the command code, address and data in that order.

Data transfer procedure

① Command code	C0h (1 1 0 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 0 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D31 . . . . . D24)
⑤ Data	(D23 . . . . . D16)
⑥ Data	(D15 . . . . . D8)
⑦ Data	(D7 . . . . . D0)



Input of continuous address data into PRAM



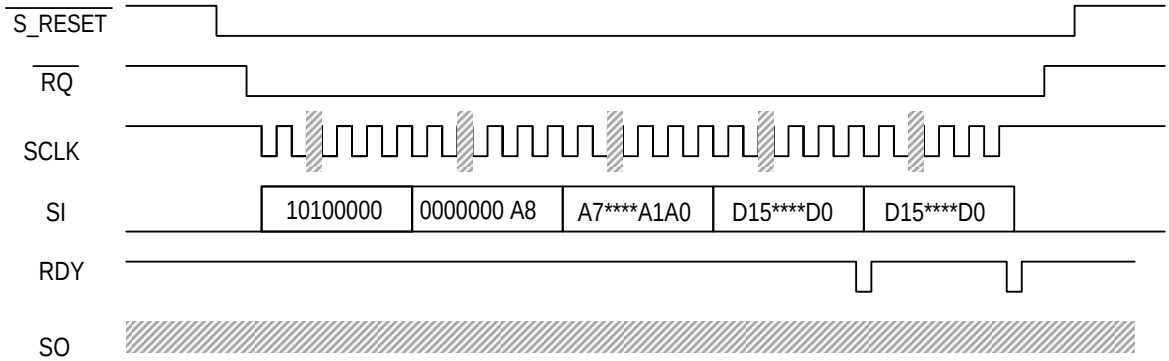
Input of discontinuous address data into PRAM

7-1-c) Coefficient RAM write (during reset phase)

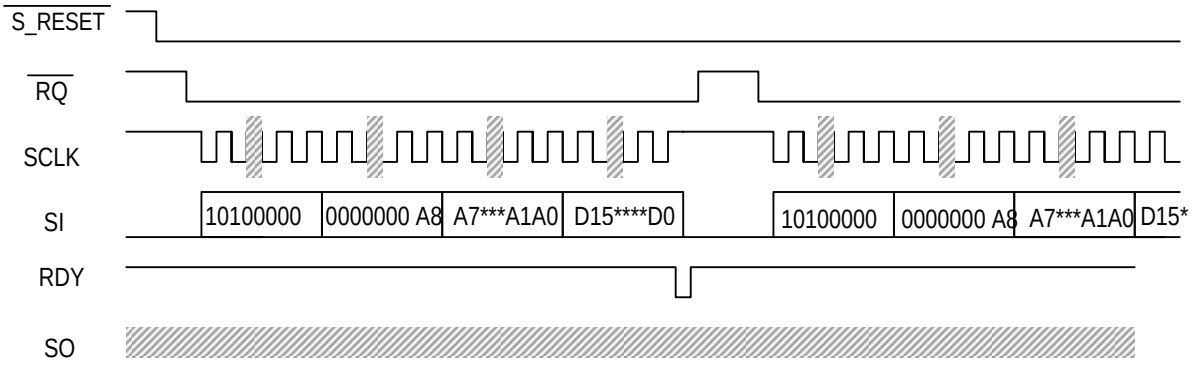
5 bytes of data are used to perform coefficient RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the CRAM, it goes to "H" to allow the next data to be input. When writing to sequential addresses, input the data as shown below. To write discontinuous data, transition the $\overline{RQ}$ terminal from "H" to "L" and then input the command code, address and data.

Data transfer procedure

① Command code	A0h (1 0 1 0 0 0 0 0)
② Address upper	(0 0 0 0 0 0 0 A8)
③ Address lower	(A7 . . . . . A0)
④ Data	(D15 . . . . . D8)
⑤ Data	(D7 . . . . . D0)



Input of continuous address data into CRAM



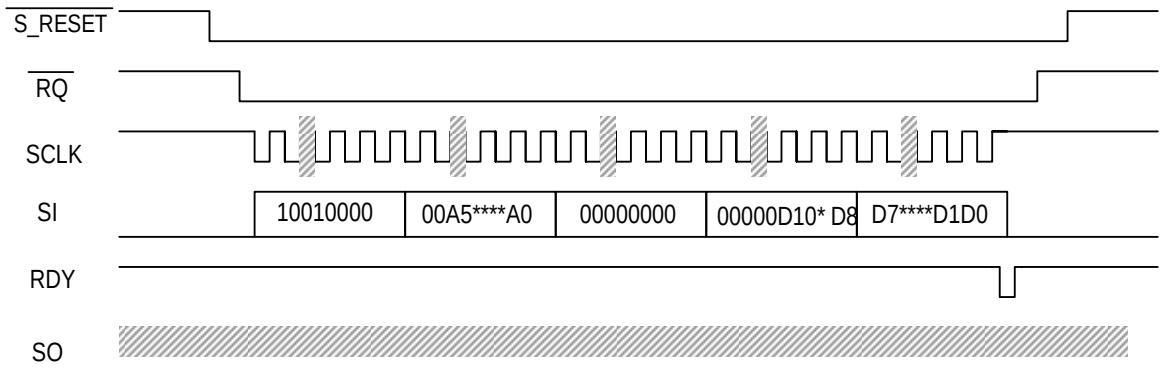
Input of discontinuous address data into CRAM

7-1-d) Offset RAM write (during reset phase)

5 bytes of data are used to perform offset RAM write operations (during reset phase). When all data has been transferred, the RDY terminal goes to "H". Upon completion of writing into the OFRAM, it goes to "H" to allow the next data to be input. When writing to sequential addresses, input the data without a command code or address. To write discontinuous data, shift the $\overline{RQ}$ terminal from "H" to "L" and then input the command code, address and data in that order.

Data transfer procedure

① Command code	90h (1 0 0 1 0 0 0 0)
② Address	(0 0 A5 A4 .. . . A0)
③ Data	(0 0 0 0 0 0 0 0)
④ Data	(0 0 0 D12 D11 * * . D8)
⑤ Data	(D7 . . . . . D0)

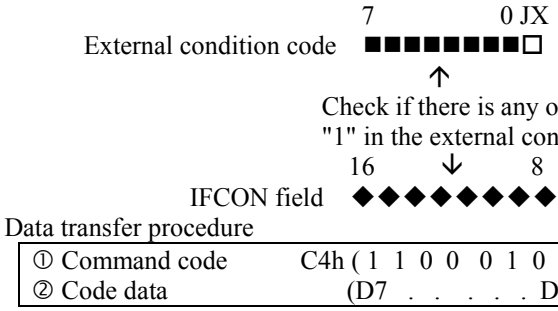


Input of data into OFRAM

7-1-e) External conditional jump code write (during reset phase)

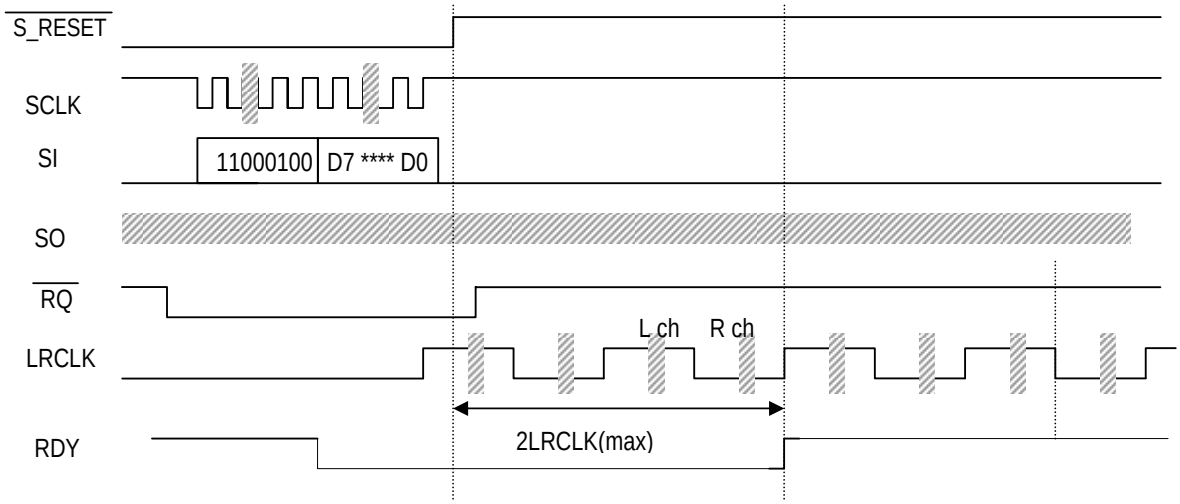
Two bytes of data are used to perform offset is external conditional jump operations. The data can be entered during both the reset and operation phases, and the input data are set to the specified register at the leading edge of the LRCLK. When all data bits have been transferred, the RDY terminal goes to "L". Upon write completion, it goes to "H". A jump command will be executed if there is any one agreement between "1" of each bit of external condition code 8 bits (soft set) plus 1 bit (hard set) at the external input terminal JX and "1" of each bit of the IFCON field. The data during the reset phase can be written only before release of the reset, after all data has been transferred. $\overline{RQ}$ Transition from "L" to "H" in the write operation during the reset phase must be executed after three LRCLK in the slave mode or one LRCLK in master mode, respectively, from the trailing edge of the LRCLK after release of the reset. Then the RDY goes to "H" after capturing the rise of the next LRCLK. A write operation from the microcomputer is disabled until the RDY goes to "H". The IFCON field provides external conditions written on the program. It resets to 00h by $\overline{INIT\_RESET}$ ="L", however, it remains previous condition even $\overline{S\_RESET}$ ="L".

Note: It should be noted that the LRCLK phase is inverted in the I2S-compatible state.



Data transfer procedure

① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



Timing for external conditional jump write operation (during reset phase)

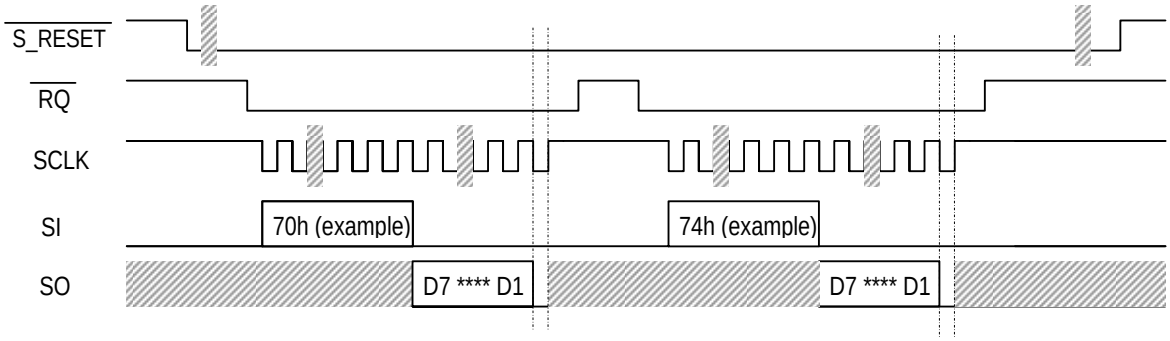
7-2) Read during reset phase

7-2-a) Control register data read (during reset phase)

To read data written into the control registers, input the command code and 16 bits of SCLK. After the input command code, the data of D7 to D1 outputs from SO is synchronized with the falling edge of SCLK. D0 is invalid, so please ignore this bit.

Data transfer procedure

① Command code 70h,74h,78h,7Ch



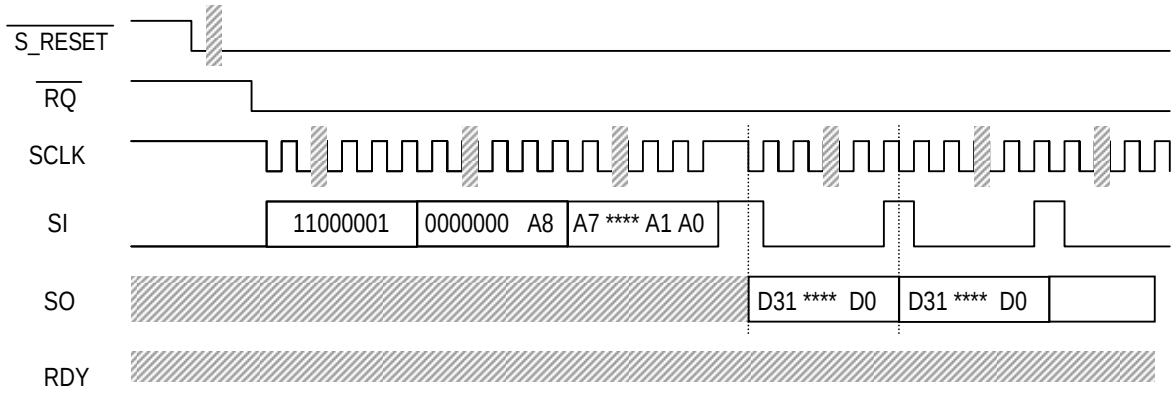
Reading of Control Register data

7-2-b) Program RAM read (during reset phase)

To read data written into PRAM, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". The data is then clocked out from SO in synchronization with the falling edge of SCLK. (Ignore the RDY operation that will occur in this case.)
If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

①Command code input C1h (1 1 0 0 0 0 0 1)
②Read address input MSB (0 0 0 0 0 0 0 A8)
③Read address input LSB (A7 . . . . A0)



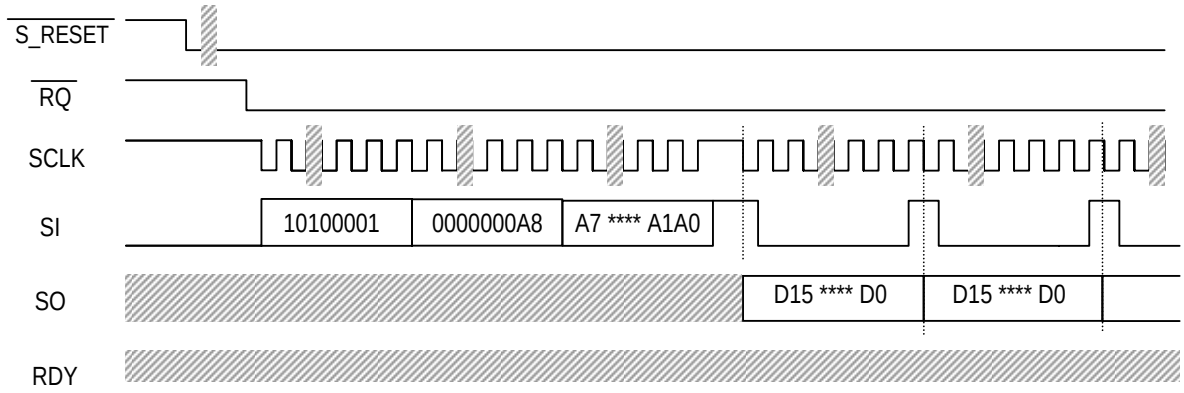
Reading of PRAM data

7-2-c) CRAM data read (during reset phase)

To read out the written coefficient data, input the command code and the address you want to read out. After that, set SI to "H" and SCLK to "L". The data is clocked out from SO in synchronization with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

① Command code A1h	(1 0 1 0 0 0 0 1)
② Address upper	(0 . . . . . A8)
③ Address lower	(A7 . . . . . A0)



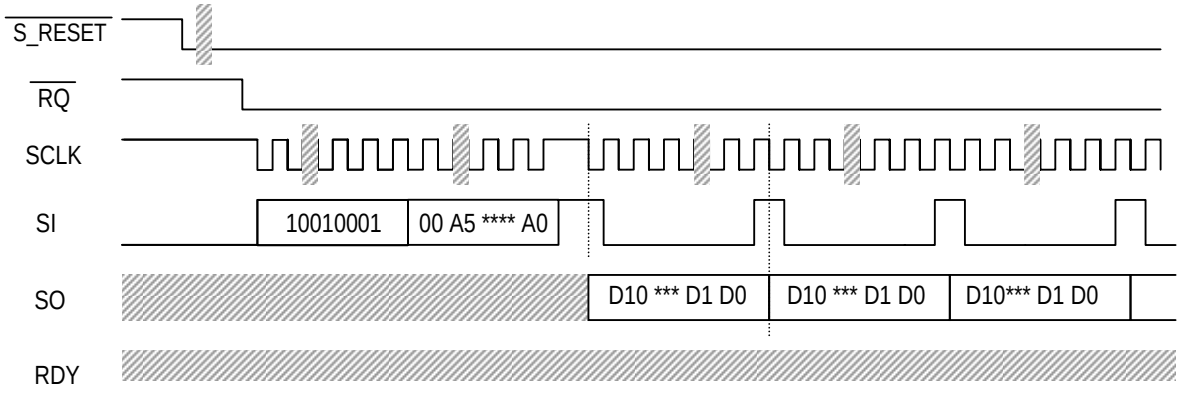
Reading of CRAM data

7-2-d) OFRAM data read (during reset phase)

The written offset data can be read out during the reset phase. To read it, input the command code and the address you want to read. After that, set SI to "H" and SCLK to "L". This completes preparation for outputting the data. Then set SI to "L", and the data is clocked out in synchronization with the falling edge of SCLK. If there are continuous addresses to be read, repeat the above procedure starting from the step where SI is set to "H".

Data transfer procedure

① Command code	91h (1 0 0 0 1 0 0 0 1)
② Address	(0 0 A5 . . . . A0)



Reading of OFRAM data

7-3) Write during RUN phase

7-3-a) CRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite CRAM (coefficient RAM) during program execution. After inputting the command code, you can input a maximum of 16 data bytes of a continuous address you want to rewrite, then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

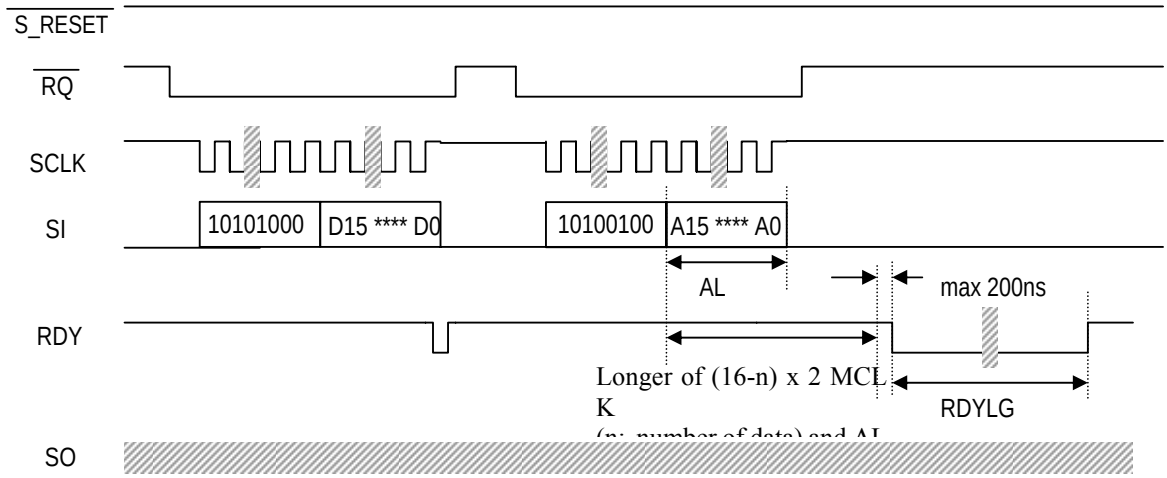
Coefficient RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	A8h	(1 0 1 0 1 0 0 0)
	② Data		(D15 . . . . D8)
	③ Data		(D7 . . . . . D0)
* Rewrite	① Command code	A4h	(1 0 1 0 0 1 0 0)
	② Address upper		(0 0 0 0 0 0 0 A8)
	③ Address lower		(A7 . . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one

CRAM rewriting preparation and writing

7-3-b) OFRAM rewrite preparation and write (during RUN phase)

This function is used to rewrite OFRAM (offset RAM) during program execution. After inputting the command code, you can input a maximum of 16 data bytes of a continuous address you want to rewrite.
Then input the write command code and rewrite the leading address. Every time the RAM address to be rewritten is specified, the contents of RAM are rewritten. The following is an example to show how five data bytes from address "10" of the coefficient RAM are rewritten:

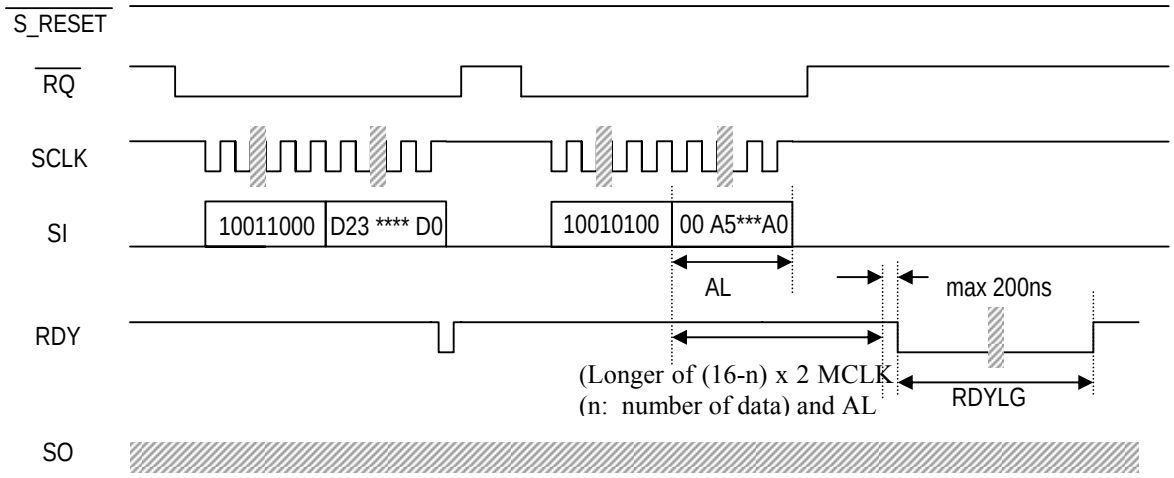
Offset RAM execution address 7 8 9 10 11 13 16 11 12 13 14 15

Rewrite position ↓ ↓ ↑ ↓ ↓ ↓

Note that address "13" is not executed until address "12" is rewritten.

Data transfer procedure

* Preparation for rewrite	① Command code	98h (1 0 0 0 1 1 0 0 0)
	② Data	(D23 . . . . . D16)
	③ Data	(D15 . . . . . D8)
	④ Data	(D7 . . . . . D0)
* Rewrite	① Command code	94h (1 0 0 0 1 0 1 0 0)
	② Address	(0 0 A5A4 . . . A0)



Note: The RDY signal will go to high within the maximum of two LRCLKs if the RDYLG width is programmed to ensure a new address to be rewritten within one sampling cycle.

OFRAM rewriting preparation and writing

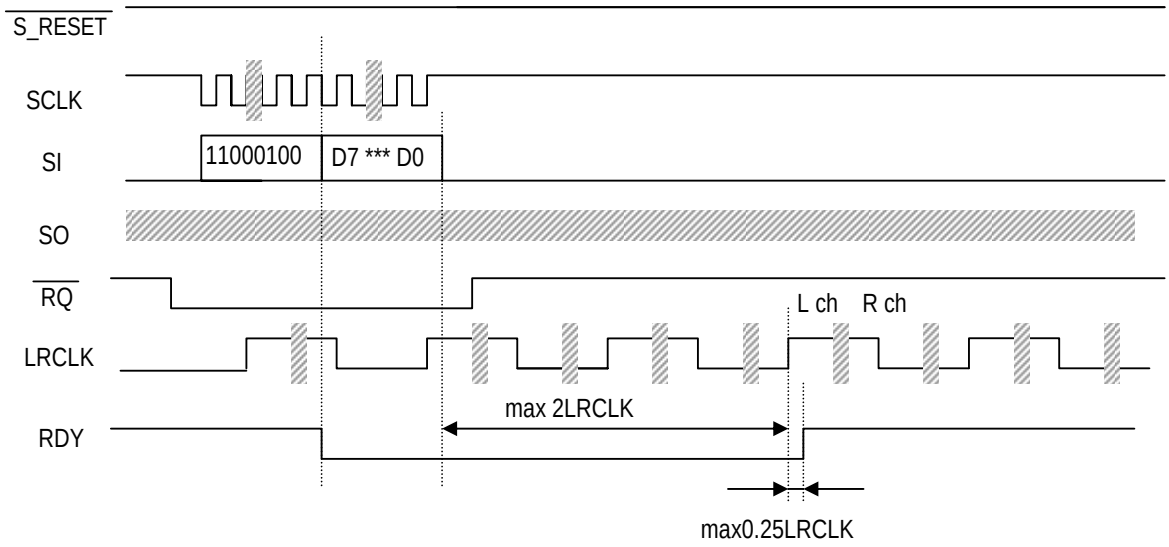
7-3-c) External conditional jump code rewrite (during RUN phase)

Two data bytes are used to write an external conditional jump code. Data can be input during both the reset and operation phases, and input data is set to the specified register at the rising edge of LRCLK. When all data has been transferred, the RDY terminal goes to "L". Upon completion of writing, it goes to "H". A jump command will be executed if there is any one agreement between each bit of the 8-bit external condition code and "1"of each bit of the IFCON field. A write operation from the microcomputer is disabled until RDY goes to "H".

Note: The LRCLK phase is inverted in the I2S-compatible state.

Data transfer procedure

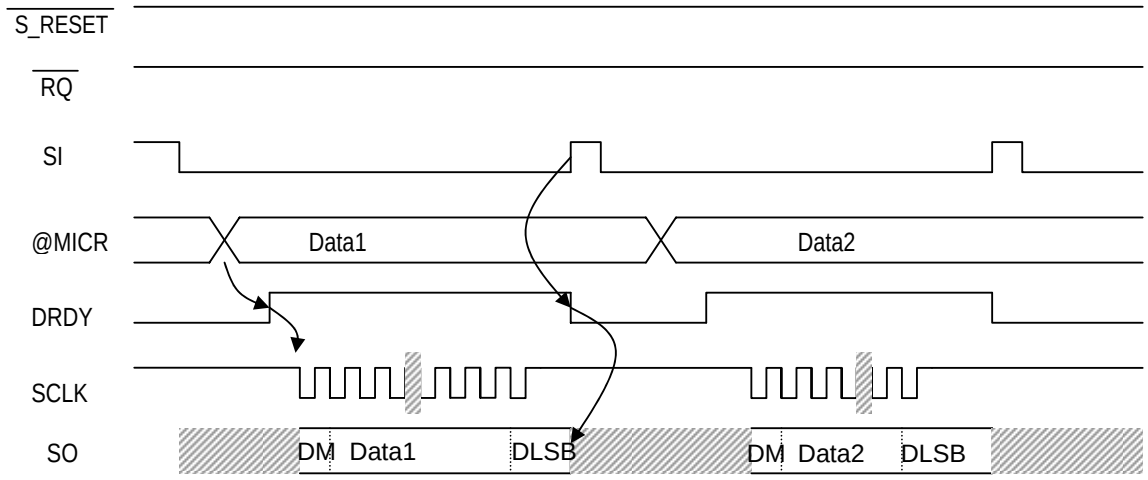
① Command code	C4h (1 1 0 0 0 1 0 0)
② Code data	(D7 . . . . . D0)



External condition jump write timing (during RUN phase)

7-4) Read-out during RUN phase (SO output)

SO outputs data on DBUS (data bus) of the DSP section. Data is set when @MICR the DST field specifies. Setting of data allows DRDY to go to "H", and data is output synchronized with the falling edge of SCLK. When SI goes to "H", DRDY goes to "L" to wait for the next command. Once DRDY goes to "H", the data of the last @MICR command immediately before DRDY goes to "H" will be held until SI goes to "H", and subsequent commands will be rejected. A maximum of 24 bits are output from SO. After the required number of data (not exceeding 24 bits) is taken out by SCLK, setting SI to “H” can output the next data.



SO read (during RUN phase)

(8) ADC section high-pass filter

The AK7744 incorporates a digital high-pass filter (HPF) for canceling DC offset in the ADC. The HPF cut-off frequency is about 1 Hz (fs = 48 kHz). This cut-off frequency is proportional to the sampling frequency (fs).

	48kHz	44.1kHz	32kHz
Cut-off frequency	0.93Hz	0.86Hz	0.62Hz

5) Simple error check for communication

The AK7744 has a simple CRC error check function.

(Note: Its main purpose is checking against the noise effects during ata writes from microprocessor to the AK7744. **This check CANNOT guarantee 100% error detection** on the AK7744, because this CRC (cyclic redundancy check) is before writing internal AK7744's RAM or its register.

Explanation:

* Serial data(X): Input SI data from $\overline{RQ}$ fall to rise up.
* Generator polynomial G(x) =$x^{16}+x^{12}+x^5+1$ (X.25 of CCITT standard order of hexadecimal is 11021h).
* The rest of D(x) divides by G(x) is R(x).
  This division is using exclusive-or instead of subtraction during this calculation.
  It makes good 16-bit zero data after translated serial data D(X) and the rest R(X) of this division comes out 16bit data.

In order to do simple error check is as following:

1) Use the command code B6h and write the R(x) (the rest result of serial data D(x) divided by G(x)).
2) Then use the command code D6h and read out R(x) to check whether the R(x) is correct or not. (Unless this read out, CRC check itself works.)
3) If the result of the rest D(x) divided by G(x) is equal to R(x), SO outputs "H" from the next rising edge of $\overline{RQ}$ to falling edge of $\overline{RQ}$. (However, SO read out from micro-controller is prior to this signal. Refrain from a runtime read out while doing CRC check.) If R(x) is not equal to the result, it outputs "L".
4) If you want to check other serial data, then repeat action form 1) to 3).

Note) In the case of detecting CRC error in runtime "CRAM rewrite" (A4h) or "OFRAM rewrite"(94h), the possibility of writing data to the wrong address exists.

* Specific order of data translates.

1) Write the register

The rest R(x) data writing is using 3-byte/unit (24bit)

Data translate order.

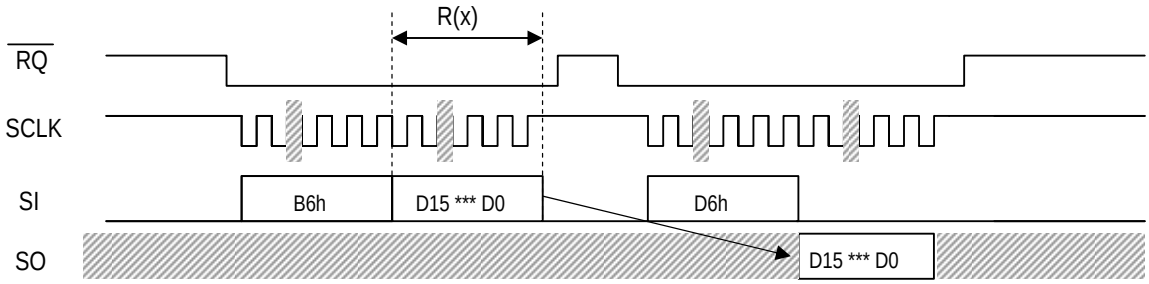
①Command code B6h
②Upper 8bit of R(x) (D15 * * * * * * D8)
③Lower 8bit of R(x) (D7 * * * * * * D0)

2) Read out the register

The rest R(x) data reading out is 3-byte/unit (24bit)

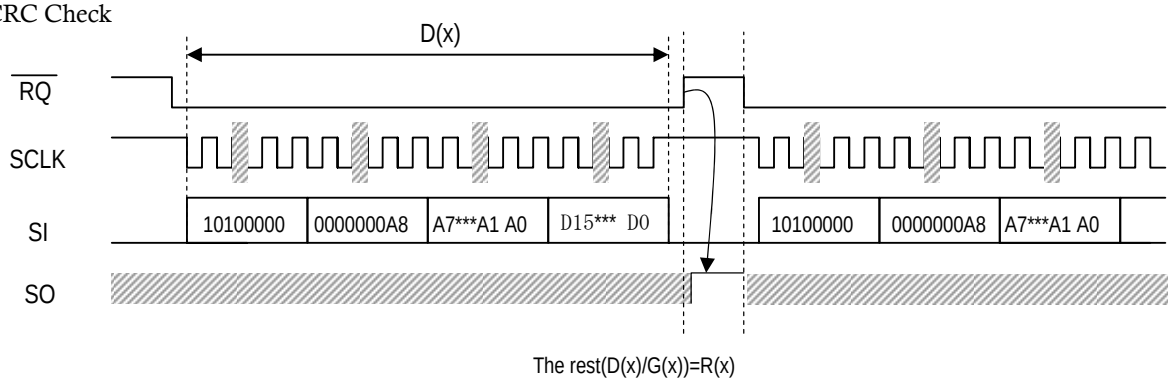
Data translate order

①Command code D6h
②Upper 8bit of R(x) (D15 * * * * * * D8)
③Lower 8bit of R(x) (D7 * * * * * * D0)



Example: Control register writing, reading

3) CRC Check



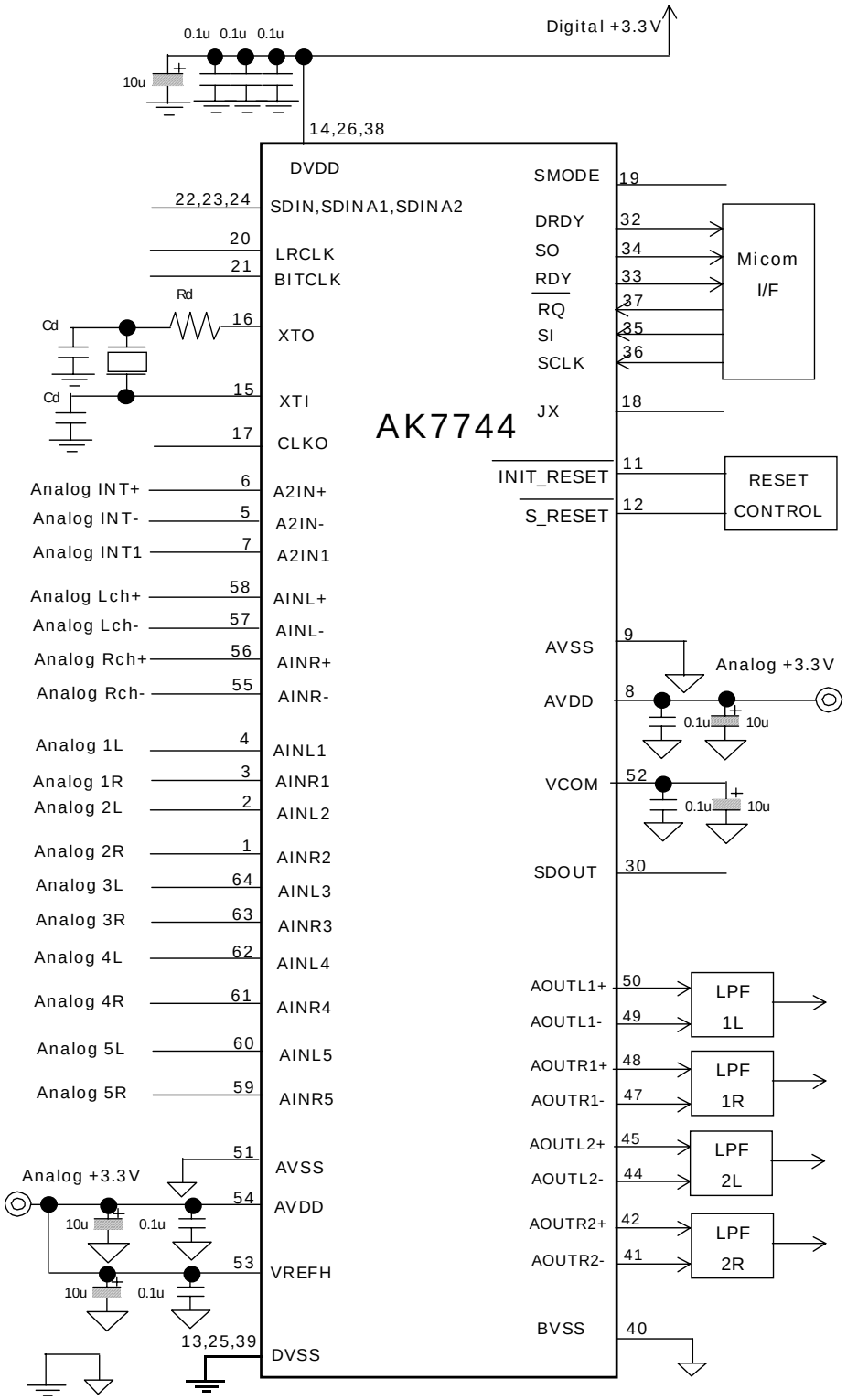
The rest of D(x)/G(x)=R(x) CRC Check example.

4) Example of the R(x) made from D(x).

Examples	D(X)	R(X)
1	D6ABCDh	1E51h
2	D2A5A5h	0C30h
3	A855557777AAAA0000FFFFh	2297h

9. System Design

(1) Connection example



(2) Peripheral circuit

1) Ground and power supply

A To minimize digital noise coupling, AVDD and DVDD should be individually de-coupled at the AK7744. System analog power is supplied to AVDD. Generally, the power supply and ground wires must be connected separately for the analog and digital sections. Connect them at a position close to the power source on the PC board. Decoupling capacitors and small ceramic capacitors should be connected as close as possible to the AK7744

2) Reference voltage

The input voltage difference between the VREFH pin and the AVSS pin determines the full scale of analog input, while the potential difference between the VREFH pin and the AVSS pin determines the full scale of the analog output. Normally, connect AVDD to VREFH, and connect 0.1μF ceramic capacitors from them to AVSS. To shut out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor in particular should be connected as close as possible to the pin. To avoid coupling to the AK7744, digital signals and clock signals should be kept away as far as possible from the VREFH pin.

VCOM is used as the common voltage of the analog signal.To shut out high frequency noise, connect a 0.1μF ceramic capacitor in parallel with an appropriate 10μF electrolytic capacitor between this pin and AVSS. The ceramic capacitor should be connected as close as possible to the pin. Do not lead current from the VCOM pin.

3) Analog input

Analog input signals are applied to the modulator through the differential input pins or single-ended pins of each channel selected by the input selector. When using the differential inputs, this voltage is equal to the differential voltage between AIN+ and AIN- (ΔVAIN=(AIN+)-(AIN-)), and the input range is ±FS= ±(VREFH-AVSS)×(2.0/3.3). When VREFH = 3.3V and AVSS = 0V, the input range is within ±2.0Vpp. When using single-ended inputs, this input range is FS = (VREFH-AVSS)×(2.0/3.3). When VREFH = 3.3V and AVSS = 0V, the input range is within 2.0Vpp the output code format is given in terms of 2's complements.

The analog source voltage to the AK7744 is +3.3V(Typ.). Voltage of AVDD+0.3V or more, voltage of AVSS-0.3V or less, and current of 10 mA or more must not be applied to analog input pins (AINL+,AINL-,AINR+,AINR-,AINL1,AINR1,AINL2,AINR2,AINL3,AINR3,AINL4,AINR4,AINL5,AINR5,

A2IN+,A2IN-,A2IN1,VREFH) Excessive current will damage the internal protection circuit and will cause latch-up, thereby damaging the IC. Accordingly, if the surrounding analog circuit voltage is ±15 V, the analog input pins must be protected from high-voltage signals.

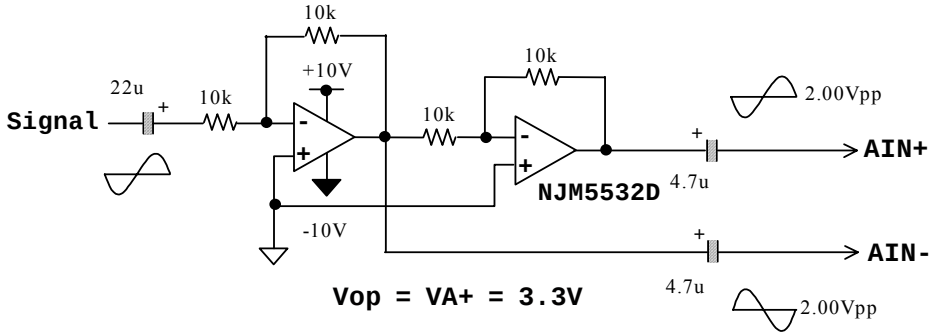


Fig. 1 Example of input buffer circuit (differential input)

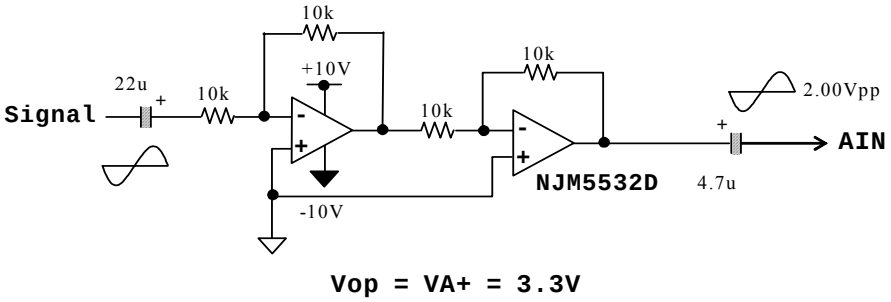


Fig. 2 Example of input buffer circuit (single ended input)

An analog signal can be applied to the AK7744 is single ended mode. In this case, apply the analog signal (the full scale is 2.0Vpp when the internal reference voltage is used). However, use of a low saturated operational a mplifier is recommended if the operational amplifier is driven by the 3.3-volt power supply.

4) Analog output

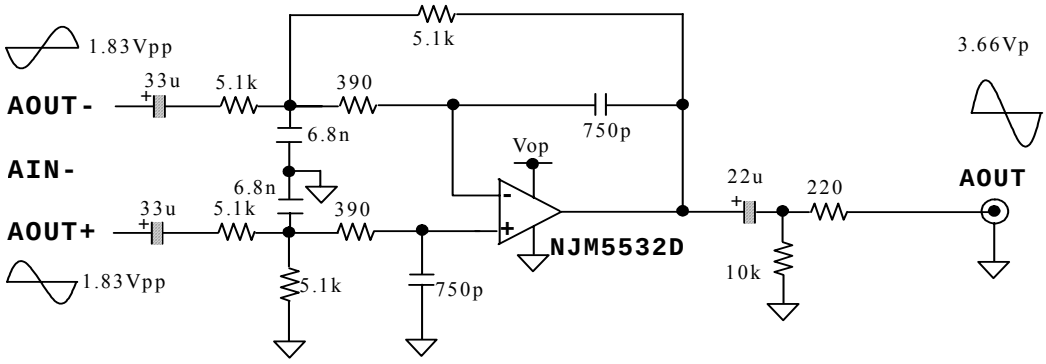


Fig.3 Example of output LPF circuit

The analog outputs are full differential outputs and nominally ±1.83Vpp (typ @ VRDAH=3.3V) centered in the internal common voltage about (AVDD/2). The differential outputs are summed externally, VAOUT=(AOUT+)-(AOUT-) between AOUT+ and AOUT-.
If the summing gain is 1, the output range is VAOUT = 3.66Vpp(typ@ VRDAH=3.3V). The bias voltage of external summing circuit is supplied externally.
The input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal AOUT is 0V for 000000H(@24bit).

The internal switched-capacitor filter and external LPF attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

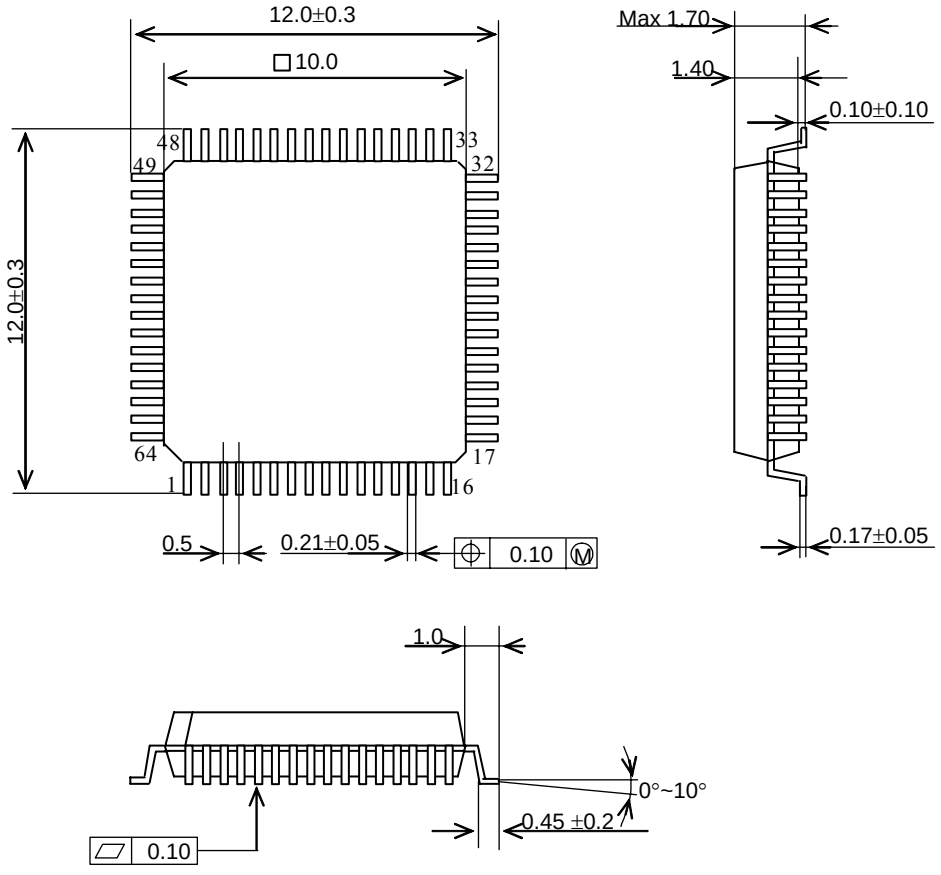
Differential outputs can eliminate few mV+AVDD/2 DC offset on analog outputs with capacitors.
Fig.3 shows the example of external op-amp circuit summing the differential outputs.

5) Connection to digital circuit

To minimize the noise resulting from the digital circuit, connect low voltage logic to the digital output. The applicable logic family includes the 74LV, 74LV-A, 74ALVC and 74AVC series.

10. Package

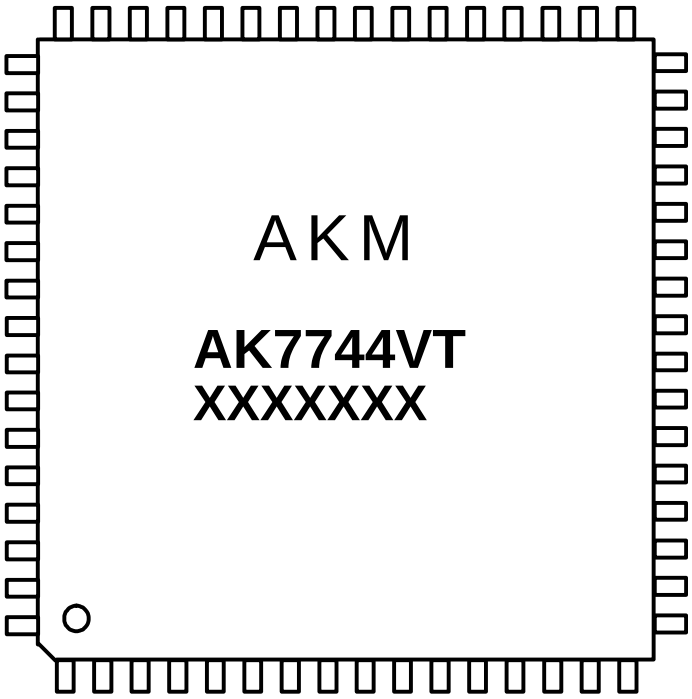
- 64pin LQFP (Unit : mm)



- Material & Lead finish

Package:	Epoxy
Lead-frame:	Copper
Lead-finish	Soldering (Not include lead) plate

11. Marking



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK7744VT
4) Asahi Kasei Logo