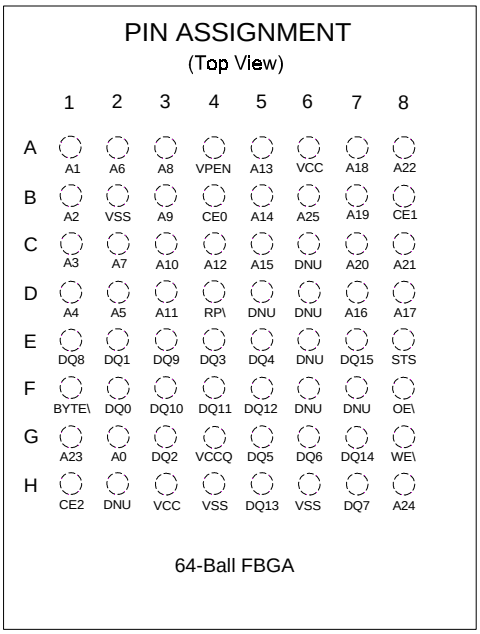
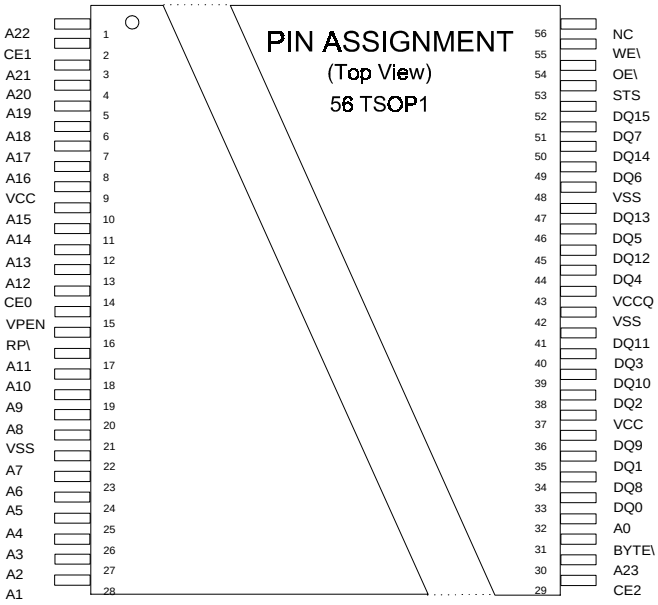
Plastic Encapsulated Microcircuit
128Mb, x8 and x16 Q-FLASH Memory
Even Sectored, Single Bit per Cell Architecture



Features

- 100% Pin and Function compatible to Intel's MLC Family
- NOR Cell Architecture
- 2.7V to 3.6V VCC
- 2.7V to 3.6V or 5V VPEN (Programming Voltage)
- Asynchronous Page Mode Reads
- Manufacturer's ID Code:
  - ✓ MT28F128J3MRG Micron 0x2Ch
- Industry Standard Pin-Out
- Fully compatible TTL Input and Outputs
- Common Flash Interface [CFI]
- Scalable Command Set
- Automatic WRITE and ERASE Algorithms
- 5.6us per Byte effective programming time
- 128 bit protection register
  - ✓ 64-bit unique device identifier
  - ✓ 64-bit user programmable OTP cells
- Enhanced data protection feature with use of VPEN=VSS
- Security OTP block feature
- 100,000 ERASE cycles per BLOCK
- Automatic Suspend Options:
  - ✓ Block ERASE SUSPEND-to-READ
  - ✓ Block ERASE SUSPEND-to-PROGRAM
  - ✓ PROGRAM SUSPEND-to-READ
- Available Operating Ranges:
  - ✓ Enhanced [-**ET**] -40°C to +105°C
  - ✓ Mil-Temperature [-**XT**] -55°C to +125°C



For in-depth functional product detail and Timing Diagrams, please reference Micron's full product Datasheet:

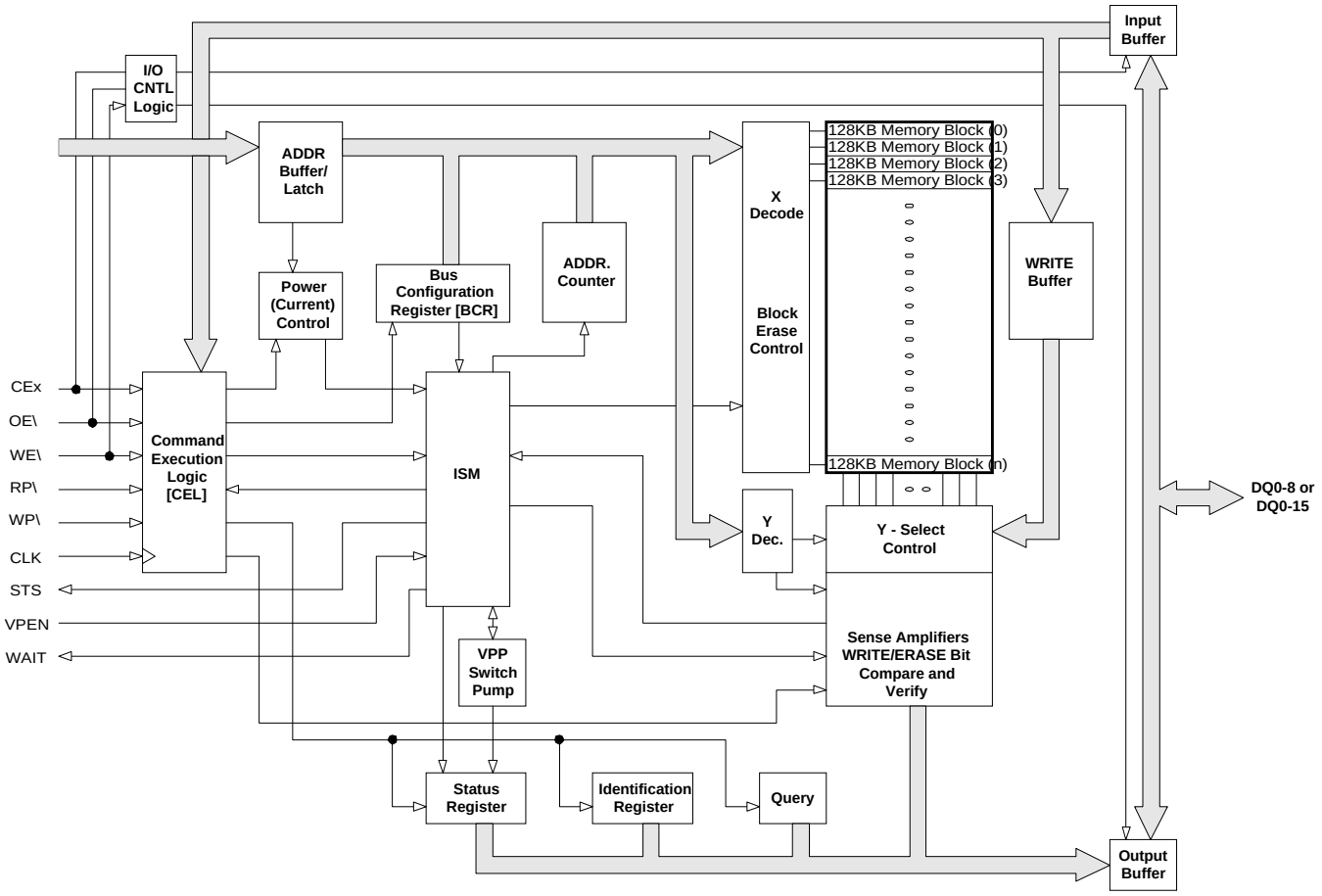
MT28F640J3 Rev. L Dated 04/16/04

General Description

ASI's, AS28F128J3M Enhanced or Mil-Temp variant of Micron's Q-Flash family of devices, is a nonvolatile, electrically block-erasable (FLASH), programmable memory device manufactured using Micron's 0.15um process technology. This device containing 134,217,728 bits organized as either 16,777,218 (x8) or 8,388,608 bytes (x16). The device is uniformly sectored with one hundred and twenty eight 128KB ERASE blocks.

This device features in-system block locking. They also have a Common FLASH Interface [CFI] that permits software algorithms to be used for entire families of devices. The software is device-independent, JEDEC ID-independent with forward and backward compatibility.

Functional Block Diagram:



Additionally, the Scaleable Command Set [SCS] allows a single, simple software driver in all host systems to work with all SCS compliant FLASH memory devices. The SCS provides the fastest system/device data transfer rates and minimizes the device and system-level implementation costs.

To optimize the processor-memory interface, the device accommodates VPEN, which is switchable during BLOCK ERASE, PROGRAM, or LOCK BIT configurations and in addition can be hard-wired to VCC all dependent on the end application(s). VPEN is treated as an input pin to enable ERASING, PROGRAMMING, and BLOCK LOCKING. When VPEN is lower than the VCC lockout voltage (VLKO), all program functions are disabled. BLOCK ERASE SUSPEND mode enables the user to stop BLOCK ERASE to READ data from or PROGRAM data to any other blocks. Similarly, PROGRAM SUSPEND mode enables the user to SUSPEND PROGRAMMING to READ data or execute code from any un-suspended block(s).

VPEN serves as an input with 2.7V, 3.3V or 5V levels for application programming. VPEN in this Q-Flash device can provide data protection when connected to ground. This pin also enables PROGRAM or ERASE LOCKOUT functions/controls during power transitions.

This device is an even-sectored device architecture offering individual BLOCK LOCKING that can LOCK and UN-LOCK a block using the SECTOR LOCK BITS command sequence.

Status [STS] is a logic signal output that gives an additional indicator of the internal state machine [ISM] activity by providing a hardware signal of both the status and status masking. This status indicator minimizes central processing unit overhead and system power consumption. In the default mode, STS acts as an RY/BY\ pin. When LOW, STS indicates that the ISM is performing a BLOCK ERASE, PROGRAM, or LOCK BIT configuration. When HIGH, STS indicates that the ISM is ready for a new command.

Three Chip Enable (CEx) pins are used for enabling and disabling the device by activating the device's control logic, input buffer, decoders, and sense amplifiers.

BYTE\ enables the device to be used in x8 or x16 configuration. Byte=Low (logic 0) selects and 8-bit mode with address zero (A0) selecting the High or Low Byte and Byte=High (logic 1) selects the 16-bit or Word mode. When the device is in Word mode, address one (A1) becomes the low order address bit and address zero (A0) becomes a no-connect (NC).

RP\ is used to reset the device. When the device is disabled and RP\ is at VCC, the STANDBY mode is enabled. A reset time (tRWH) is required after RP\ switches to a High (logic 1) and the outputs become valid. Likewise, the device has a wake time (tRS) from RP\ High until WRITES to the Command User Interface [CUI] are recognized, RESETS the ISM and clears the status register.

Capacitance

Parameter/Condition	Symbol	Typ	Max	Units
Input Capacitance	Cin	5	8	pF
Output Capacitance	Cbyte	14	16	pF
	Cout	5	12	pF

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for any duration or segment of time may affect device reliability.

Chip Enable Truth Table

CE2	CE1	CE0	Device
VIL	VIL	VIL	Enabled
VIL	VIL	VIH	Disabled
VIL	VIH	VIL	Disabled
VIL	VIH	VIH	Disabled
VIH	VIL	VIL	Enabled
VIH	VIL	VIH	Enabled
VIH	VIH	VIL	Enabled
VIH	VIH	VIH	Disabled

Absolute Maximum Ratings

Voltage	Min	Max	Units	Notes
Temperature under Bias	-55	125	^{0}C	
Storage Temperature	-65	125	^{0}C	
For VCCQ=2.7v to 3.6v Voltage on any pin	-2	5	V	
Short Circuit Current		100	mA	1

Notes
1: All specified voltages are with respect to GND. Minimum DC voltage is -0.5v on input/output pins and -0.2v on Vcc and VPEN pins. During transitions, this level may undershoot to -2.0v for periods </= 20ns. Maximum DC voltage on input/output pins, Vcc and VPEN is VCC+0.5V which, during transitions, may overshoot to Vcc + 2.0v for periods <20ns.

Pin Description Table:

Signal Name	Symbol	Type	Pin	Description
Address	**A0, A1, A2. A3, A4, A5, A6, A7 A8, A9, A10, A11 A12,A13,A14,A15 A16,A17,A18,A19 A20,A21,A22,A23**	Input	**32,28,27,26, 25,24,23,22, 20,19,18,17, 13,12,11,10, 8,7,6,5, 4,3,1,30**	Address Inputs during READ and WRITE Operations. A0 is only used in x8 mode and will be a NC in x16 mode.
Chip Enables	**CE0, CE1, CE2**	Input	**14,2,29**	Three Chip Enable pins for Multiple devices. See chart for function
Write Enable	**WE**	Input	**55**	Write Control
Reset/Power-Down	**RP**	Input	**16**	Reset/Power-Down, When Low the control pin resets the status Reg. and ISM to array READ mode.
Output Enable	**OE**	Input	**54**	Ouput Enable control enable data output buffers when Low, and when High the output buffers are disabled
Byte Mode Control	**BYTE**	Input	**31**	Configuration Control pin. When High the device is in x16 mode, when Low the device is in Byte mode (x8)
Programming Voltage	**VPEN**	Input	**15**	Necessary Voltage pin for Programming, Erasing or configuring lock bits. Typically connected to VCC. When VPEN</=VPENLK, this enables Hardware Write Protect.
Status Pin/Flag	**STS**	Output	**53**	Indicates the status of the ISM. When configured in level mode, STS acts as a RY/BY\ pin. When configured in its pulse mode, it can pulse to indicate PROGRAM and or ERASE completion.
Input/Output Voltage	**VCCQ**	Supply	**43**	Separate/Isolated Voltage supply for Input/Output bus. Allows voltage matching to different interface standards.
Supply Voltage	**VCC**	Supply	**9, 37**	Power Supply: 2.7V - 3.6V
Digital Ground	**GND**	Supply	**21, 42, 48**	Ground
No Connect(s)	**NC**	-	**1, 30, 56**	No electrical connection or function

Bus Operations:

MODE	RP\	CE0	CE1	CE2	OE\	WE\	VPEN	DQ	NOTES	ADDRESS	STS Default Mode
Read Array	VIH	Enabled	Enabled	Enabled	VIL	VIH	X	Dout	1,2,3	X	High-Z (VOH with External PU)
Output Disable	VIH	Enabled	Enabled	Enabled	VIH	VIH	X	High-Z		X	X
Standby	VIH	Disabled	Disabled	Disabled	X	X	X	High-Z		X	X
Reset/Power-Down	VIL	X	X	X	X	X	X	High-Z		X	High-Z (VOH with External PU)
Read Identifier Codes	VIH	Enabled	Enabled	Enabled	VIL	VIH	X		4	See Figure 7 of Micron DS	High-Z (VOH with External PU)
Read Query	VIH	Enabled	Enabled	Enabled	VIL	VIH	X		5	See Figure 7 of Micron DS	High-Z (VOH with External PU)
Read Status (ISM off)	VIH	Enabled	Enabled	Enabled	VIL	VIH	X			X	X
Read Status (ISN on)	VIH	Enabled	Enabled	Enabled	VIL	VIH	X	Dout		X	X
Write	VIH	Enabled	Enabled	Enabled	VIH	VIL	VPENH	Din	3,6,7	X	X

Notes

1 Refer to DC Characteristics. When VPEN</= VPENLK, memory contents can be read but not altered
2 X can be VIL or VIH for control and address pins, and VPENLK or VPENH for VPEN. See DC Characteristics for VPENLK and VPENH voltages
3 In default mode, STA is VOL when the ISM is executing internal Block Erase, Program, or lock bit configuration algorithms. It is VOH when the ISM is not busy, in block erase suspend mode, program suspend mode, or reset/power-down mode.
4 See Read Identifier codes of the Micron Datasheet (DS)
5 See Read Query Mode Command section of the Micron Datasheet (DS)
6 Command Writes involving block erase, program, or lock bit configuration are reliably executed when VPEN=VPENH and VCC is within Specification
7 Refer to Table 4 on page 15 of the Micron Datasheet (DS)

DC Electrical Characteristics:

(VDD=3.0v-5%/+10%,TA=Min/Max temperatures of Operational Range chosen)

Symbol	Parameter	Test Conditions	Min	Max	Units	Notes
Vcc	Supply Voltage		2.7	3.6	V	
VccQ	Isolated Input/Output Supply		2.7	3.6	V	
ILI	Input Load Current	Vin=VccQ or GND, VCC=VCC Max., VCCQ = VCCQ Max		+/- 1.0	uA	
ILO	Output Leakage Current	Vin=VccQ or GND, VCC=VCC Max., VCCQ = VCCQ Max		+/-10.0	uA	
VIL	Input Low Voltage		-0.5	0.8	V	1
VIH	Input High Voltage		2	VCCQ+0.5	V	1
VOL	Output Low Voltage	VccQ=VccQ (MIN), IOL = 2mA		0.4	V	1,2
		VccQ=VccQ (MIN), IOL = 100uA		0.2	V	
VOH	Output High Voltage	VccQ=VccQ (MIN), IOH = 2.5mA	0.85xVCCQ		V	1
		VccQ=VccQ (MIN), IOH = 100uA	VCCQ-0.2		V	
VPENLK	Program Voltage Lockout			0.8	V	3,4,5
VPENH	Program Voltage			3.6	V	4,5,6
VLKO	Vcc Lockout Voltage		2.2		V	1
ICC1	Standby Current	CMOS Inputs; VCC= VCC (MAX), Device Enabled, RP\=VCCQ+/-0.2v	50	220	uA	
		TTL Inputs; VCC=VCC (MAX): Device Enabled, RP\=VIH	90	2000	uA	
ICC2	Power-Down Current	RP\=GND,+/-0.2V; IOUT (STS)=0mA	50	120	uA	
ICC3	Page Mode READ Current	CMOS Inputs; VCC=VCC(MAX); VCCQ=VCCQ(MAX) using standard 4-word page mode READS; Device is enabled; f=5MHz; IOUT=0mA	3	10	mA	
		CMOS Inputs; Vcc=Vcc(MAX); VCCQ=VCCQ(MAX) using standard 4-word page mode READS; Device is enabled; Ff=33MHz; IOUT=0mA	8	15	mA	
ICC4	Asynchronous READ Mode Current	CMOS Inputs; VCC=VCC(MAX); VCCQ=VCCQ(MAX) using standard work/byte single READS; Device Enabled; f=5MHz; IOUT=0mA	9	50	mA	
ICC5	PROGRAM or set LOCK BITS Current	CMOS Inputs, VPEN=VCC	17	60	mA	
		TTL Inputs, VPEN=VCC	17	70		
ICC6	BLOCL ERASE or CLEAR BLOCK LOCK bits Current	CMOS Inputs, VPEN=VCC	17	70	mA	
		TTL Inputs, VPEN=VCC	17	80		
ICC7	PROGRAM SUSPEND or BLOCK ERASE SUSPEND Current	Device is Disabled		10	mA	

Notes

[1] Sampled, not 100% tested
[2] Includes STS
[3] ICCWS and ICCES are specified with the device deselected. If the device is read or written while in ERASE SUSPEND mode, the device's curent draw is ICCR or ICCW
[4] BLOCK ERASE, PROGRAMMING, and LOCK BIT configurations are inhibited when VPEN</= VPENLK, and they are not guaranteed in the range betwn VPENLK (MAX) and VPENH (MIN), or above VPENH (Max)
[5] Typically, VPEN is connected to VCC
[6] VPENH (MIN) = 2.7v

Memory Command Set Operations:

Command	Scalable or Basic Command Set [SCS or BCS]	Bus Cycles	First Bus Cycle			Second Bus Cycle			Notes
			Operation	Address	Data	Operation	Address	Data	
READ ARRAY	SCS / BCS	1	WRITE	X	FFh				
READ IDENTIFIER CODES	SCS / BCS	>/= 2	WRITE	X	90h	READ	IA	ID	1
READ QUERY	SCS		WRITE	X	98h	READ	QA	QD	
READ STATUS REGISTER	SCS / BCS	2	WRITE	X	70h	READ	X	SRD	2
CLEAR STATUS REGISTER	SCS / BCS	1	WRITE	X	50h				
WRITE TO BUFFER	SCS / BCS	>2	WRITE	BA	E8h	WRITE	BA	N	3, 4, 5
WORD/BYTE PROGRAM	SCS / BCS	2	WRITE	X	40h or 10h	WRITE	PA	PD	6, 7
BLOCK ERASE	SCS / BCS	2	WRITE	BA	20h	WRITE	BA	D0h	5, 6
BLOCK ERASE/PROGRAM SUSPEND	SCS / BCS	1	WRITE	X	B0h				7, 8
BLOCK ERASE/PROGRAM RESUME	SCS / BCS	1	WRITE	X	D0h				7
CONFIGURATION	SCS	2	WRITE	X	B8h	WRITE	X	CC	
SET BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	BA	01h	
CLEAR BLOCK LOCK BITS	SCS	2	WRITE	X	60h	WRITE	X	D0h	
PROTECTION PROGRAM		2	WRITE	X	C0h	WRITE	PA	PD	

Key:

[IA]	Identifier Code address
[ID]	Data read from identifier Code
[BA]	Address within a Block
[QA]	Query data base Address
[PA]	Address of Memory location to be programmed
[QD]	Data read from Query data base
[SRD]	Data read from Status Register

Notes

[1]	Following the READ IDENTIFIER CODES command, READ operations access manufacturer, device, and block lock codes.
[2]	If the ISM is running, only DQ7 is valid; DQ15-DQ8 and DQ6-DQ0 are placed in High-Z
[3]	After the WRITE-to-BUFFER command is issued, check the XSR to make sure a buffer is available for WRITING
[4]	The number of Bytes/words to be written to the write buffer = n+1, where n=byte/word count argument. Count ranges on this device for byte mode are n=00H to n=1Fh and for word mode, n=0000h to 000Fh. The third and consecutive bus cycles, as determined by n, are for writing data into the write buffer. The CONFIRM command (D0h) is expected after exactly n+1 WRITE cycles; any other command at that point in the sequence aborts the WRITE-to-BUFFER operation.
[5]	The WRITE-to-BUFFER or ERASE operation does not begin until a CONFIRM command (D0h) is issued
[6]	Attempts to issue a BLOCK ERASE or PROGRAM to a locked block will fail
[7]	Etiher 40h or 10h is recognized by the ISM as the byte/word program setup
[8]	PROGRAM SUSPEND can be issued after either the WRITE-to-BUFFER or WORD/BYTE PROGRAM operation is inititated. The CLEAR BLOCK LOCK BITS operation simultaneously clears all block lock bits.

AC Switching Characteristics:

(VDD=3.0V –5%/+10%, TA= Min. / Max. temperatures of Operational Range chosen)

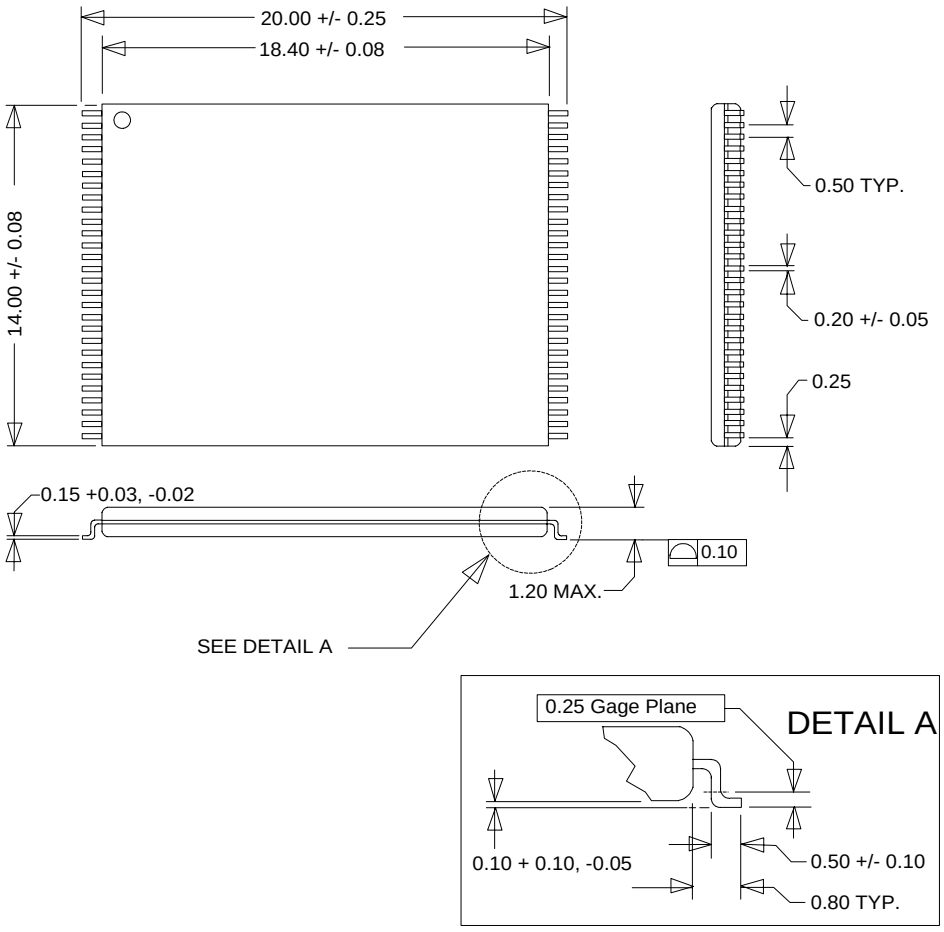
Parameter	Symbol	128Mb		Units	Notes
Write Operations		**Min**	**Max**		
RP\ High Recovery to WE\ (CEx) going Low	**tRS**	1.0		us	1
CEx (WE\) Low to WE\ (CEx) going High	**tCS**	0		ns	
Write Pulse Width	**tWP**	70.0		ns	
Data Setup to WE\ going High	**tDS**	50.0		ns	
Address Setup to WE\ going High	**tAS**	55.0		us	
CEx Hold from WE\ High	**tCH**	0		ns	
Data Hold from WE\ High	**tDH**	0			
Address Hold from WE\ High	**tAH**	0			
Write Pulse Width High	**tWPH**	30		ns	
VPEN Setup to WE\ going High	**tVPS**	0		ns	1
Write Recovery before READ	**tWR**	35		ns	
WE\ High to STA going Low	**tSTS**		200	ns	
VPEN Hold from valid SRD, STS going High	**tVPH**	0		ns	1
WE\ High to Status Registry Busy	**tWB**		200	ns	1
				ns	
Block Erase, Program and Lock Bit Performance		**Typ**	**Max**		
Write Buffer Byte Program time (Program time 32 Bytes/ 16 Words)	**tWED1**	180	654	us	
Byte/Word Program time	**tWED2**	11.20	630	us	
Block Program time	**tWED3**	0.70	1.70	sec	
Block Erase time	**tWED4**	0.75	5	sec	
Set Lock Bits time	**tWED5**	10.00	75	us	
Clear Block Lock Bits time	**tWED6**	0.50	0.70	sec	
Program Suspend Latency time to Read	**tLPS**	25	30	us	
Erase Suspend Latency time to Read	**tLES**	25	35	us	
Read Only Operations		**Min**	**Max**		
Read Cycle time	**tRC**	115		ns	
Address to Output Delay	**tAA**		115	ns	
CEx to Output Delay	**tACE**		115	ns	
OE\ to Non-Array Output Delay	**tAOE**		50	ns	
OE\ to Array Output Delay	**tAOA**		25	ns	
RP\ High to Output Delay	**tRWH**		210	ns	
CEx to Output in Low-Z	**tOEC**	0		ns	1
OE\ to Output in Low-Z	**tOEO**	0		ns	1
Cex High to Output in High-Z	**tODC**		35	ns	1
OE\ High to Output in High-Z	**tODO**		15	ns	1
Output Hold from Address, Cex, or OE\ change, whichever occurs first	**tOH**	0		ns	1
CEx Low to BYTE\ High or Low	**tCB**		10	ns	1
BYTE\ to Output Delay	**tABY**		1,000	ns	1
BYTE\ to Output in High-Z	**tODB**		1,000	ns	1
CEx High to CEx Low	**tCWH**	0.0		ns	1
Page Address Access	**tAPA**		25	ns	
Reset Specifications		**Min**	**Max**		
RP\ Pulse Low time	**tPLPH**	35		us	
RP\ High to RESET during BLOCK ERASE, PROGRAM, or Lock Bit configuration	**tPHRH**		100	ns	

Notes to Switching Specifications:

1. Sampled, not 100% tested

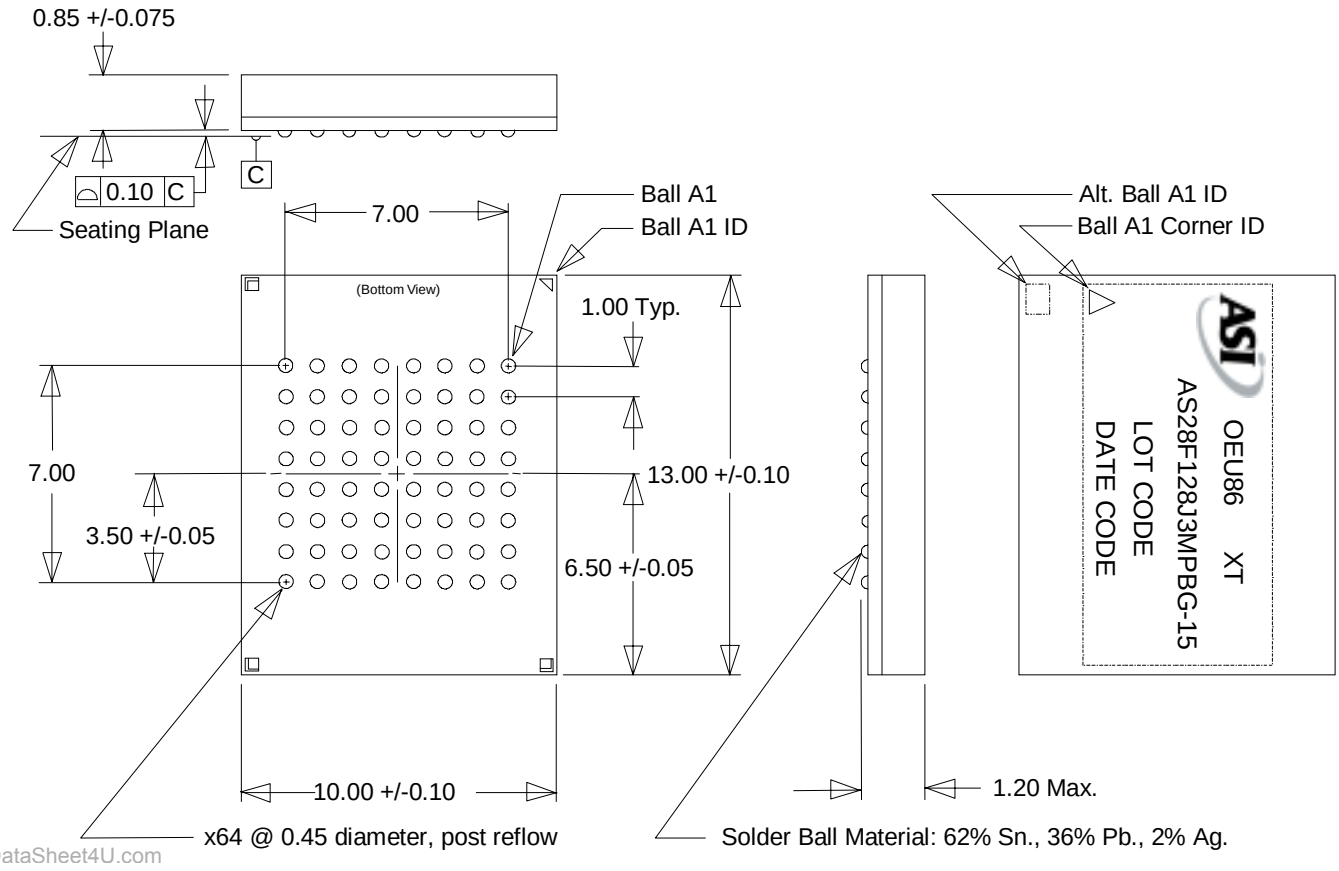
Mechanical Diagram

TSOP, Type I, 56 Pin
(Dimensions in **mm)**



Mechanical Diagram

PBGA, 10mm x 13mm, 64 Ball w/1.00mm Pitch
(Dimensions in **mm)**



ASI Ordering Information

ASI Part Number	Configuration	Speed (ns)	Pkg.	Comments
Enhanced Operating Range (-40^{0}C to +105^{0}C)				
AS28F128J3MRG-15/ET	128Mb, x8/x16 Q-Flash	115	TSOP1-56	
AS28F128J3MPBG-15/ET	128Mb, x8/x16 Q-Flash	115	FBGA-64	Consult Factory, MOQ's Apply
Extended Operating Range (-55^{0}C to +125^{0}C)				
AS28F128J3MRG-15/XT	128Mb, x8/x16 Q-Flash	115	TSOP1-56	
AS28F128J3MPBG-15/XT	128Mb, x8/x16 Q-Flash	115	FBGA-64	Consult Factory, MOQ's Apply