Quartz Crystal Requirement for ALC100/ALC100P

This document describes the quartz crystal requirements for clocking ALC100/P.

1. Frequency and Oscillation Circuits

ALC100/P are designed to work from a crystal with 24.576MHz. Fig-1 shows the equivalent circuits of crystal and oscillation circuits within ALC100/P.

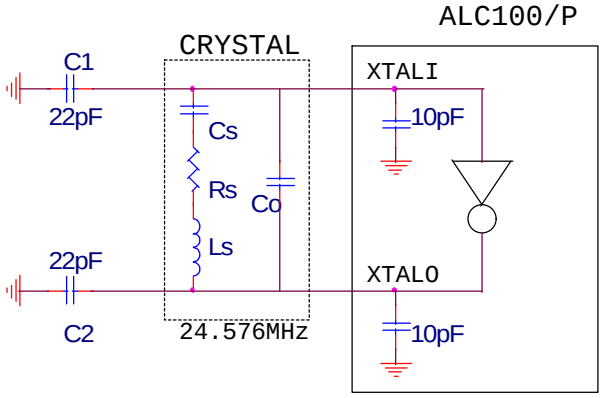

Fig-1 oscillation circuits

The series resonant frequency

$$Fs \cong \frac{1}{2p\sqrt{Ls * Cs}}$$

, and parallel resonant frequency

$$Fp \cong \frac{1}{2p\sqrt{\frac{Ls * Cs * Co}{Cs + Co}}}$$

The oscillated frequency between *Fs* and *Fp*

$$Fo = Fs * \sqrt{1 + \frac{Cs}{Co + CL}}$$

where CL=(C1+10pF)//(C2+10pF)

2. Crystal Requirements

General Specifications	Requirements
Holder Type	HC-49 U/S
Crystal Freq.	24.576 MHz
Oscillation Mode	Fundamental
Load Cap. (CL)	16 ~20 pF
Freq. Tolerance(25°C)	+/- 50 ppm
Effective Series Resistance (Rs)	40 ohm max
Effective Shunt Capacitance (Co)	7 pF
Drive Level	< 0.1 mW
Insulation Resistance	500 Mohm min. at DC 100V

Table-1 Crystal General Specification

3. Load Capacitance (CL)

To operate between Fs and Fp requires external load capacitance. Although ALC100/P has embed internal 10pF capacitors at XTALI and XTALO, the oscillated frequency may be a little higher than 24.576MHz if no C1 and C2 placed.

To reduce the bit clock jitter and get more accurate frequency, the external capacitor C1 and C2 most be used.

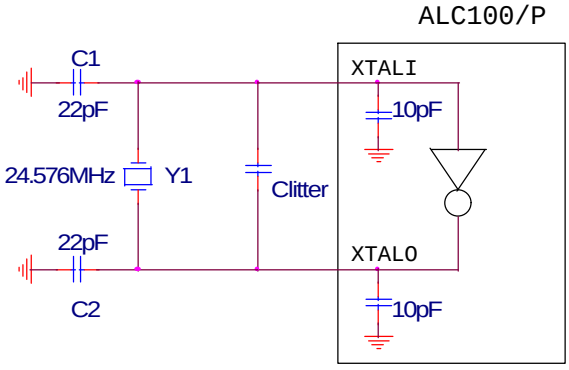

Fig-2 Clitter due to PCB Trace

In ideal case, ignore the Clitter at suggested C1=C2=22pF, the equivalent load capacitance is

$$CL = (22\,pF + 10\,pF)\,//(22\,pF + 10\,pF) = 16\,pF$$

According to Table-1 specification, the crystal with *CL* is 16pF is adapted. But in most case, the litter capacitor (Clitter) generated by PCB trace is existent. So the real CL is

$$CL = (C1 + 10\,pF)\,//(C2 + 10\,pF) + Clitter$$

Consider the litter capacitance , crystal with CL=20pF is allowable.

4. Drive Level

ALC100/P has lower drive capability than ALC200. To guarantee the successful oscillation, Crystals with drive level less than 100mW are recommended.

If used crystal with drive level exceed 100mW or PCB trace capacitance is large, C1 and C2 must be replaced by lower value to reduce the drive loading. The disadvantage of reducing C1 and C2 is increasing oscillated frequency about several KHz and get worse bit clock jitter. To conquer this problem, you can reduce C2 first. If it still doesn't work, reduce C1 and C2 step by step, keep the relation C1 is larger than C2 to help oscillation occurs. In most of case, this methodology is useful to force oscillation and suppress clock jitter.