AVERLOGIC

AL4V183/185

16K, 64K-Bit Line FIFO

Applications

- Multimedia System
- Video line capture
- TBC(Time Base Corrector)
- Hard Disk cache memory
- Anti-skip audio data buffer

Description

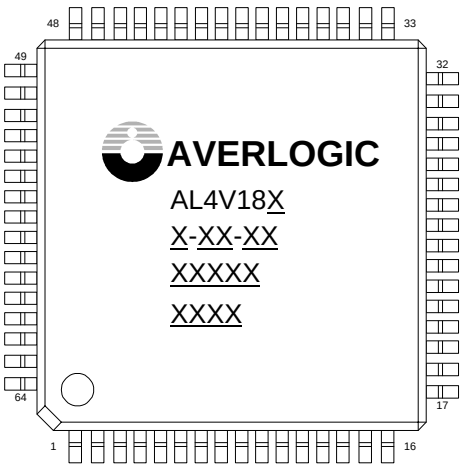
The AL4V183/185 series memory products are high-performance, low-power 18-bit read/write FIFO (First-In-First-Out) memory chip designed to buffer high speed streaming data for a wide range of applications, such as optical disk data caching, video line data buffering. This product series supports bus conversion functions, such as Bus-Matching, Endian selection that can reduce designing efforts.

Features

- High performance, low-power, FIFO(First-In First-Out) memory
- 1K x18 bit 1/O port (AL4V183)
- 4K x18 bit I/O port (AL4V185)
- High clock speed (100 MHz)
- Fully independent read/write access
- Output enable control (data skipping)
- User selectable input and output bus width
- Big/Little-Endian word format selectable
- 3.3V±10% power supply with 5V signal input tolerance
- Standard 64-pin STQFP

Ordering Information

Part number	AL4V183, AL4V185
Package	64-pin plastic STQFP
Power Supply	+3.3V±10%



STQFP PACKAGE TOP VIEW

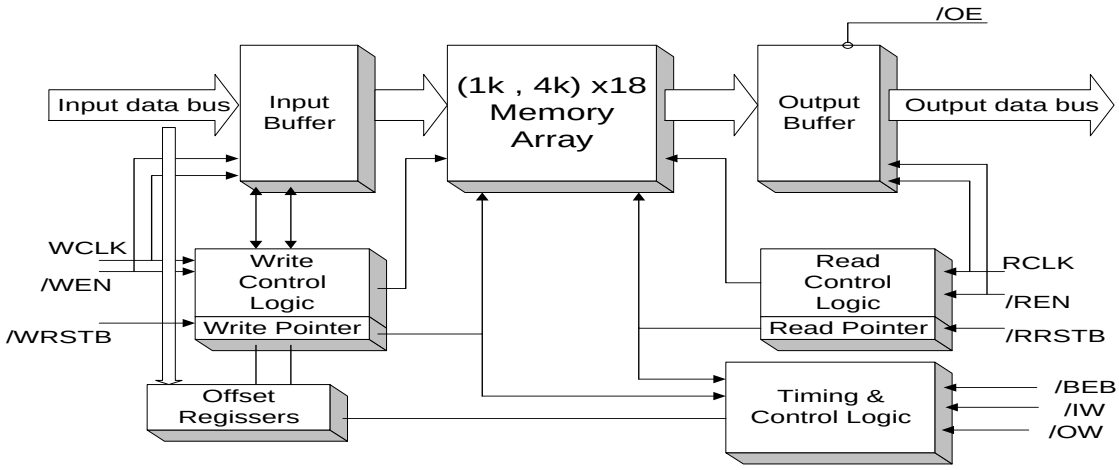


Figure 1. AL4V18x FIFO Block Diagram

The 18bit input and output ports operate independently at a maximum speed of 100 MHz. The built-in address decoder and pointer managing circuits provide a straightforward bus interface to serially read/write memory that reduces inter-chip design efforts. The AL4V18x embedded memory array and high performance process technologies with extended controller functions (read skip, fixed and programmable status flags... etc.) offer flexible memory management.

These FIFOs support up to 18-bit input and output data bus-width that is controlled by separate clock and enable signals respectively. The input data is acquired at each rising edge of a free running write clock while a write enable control pin is asserted. The output data is available after each rising edge of a free running read clock while a read enable and output enable control pins are asserted. When output enable (/OE) is LOW, the data output bus is active. If /OE is HIGH, the output data bus will be in a high-impedance. This signal can control whether the data is going to be skipped during the read operation.

Bus-Matching feature can flexibly configure input and output bus width. The chip can automatically convert the input data bus width to match up output data bus width by packing or unpacking the data. A Big-Endian/Little-Endian data word format is provided to invert the read-in bytes sequence for output. And the Retransmit function allows data to be reread from the FIFO more than once.

These chips are available as a 64pin STQFP Package.

AVERLOGIC TECHNOLOGIES, INC. TEL: 1 408 361-0400 e-mail: sales_usa@averlogic.com URL: www.averlogic.com
AVERLOGIC TECHNOLOGIES, CORP. TEL: 886 2-87523988 e-mail: sales@averlogic.com.tw URL: www.averlogic.com.tw