

Product Summary

V_{DS}	25	V	
Q_{g}	14	nC	
Q_{gd}	2.5	nC	
$R_{\text{DS(on)}}$	V_{GS} = 3.0V	2.8	mΩ
	V_{GS} = 4.5V	2.1	mΩ
	V _{GS} = 8.0V 1.9		mΩ
V_{th}	1.1	V	

Top View

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Maximum Values ($T_A = 25^{\circ}C$ unless otherwise stated)

Symbol	Parameter	Value	Units
V _{DS}	Drain to Source Voltage	25	V
V _{GS}	Gate to Source Voltage	+10 / -6	V
ID	Continuous Drain Current, T _c = 25°C	100	А
	Continuous Drain Current ¹	31	А
IDM	Pulsed Drain Current, $T_A = 25^{\circ}C^2$	200	А
PD	Power Dissipation ¹	3.1	W
T _J , Т _{STG}	Operating Junction and Storage Temperature Range		°C
E _{AS}	Avalanche Energy, single pulse I_D =66A, L = 0.1mH, R_G = 25 Ω	218	mJ

 $R_{0,0} = 39^{\circ}$ C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB. 1.

2. See Figure 10



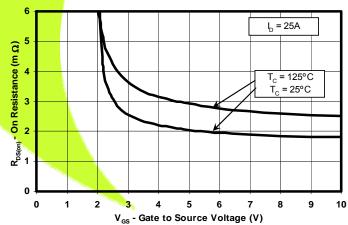
Features

• Ultra Low Qg & Qgd

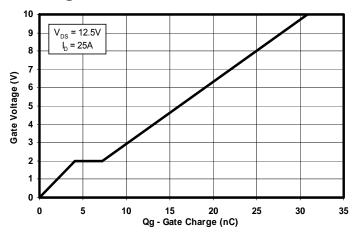
Avalanche Rated

RoHS Compliant

• Pb Free Terminal Plating



Gate Charge



Ordering Information

Туре	Package	Package Media	Qty	Ship
CSD16321Q5	QFN 5X6 Plastic Package	13 inch reel	2500	Tape and Reel

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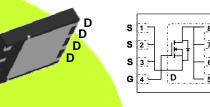
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QFN 5mm x 6mm Plastic Package





Electrical Characteristics (T_A = 25^oC unless otherwise stated)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Static Ch	aracteristics				•	
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I₀ = 250µA	25	—	—	V
IDSS	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V	_	—	1	μA
lgss	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = 10V	—	—	100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	0.9	1.1	1.4	V
		V _{GS} = <mark>3.0V, I_D = 25A</mark>	_	2.8	3.5	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = <mark>4.5V, I_D = 25A</mark>	_	2.1	2.6	mΩ
		V _{GS}	_	1.9	2.4	mΩ
g fs	Transconductance	V _{DS} = 12.5V, I _D = 25A	_	150	_	S
Dynamic	Characteristics				•	
Ciss	Input Capacitance		_	2360	3100	pF
Coss	Output Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V$	_	1700	2200	pF
CRSS	Reverse Transfer Capacitance	- f = 1MHz	_	115	150	pF
Rg	Series Gate Resistance		_	1.2	_	Ω
Qg	Gate Charge Total (4.5V)		-	14	19	nC
Q _{gd}	Gate Charge Gate to Drain		_	2.5	_	nC
Q _{gs}	Gate Charge Gate to Source	- V _{DS} = 12.5V, I _D = 25A	_	4.0	—	nC
Q _{g(th)}	Gate Charge at Vth		_	2.1	_	nC
Qoss	Output Charge	V_{DS} = 15V, V_{GS} = 0V	_	36	_	nC
t _{d(on)}	Turn On Delay Time		_	11	_	ns
tr	Rise Time	$V_{DS} = 12.5V$	_	19	_	ns
t _{d(off)}	Turn Off Delay Time	V_{GS} = 4.5V I _D = 25A R _G = 2.7 Ω	—	40	—	ns
tr	Fall Time	NG - 2.7 SZ	_	30	-	ns
Diode Ch	naracteristics					
Vsd	Diode Forward Voltage	$I_{\rm S}$ = 25A, $V_{\rm GS}$ = 0V	—	0.8	1.0	V
Qrr	Reverse Recovery Charge	V _{dd} =13V, I _F = 25A, di/dt = 300A/µs	-	33	_	nC
ter	Reverse Recovery Time	V _{dd} =13V, I _F = 25A,		32	_	ns

di/dt = 300A/µs

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Reverse Recovery Time

trr

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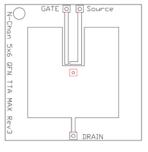


Thermal Characteristics (T_A = 25^oC unless otherwise stated)

Symbol	Parameter		Тур	Max	Units
Thermal Characteristics					
R ejc	Thermal Resistance Junction to Case ³			1.1	°C/W
R _{ØJA}	Thermal Resistance Junction to Ambient ^{3,4}			50	°C/W

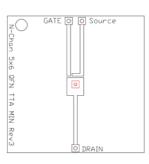
3. $R_{\theta jc}$ is determined with the device mounted on a 1in square 2 oz. Cu pad on a 1.5x1.5 in .060in thick FR4 board. $R_{\theta jc}$ is guaranteed by design while $R_{\theta ca}$ is determined by the user's board design.

4. Device mounted on FR4 Material with 1in² of 2 oz. Cu.



Max Reja = 48°C/W when mounted on 1in² of

2 oz. Cu.



Max R_{θ} ja = 115°C/W when mounted on min pad area of

2 oz. Cu.

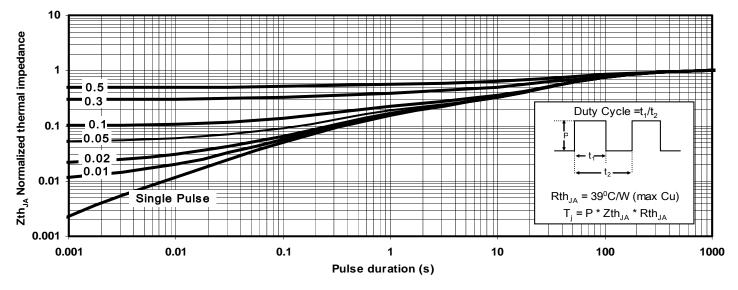
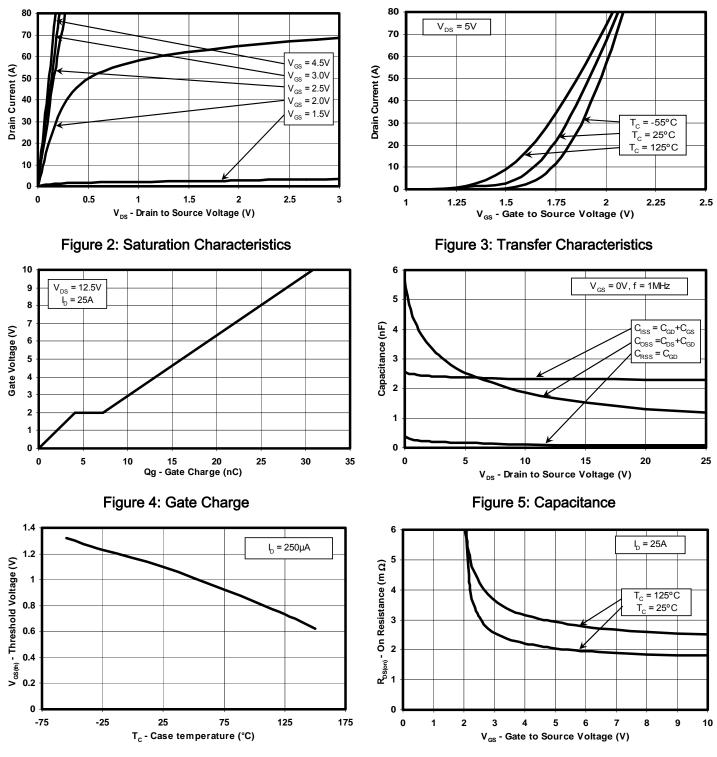


Figure 1: Transient Thermal Impedance

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Typical MOSFET Characteristics (T_A = 25^oC unless otherwise stated)





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Figure 7: On Resistance vs. Gate Voltage

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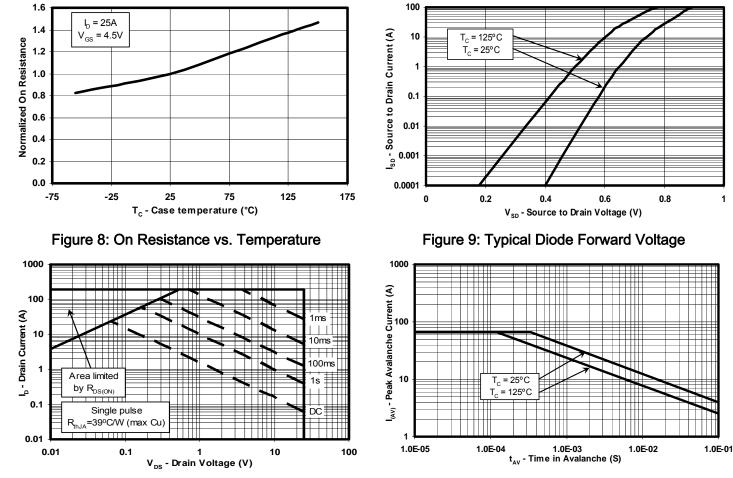


Figure 10: Maximum Safe Operating Area

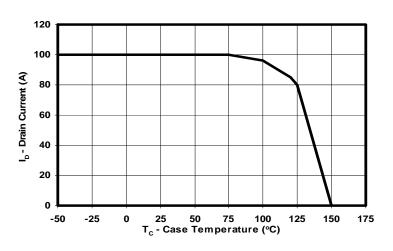


Figure 12: Maximum Drain Current vs. Temperature

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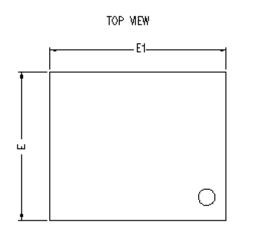
Figure 11: Single Pulse Unclamped Inductive

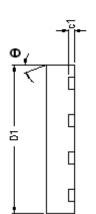
Switching

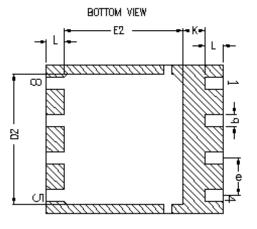
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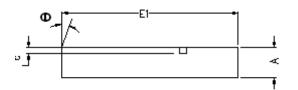
Q5 Package Dimensions





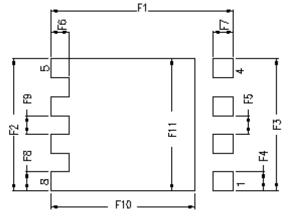


SIDE MEW



DIM	MILLIM	ETERS	INC	HES	
DIM	Min	Max	Min	Max	
Α	0.950	1.050	0.037	0.039	
b	0.360	0.460	0.014	0.018	
С	0.150	0.250	0.006	0.010	
c1	0.150	0.250	0.006	0.010	
D1	4.900	5.100	0.193	0.201	
D2	4.320	4.520	0.170	0.178	
E	4.900	5.100	0.193	0.201	
E1	5.900	6.100	0.232	0.240	
E2	3.920	4.12	0.154	0.162	
е	1.27 TYP		0.050		
L	0.510	0.710	0.020	0.028	
θ	0.00	-	-	-	
K	0.760	-	0.030	-	
F1	6.205	6.305	0.244	0.248	
F2	4.460	4.560	0.176	0.180	
F3	4.460	4.560	0.176	0.180	
F4	0.650	0.700	0.026	0.028	
F5	0.620	0.670	0.024	0.026	
F6	0.630	0.680	0.025	0.027	
F7	0.700	0.800	0.028	0.031	
F8	0.650	0.700	0.026	0.028	
F9	0.620	0.670	0.024	0.026	
F10	4.900	5.000	0.193	0.197	
F11	4.460	4.560	0.176	0.180	

RECOMMENDED PCB PATTERN

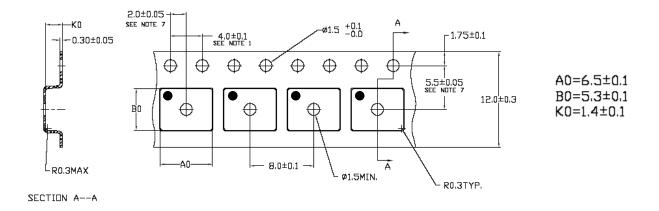


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Q5 Tape and Reel Information



Note:

- 1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE +/-0.2
- 2. CAMBER NOT TO EXCEED 1mm IN 100mm, NONCUMULATIVE OVER 250mm
 - 3. MATERIAL:BLACK STATIC DISSIPATIVE POLYSTYRENE
 - 4. ALL DIMENSIONS ARE IN mm (UNLESS OTHERWISE SPECIFIED)
 - 5. THICKNESS: 0.30 +/-0.05mm

Package Marking Information

Location:

1st Line

CSD = Fixed Characters

NNNNN = Product Code

2nd Line (Date Code)

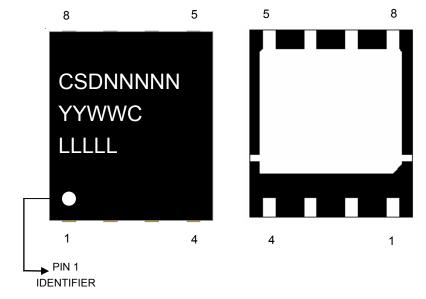
- YY = Last 2 digits of the Year
- WW = 2-digit Work Week

C = Country of Origin

- > Philippines = P
- > Taiwan = T
- > China = C

3rd Line

LLLL= Last 5 digits of the Wafer Lot #



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