

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

KEY PARAMETERS

V_{DRM}	2200V
I_{T(AV)}	4040A
I_{TSM}	54000A
dV/dt*	1500V/μs
dI/dt	300A/μs

* Higher dV/dt selections are available on request

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V _{DRM} and V _{RRM} (V)	Conditions
DCR4060V22	2200	T _{vj} = -40°C to 125°C, I _{DRM} = I _{RRM} = 200mA, V _{DRM} , V _{RRM} t _p = 10ms V _{DSM} & V _{RSM} = V _{DRM} & V _{RRM} + 100V respectively
DCR4060V20	2000	
DCR4060V18	1800	

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR4060V22

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

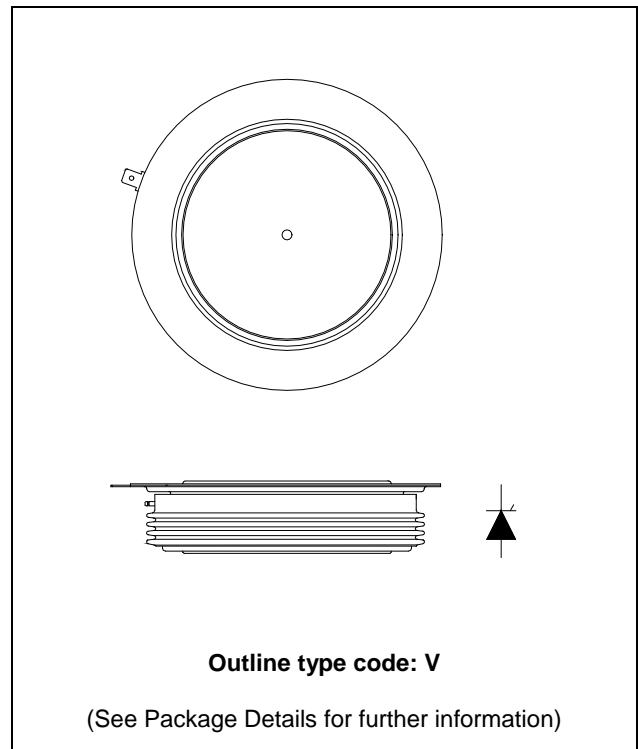


Fig. 1 Package outline

CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$ unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	4040	A
$I_{T(RMS)}$	RMS value	-	6350	A
I_r	Continuous (direct) on-state current	-	5860	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$ $V_R = 0$	54.0	kA
I^2t	I^2t for fusing		14.6	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	7.5	$^{\circ}\text{C}/\text{kW}$
		Single side cooled	Anode DC	-	13.0	$^{\circ}\text{C}/\text{kW}$
			Cathode DC	-	17.8	$^{\circ}\text{C}/\text{kW}$
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 54kN (with mounting compound)	Double side	-	2.0	$^{\circ}\text{C}/\text{kW}$
			Single side	-	4.0	$^{\circ}\text{C}/\text{kW}$
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range			-55	125	$^{\circ}\text{C}$
F_m	Clamping force			48	59	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125°C	-	200	mA	
V_{TM}	Instantaneous forward voltage	At 4000A peak, T _j = 125°C	1.15	1.30	V	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V _{DRM} , T _j = 125°C, gate open	-	1500	V/μs	
di/dt	Rate of rise of on-state current	From 67% V _{DRM} to 2x I _{T(AV)} Gate source 30V, 10Ω tr < 0.5μs, T _j = 125°C	Repetitive 50Hz	-	150	A/μs
			Non-repetitive	-	300	A/μs
V_{T(TO)}	Threshold voltage - Low level	500A to 2300A at T _{case} = 125°C	-	0.78	V	
	Threshold voltage - High level	2300A to 7000A at T _{case} = 125°C	-	0.92	V	
r_T	On-state slope resistance - low level	500A to 2300A at T _{case} = 125°C	-	0.16	mΩ	
	On-state slope resistance - High level	2300A to 7000A at T _{case} = 125°C	-	0.10	mΩ	
t_{gd}	Delay time	V _D = 67% V _{DRM} , gate source 30V, 10Ω tr = 0.5μs, T _j = 25°C	-	3	μs	
t_q	Turn-off time	T _j = 125°C, V _R = 200V, di/dt = 1A/μs, dV _{DR} /dt = 20V/μs linear	-	600	μs	
Q_s	Stored charge	I _T = 2000A, T _j = 125°C, di/dt = 1A/μs	390	1920	μC	
I_{RR}	Reverse recovery current	V _{R(peak)} ~ 1300V, V _{RM} ~ 900V	17	36	A	
I_L	Latching current	T _j = 25°C, V _D = 5V	-	3	A	
I_H	Holding current	T _j = 25°C, R _{G-K} = ∞, I _{TM} = 500A, I _T = 5A	-	300	mA	

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% $V_{DRM}, T_{case} = 125^{\circ}C$	0.4	V
I_{GT}	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	250	mA
I_{GD}	Gate non-trigger current	At 50% $V_{DRM}, T_{case} = 125^{\circ}C$	10	mA

CURVES

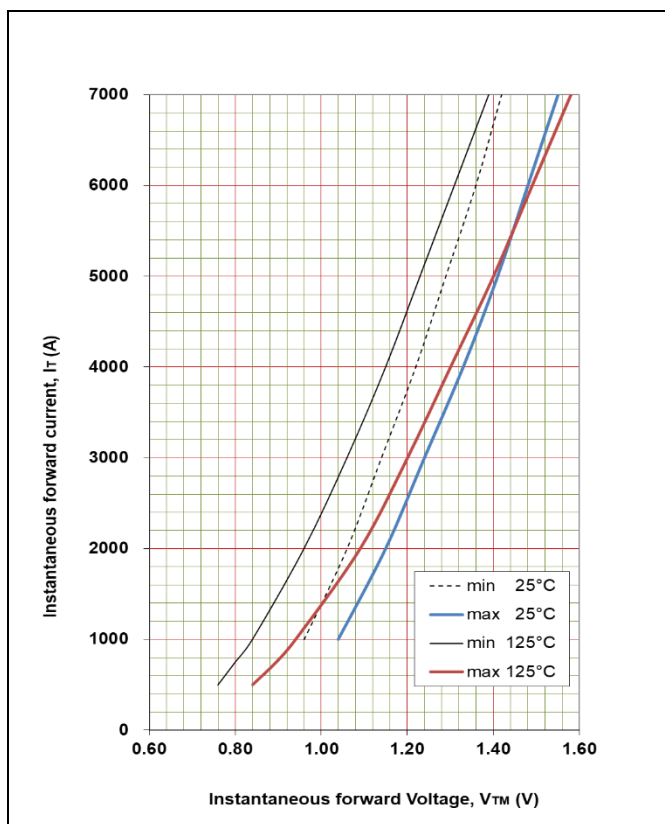


Fig. 2 Maximum & minimum on state characteristics

V_{TM} EQUATION

$$V_{TM} = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where $A = 0.404689$

$B = 0.051381$

$C = 0.000056$

$D = 0.003938$

These values are valid for $T_j = 125^{\circ}C$ for I_T 500A to 7000A

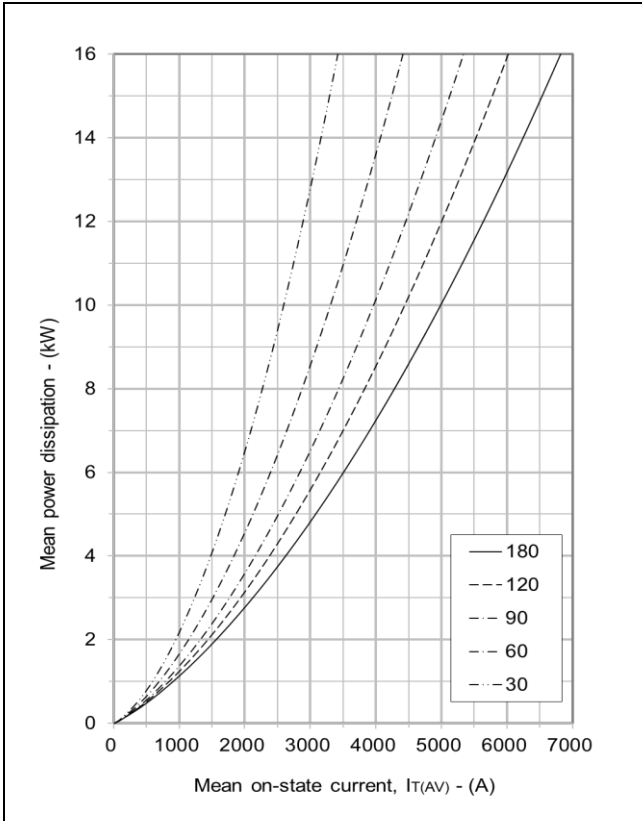


Fig. 3 On-state power dissipation - sine wave

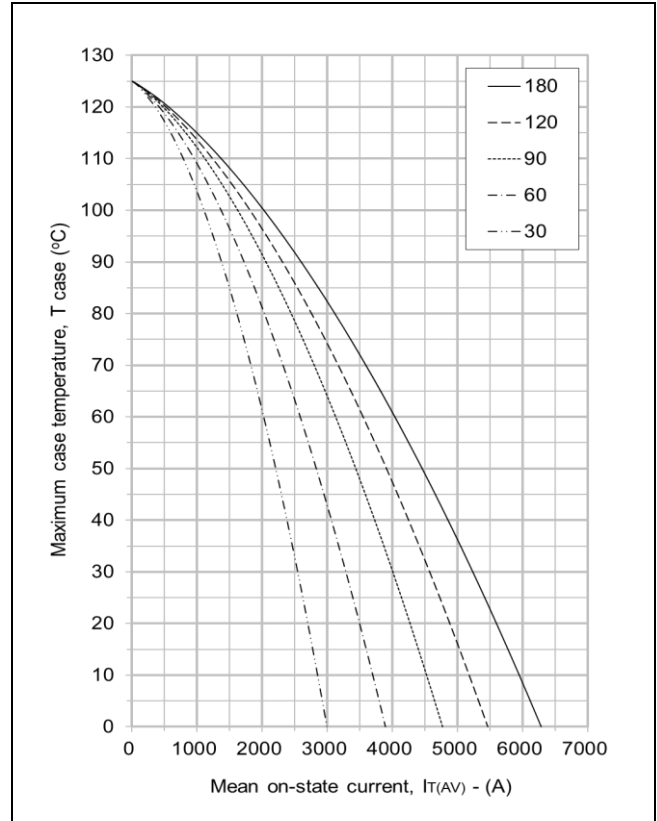


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

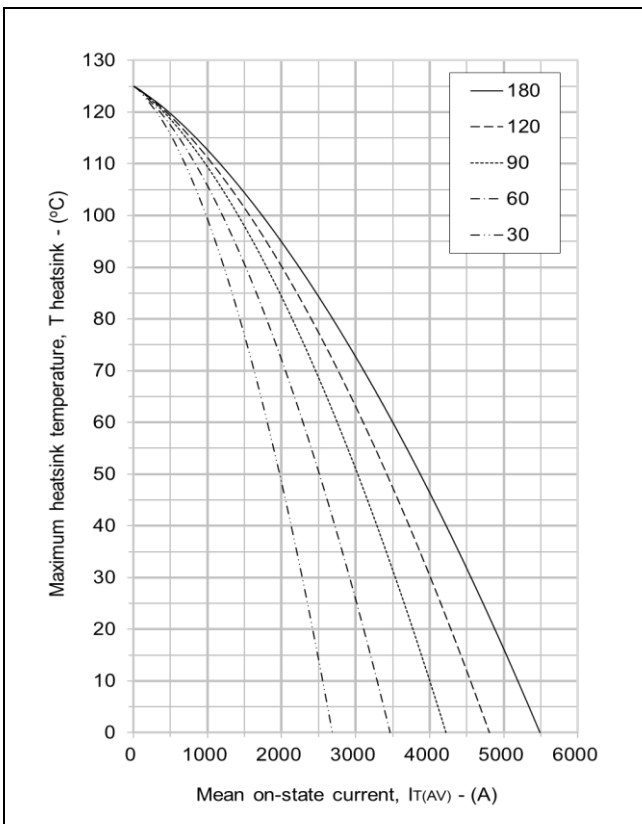


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

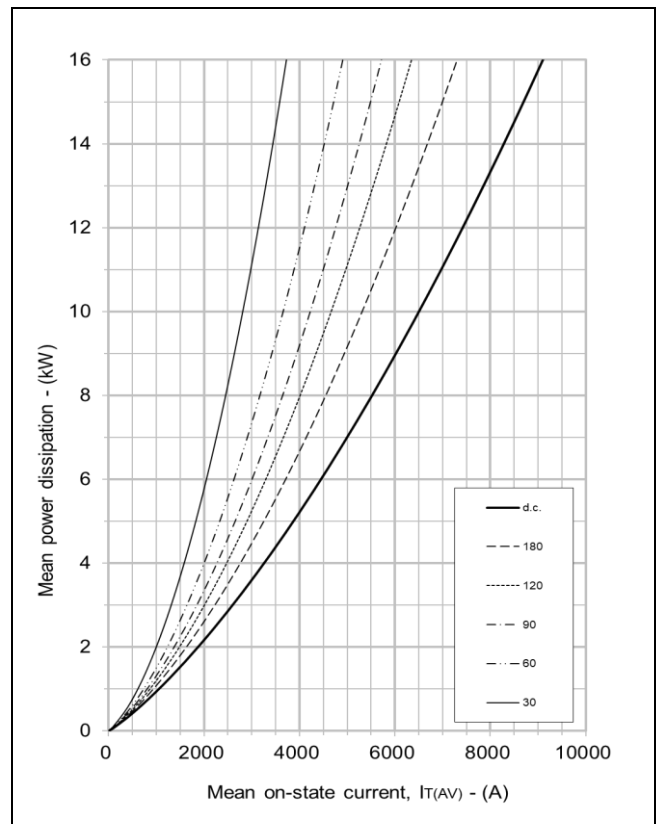


Fig. 6 On-state power dissipation - rectangular wave

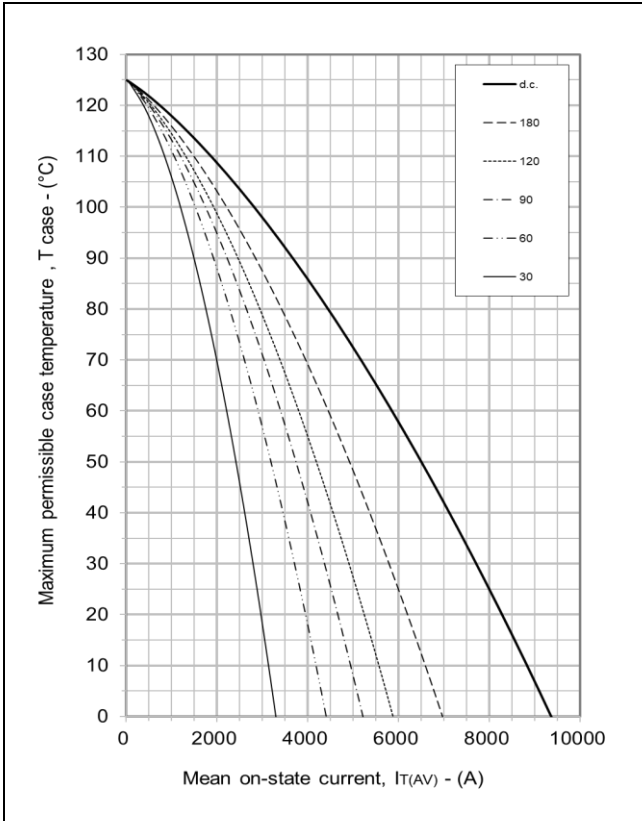


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

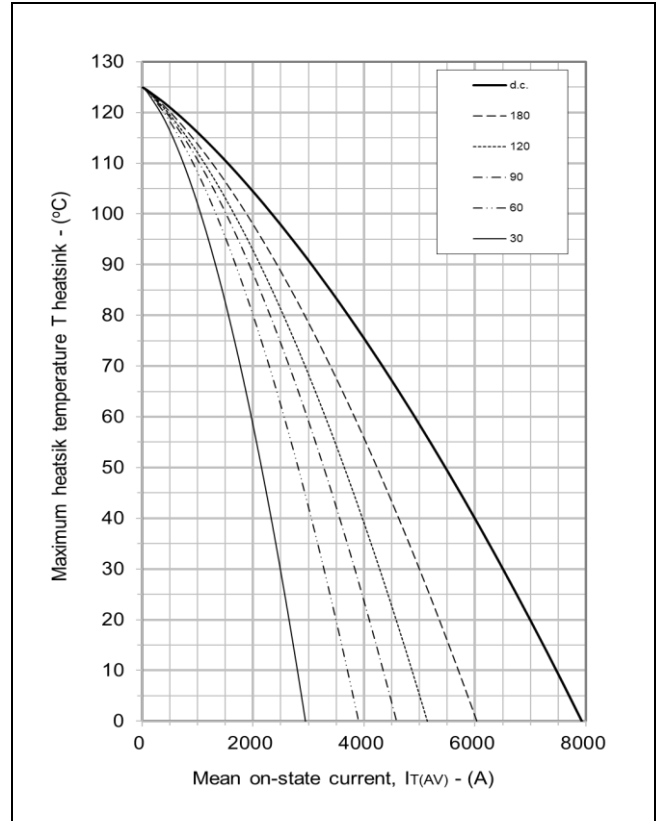


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave

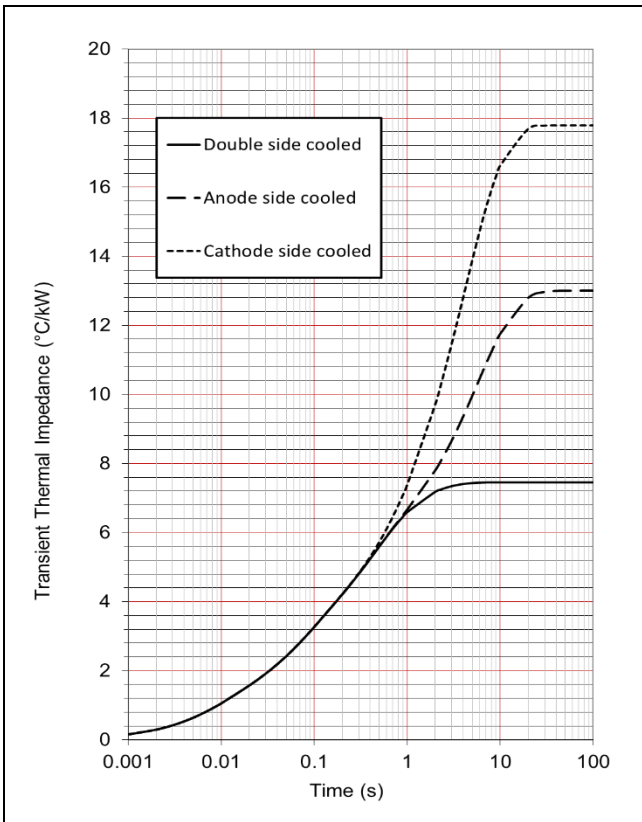


Fig. 9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

		1	2	3	4
Double side cooled	Ri(°C/kW)	0.921	1.830	3.402	1.304
	Ti(s)	0.008	0.058	0.408	1.209
Anode side cooled	Ri(°C/kW)	0.903	1.672	3.010	7.427
	Ti(s)	0.008	0.054	0.314	5.624
Cathode side cooled	Ri(°C/kW)	0.948	2.066	1.688	13.085
	Ti(s)	0.008	0.065	0.389	4.145

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

α°	Double side cooling	
	sine	rect
180	1.34	0.88
120	1.57	1.30
90	1.83	1.54
60	2.08	1.81
30	2.27	2.11
15	2.36	2.28

α°	Anode Side Cooling	
	sine	rect
180	1.34	0.88
120	1.57	1.30
90	1.84	1.54
60	2.08	1.81
30	2.28	2.11
15	2.37	2.28

α°	Cathode Sided Cooling	
	sine	rect
180	1.33	0.88
120	1.57	1.29
90	1.83	1.53
60	2.07	1.80
30	2.26	2.10
15	2.35	2.26

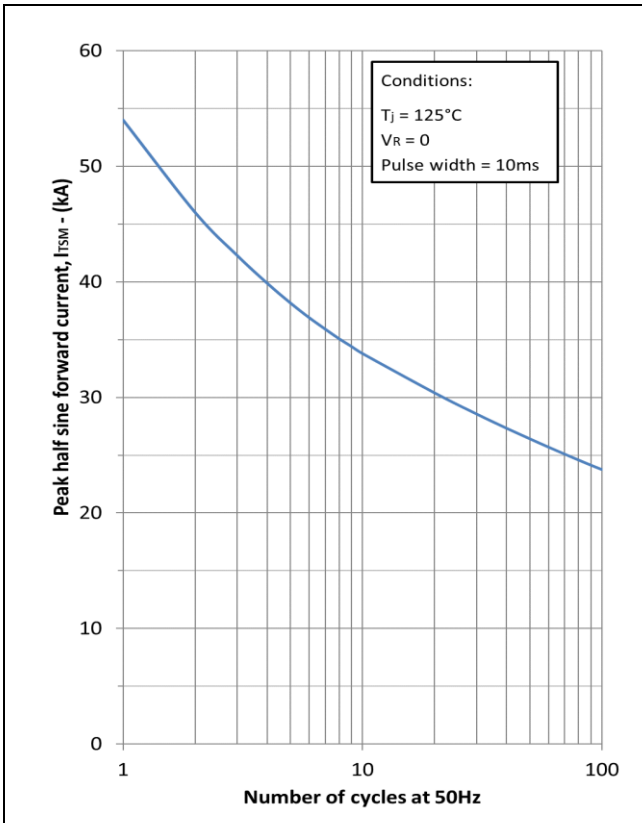


Fig. 10 Multi-cycle surge current

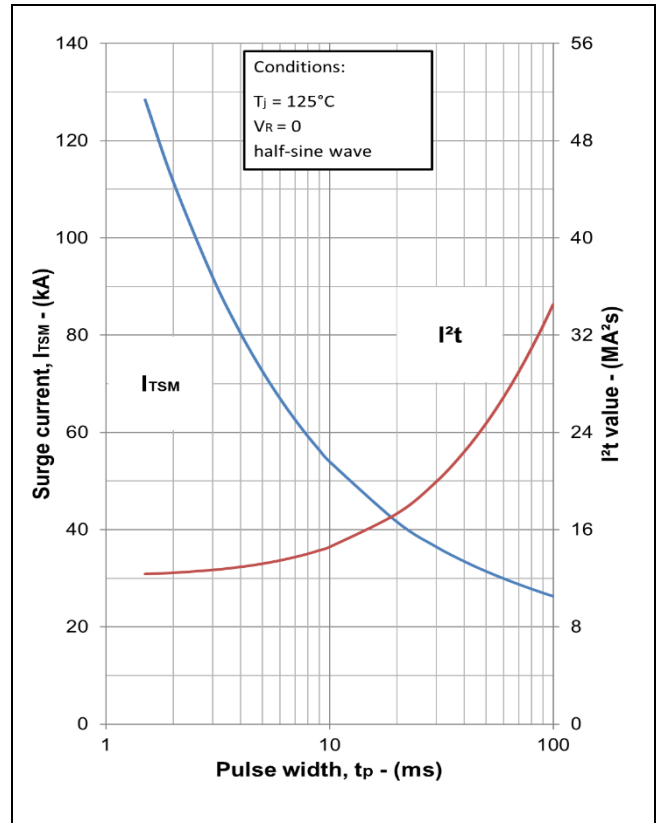


Fig. 11 Single-cycle surge current

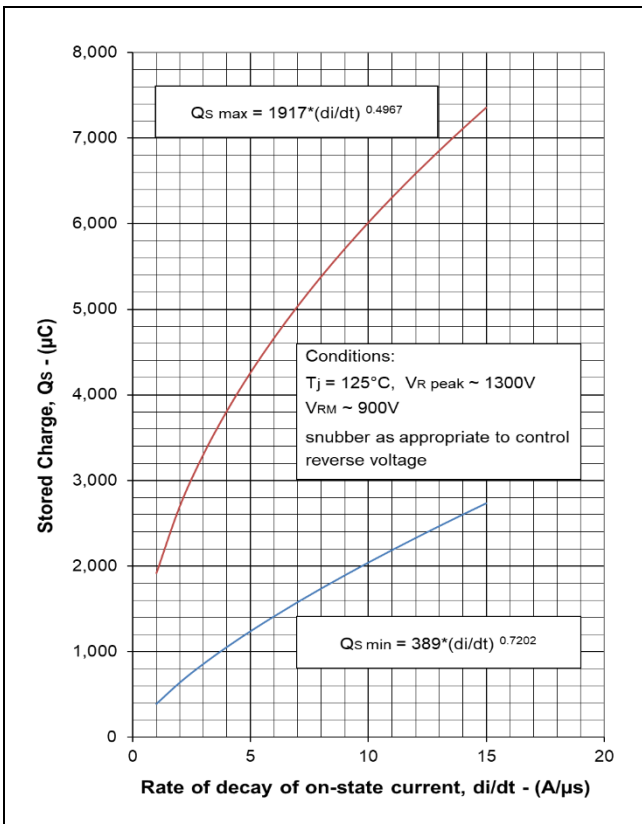


Fig. 12 Stored charge

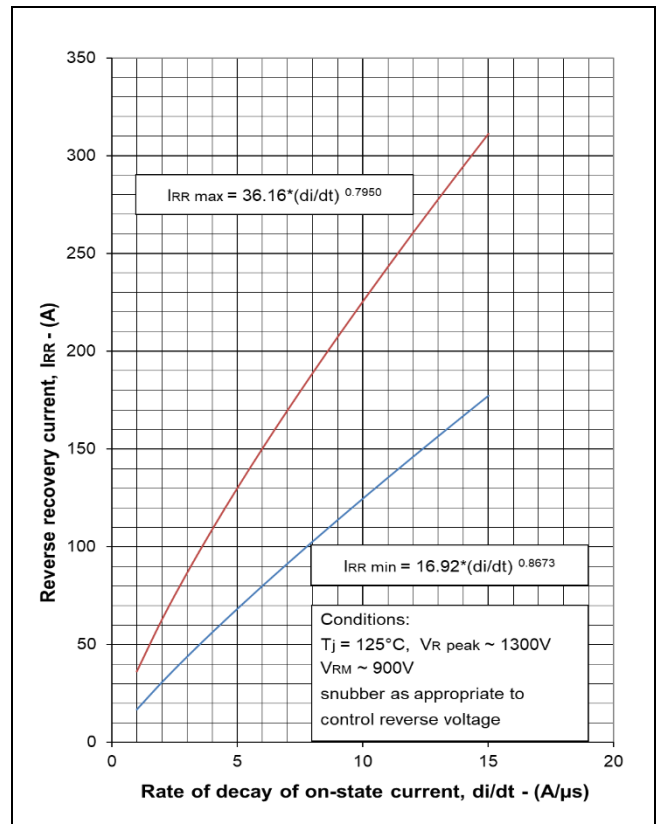


Fig. 13 Reverse recovery current

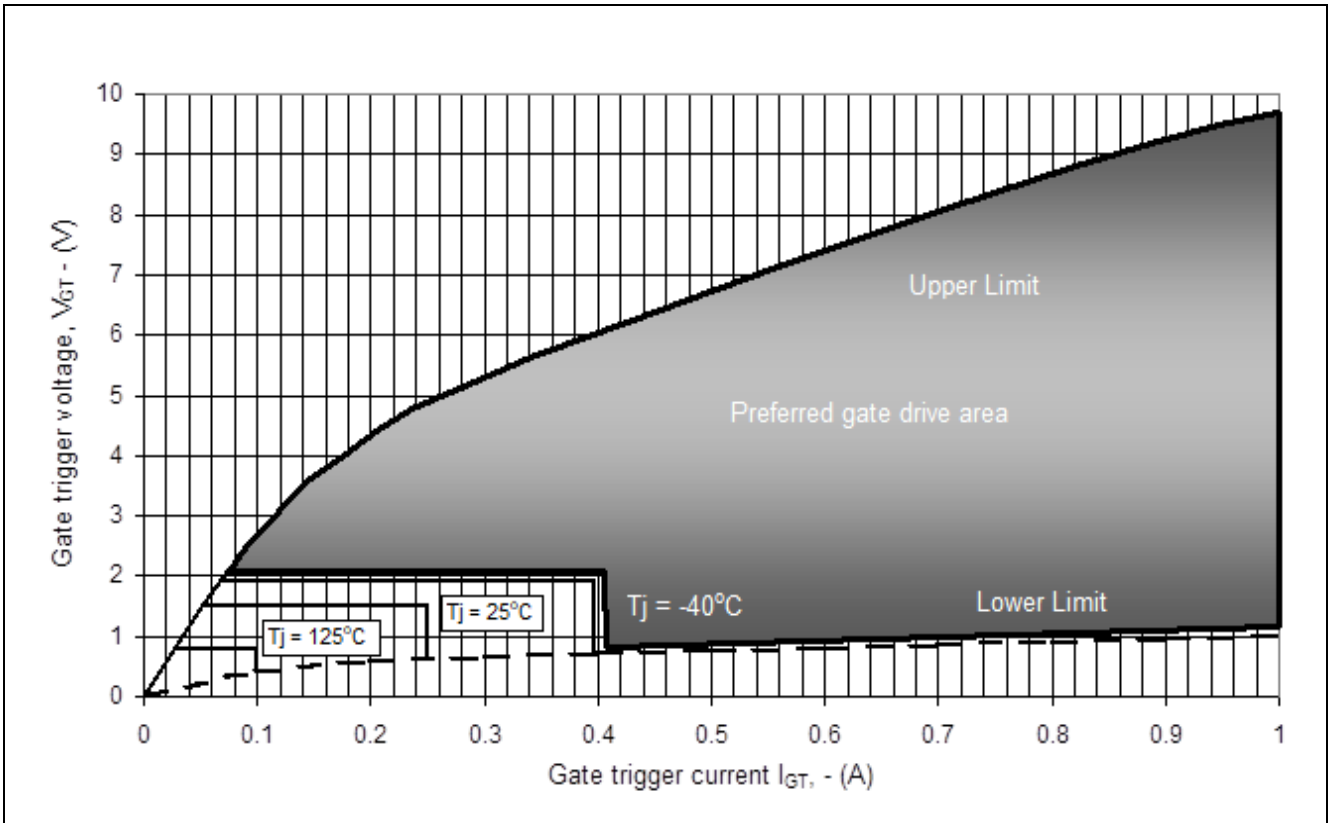


Fig. 14 Gate characteristics

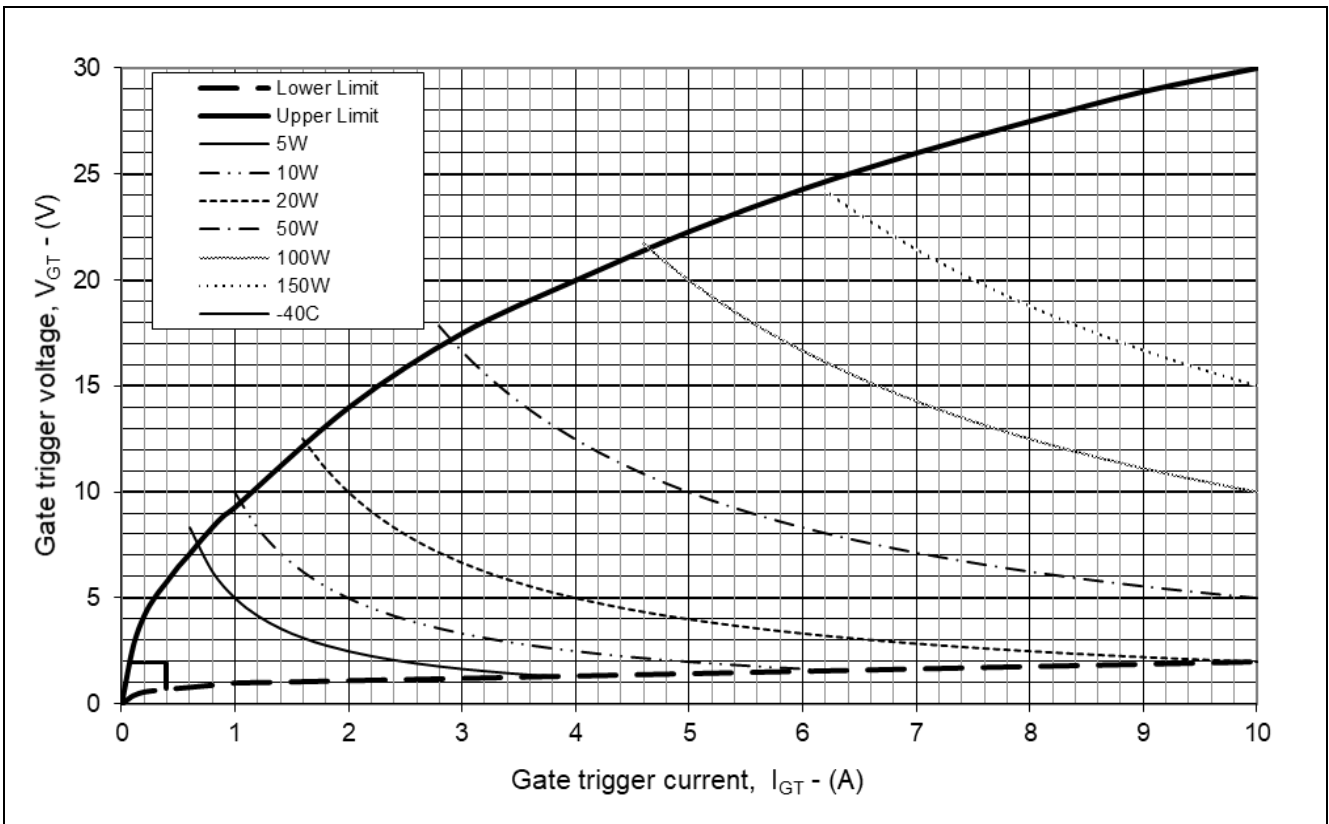


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE

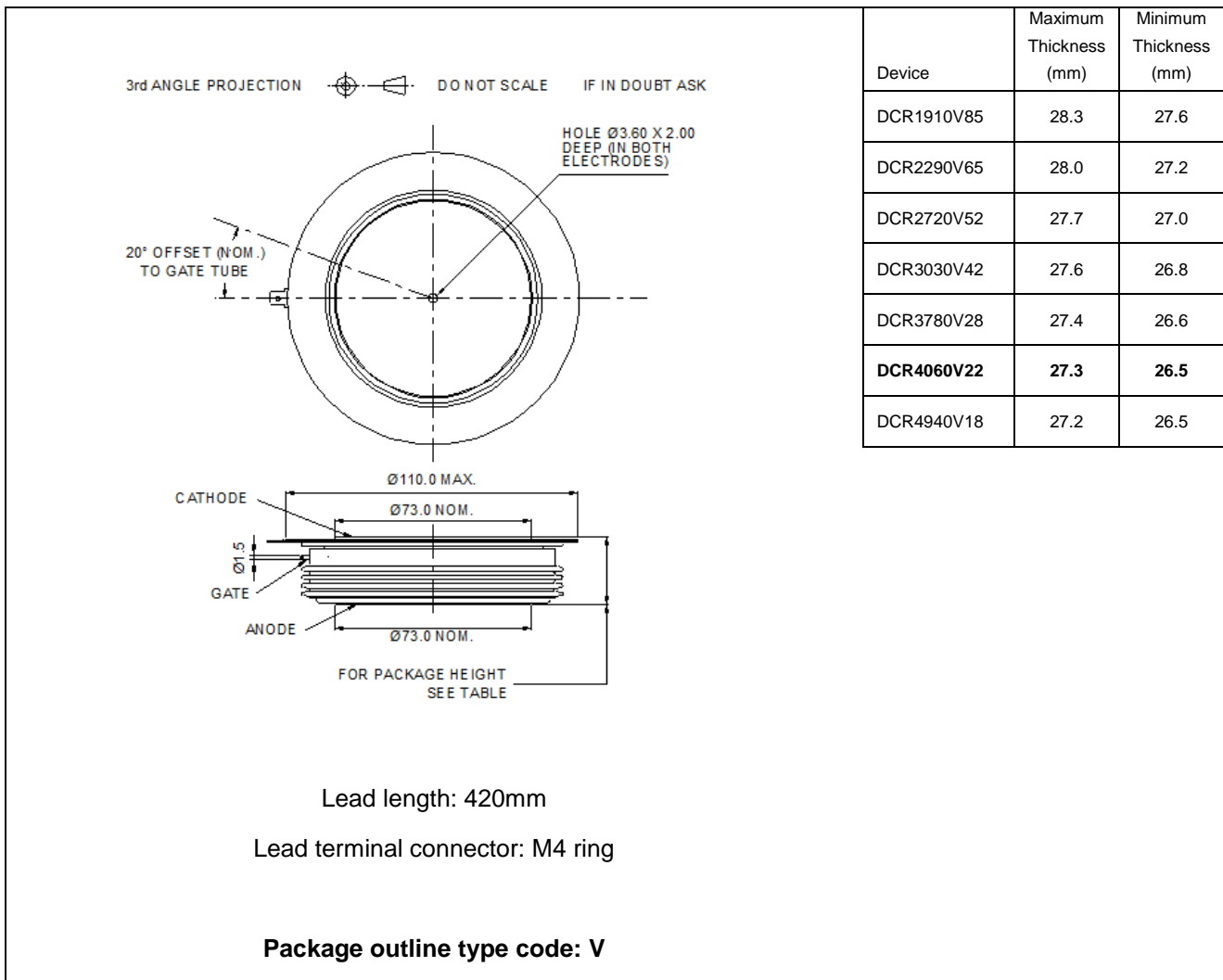


Fig. 16 Package outline

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