DALLAS SEMICONDUCTOR

DS3803
1024k Flexible NV SRAM SIMM

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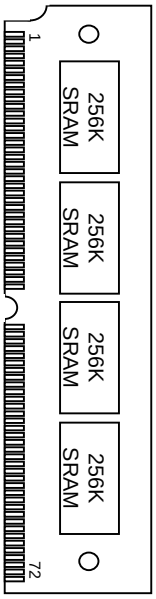
FEATURES

- Flexibly organized as 32k x 32, 64k x 16 or 128k x 8bits
- 10 years minimum data retention in the absence of external power
- Nonvolatile circuitry transparent to and independent from host system
- Automatic write protection circuitry safeguards against data loss
- Separate control and data signals for each SRAM allow byte, word or doubleword access
- Fast access time of 70 ns
- Full V_{CC} ± 10% operating range
- Employs popular JEDEC standard 72-position SIMM connector
- Extremely thin design built using TSOP-package IC components

PIN ASSIGNMENT



DS3803 72-Pin SIMM

PIN DESCRIPTION

A0 - A14	-	Address Inputs
D0A - D7A	-	Data Inputs/Outputs, Byte A
D0B - D7B	-	Data Inputs/Outputs, Byte B
D0C - D7C	-	Data Inputs/Outputs, Byte C
D0D - D7D	-	Data Inputs/Outputs, Byte D
$\overline{CEA}$ - $\overline{CED}$	-	Chip Enable Inputs
$\overline{WEA}$ - $\overline{WED}$	-	Write Enable Inputs
$\overline{OEA}$ - $\overline{OED}$	-	Output Enable Inputs
VCC	-	+5V Power Supply
GND	-	Ground
NC	-	No Connect

DESCRIPTION

The DS3803 is a self-contained, 1,048,576-bit, nonvolatile static RAM which can be flexibly organized as 32k x 32, 64k x 16 or 128k x 8. Built using four 32k x 8 SRAMs, four nonvolatile control ICs and four lithium batteries, this nonvolatile memory contains all necessary control circuitry and lithium energy sources to maintain data integrity in the absence of power for more than 10 years. The DS3803 employs the popular JEDEC standard 72-position SIMM connection scheme and requires no additional circuitry.

READ MODE

The DS3803 executes a read cycle whenever $\overline{WE}$ (Write enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 15 address inputs (A_0 - A_{14}) defines which byte of data is to be accessed from the selected SRAMs. Valid data will be available to the data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied, then data access must be measured from the later occurring signal and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than t_{ACC} .

WRITE MODE

The DS3803 executes a write cycle whenever both $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS3803 provides full functional capability for V_{CC} greater than 4.5 volts and write-protects by 4.25 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC}. Should the supply voltage decay, the NV SRAM automatically write-protects itself, all inputs become don't care, and all outputs become high impedance. As V_{CC} falls below approximately 3.0 volts, power switching circuits connect the lithium energy sources to the RAMs to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuits connect external V_{CC} to the RAMs and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts.

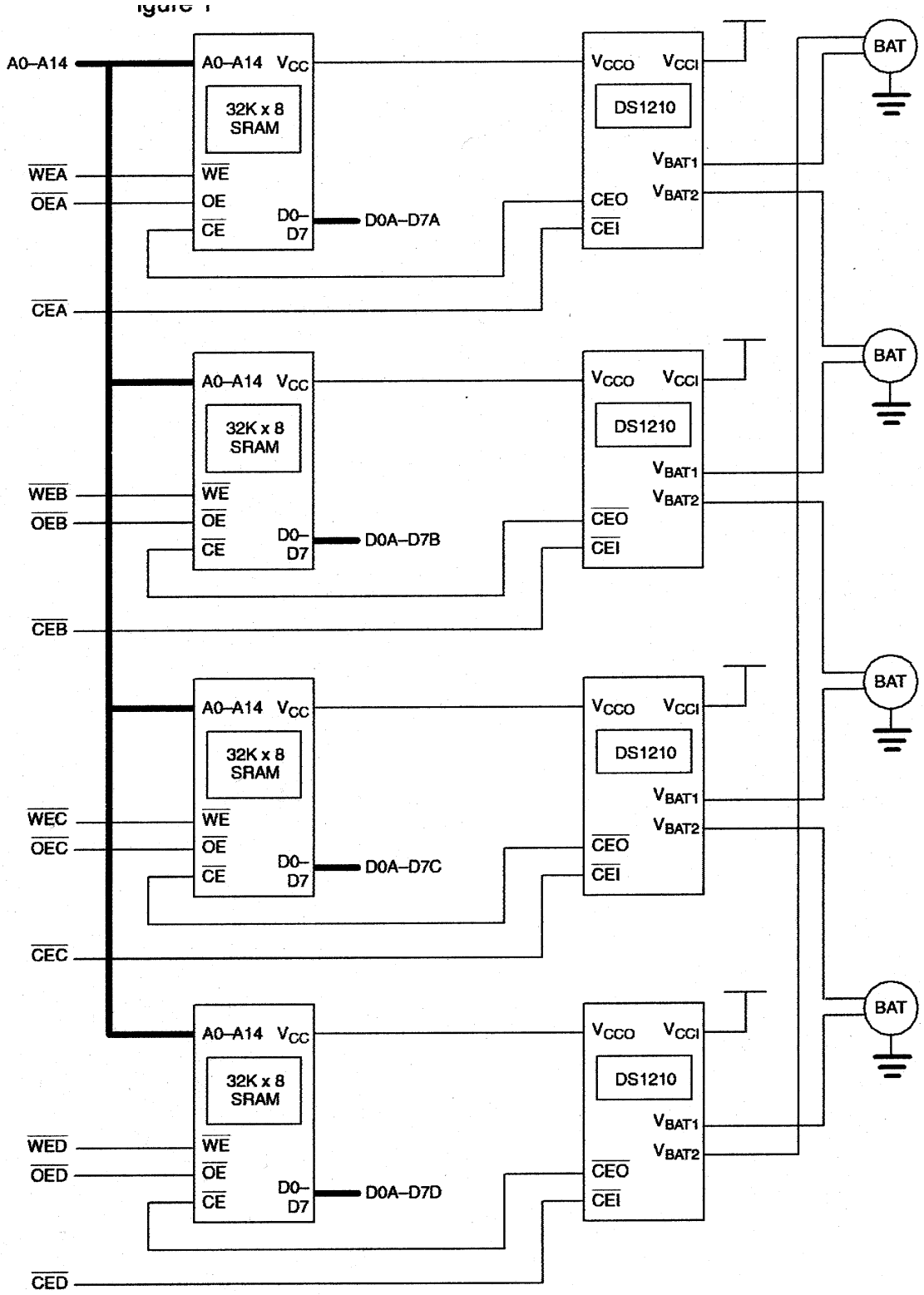
The DS3803 checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the DS3803, the battery voltages are checked with precision comparators. If both batteries providing backup power to a particular SRAM are less than 2.0 volts, the second memory access to that SRAM is inhibited. Battery status for each SRAM can therefore be determined by a three-step process. First, a read cycle is performed to any location within that SRAM in order to save the contents of that location. A subsequent write cycle can then be executed to the same memory location, altering data. If a subsequent read cycle fails to verify the written data, then battery voltage for that SRAM is less than 2.0V and data is in danger of being lost.

The DS3803 also provides battery redundancy. In many applications data integrity is paramount. The DS3803 provides two batteries for each SRAM and an internal isolation switch to select between them. During battery backup, the battery with the highest voltage is selected for use. If one battery fails, the other automatically takes over. The switch between batteries is transparent to the user.

PIN DESCRIPTION Table 1

PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	V_{CC}	16	D2B	31	D5C	46	NC	61	A9
2	D0A	17	D3B	32	D6C	47	$\overline{CED}$	62	A10
3	D1A	18	D4B	33	D7C	48	$\overline{OED}$	63	A11
4	D2A	19	D5B	34	NC	49	$\overline{WED}$	64	A12
5	D3A	20	D6B	35	$\overline{CEC}$	50	GND	65	A13
6	D4A	21	D7B	36	$\overline{OEC}$	51	V_{CC}	66	A14
7	D5A	22	NC	37	$\overline{WEC}$	52	A0	67	NC
8	D6A	23	$\overline{CEB}$	38	D0D	53	A1	68	NC
9	D7A	24	$\overline{CEB}$	39	D1D	54	A2	69	NC
10	NC	25	$\overline{WEB}$	40	D2D	55	A3	70	NC
11	$\overline{CEA}$	26	D0C	41	D3D	56	A4	71	NC
12	$\overline{OEA}$	27	D1C	42	D4D	57	A5	72	GND
13	$\overline{WEA}$	28	D2C	43	D5D	58	A6		
14	D0B	29	D3C	44	D6D	59	A7		
15	D1B	30	D4C	45	D7D	60	A8		

BLOCK DIAGRAM Figure 1



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0ºC to 70ºC
Storage Temperature -40ºC to +85ºC

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0ºC to 70ºC)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1 input Voltage	V_{IH}	2.2		V_{CC}+0.3	V	
Logic 0 input Voltage	V_{IL}	-0.3		+0.8	V	

DC ELECTRICAL CHARACTERISTICS (T_A = 0ºC to 70ºC; V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}	$0V \le V_{IN} \le V_{CC}$	-4		+4	µA
Output Leakage Current	I_{LO}	$0V \le V_{IN} \le V_{CC}$, all $\overline{CE} = V_{IH}$	-1		+1	µA
Operating Current	I_{CCO}	min cycle, duty=100% all $\overline{CE} = V_{IL}$, $I_{I/O} = 0$, $V_{IN} = V_{IH}$ or V_{IL}			300	mA
Standby Current	I_{CCS}	all $\overline{CE} = V_{IH}$			20	mA
Output High Current	I_{OH}	$V_{OH} = 2.4V$	-1.0			mA
Output Low Current	I_{OL}	$V_{OL} = 0.4V$	2.1			mA

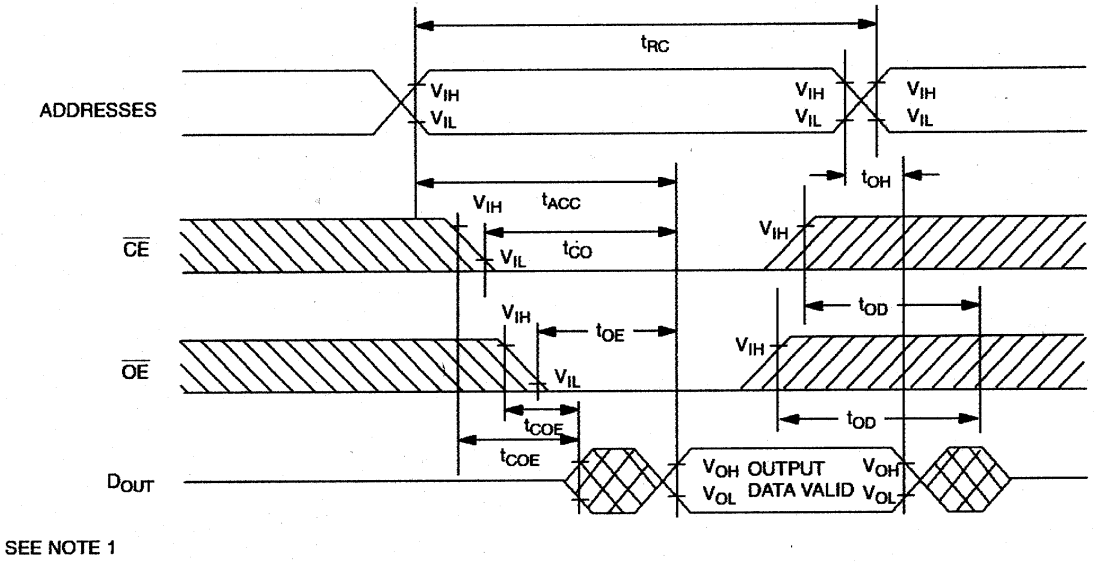
CAPACITANCE (T_A = 25ºC)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			8	pF	
Output Capacitance	$C_{I/O}$			10	pF	

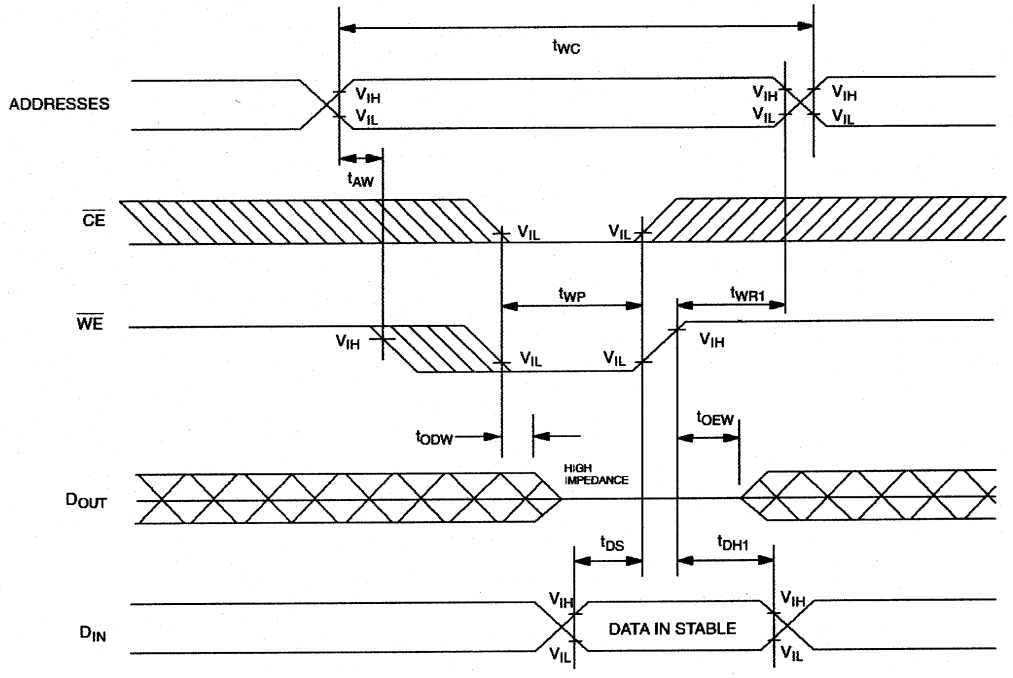
AC ELECTRICAL CHARACTERISTICS (T_A = 0ºC to 70ºC; V_{CC} = 5V ±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	70			ns	
Access Time	t_{ACC}			70	ns	
$\overline{OE}$ to Output Valid	t_{OE}			35	ns	
$\overline{CE}$ to Output Valid	t_{CO}			70	ns	
$\overline{OE}$ **or** $\overline{CE}$ to Output Active	t_{COE}	5			ns	5
Deselection to Output High Z	t_{OD}			25	ns	5
Output Hold after Address Change	t_{OH}	5			ns	
Write Cycle Time	t_{WC}	70			ns	
Write Pulse Width	t_{WP}	55			ns	3
Address Setup Time	t_{AW}	0			ns	
Write Recovery Time	t_{WR1} t_{WR2}	5 15			ns	11 12
$\overline{WE}$ Active to Output High Z	t_{ODW}			25	ns	5
$\overline{WE}$ Inactive to Output Active	t_{OEW}	5			ns	5
Data Setup Time	t_{DS}	30			ns	4
Data Hold Time	t_{DH1} t_{DH2}	0 10			ns	11 12

TIMING DIAGRAM: READ CYCLE

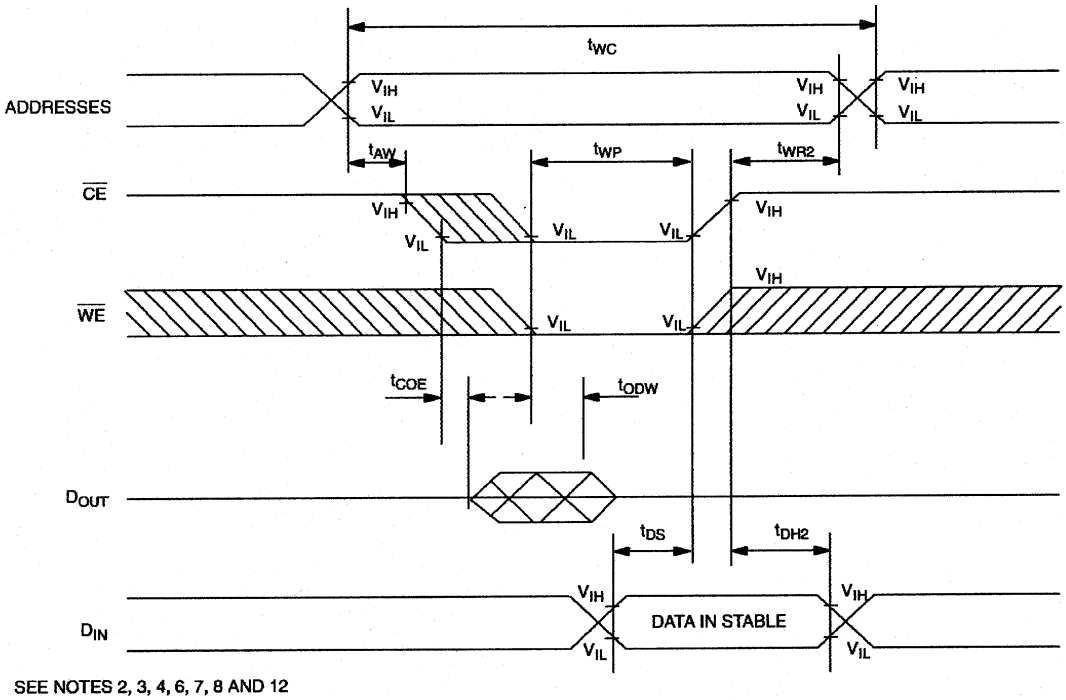


TIMING DIAGRAM: WRITE CYCLE 1 ($\overline{WE}$ Controlled)



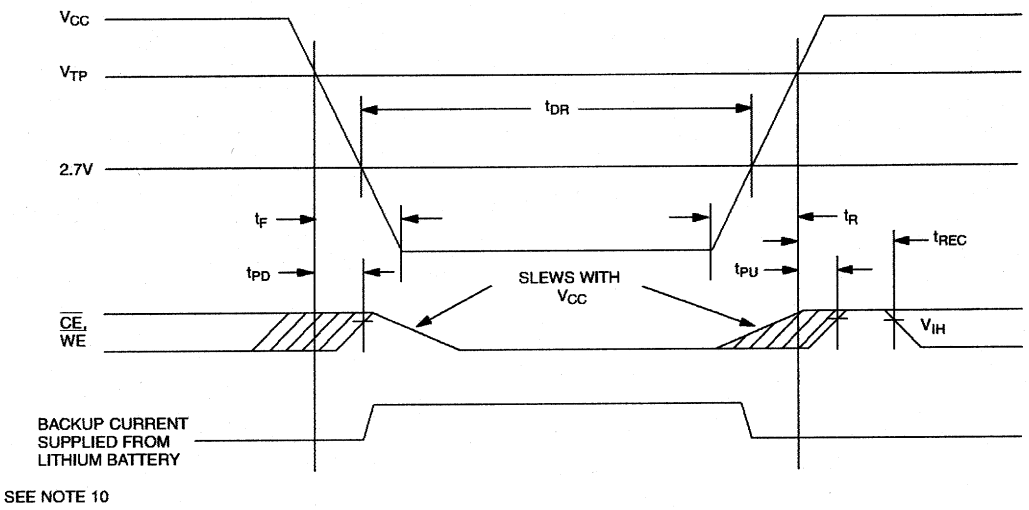
SEE NOTES 2, 3, 4, 6, 7, 8 AND 11

TIMING DIAGRAM: WRITE CYCLE 2 ($\overline{CE}$ Controlled)



SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

TIMING DIAGRAM: POWER-DOWN AND POWER-UP



POWER-DOWN AND POWER-UP TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PD}			1.5	µs	
V_{CC} Slew from V_{TP} to 0V	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP}	t_R	300			µs	
V_{CC} Valid to $\overline{CE}$ and $\overline{WE}$ Inactive	t_{PU}			2	ms	
V_{CC} Valid to End of Write Protection	t_{REC}			125	ms	

(T_A = 25ºC)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high throughout read cycle.
2. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = $V_{\overline{IH}}$ during write cycle, the output buffers remain in a high impedance state.

3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS3803 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. In a power-down condition the voltage on any pin may not exceed the voltage on V_{CC}.
11. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
12. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.

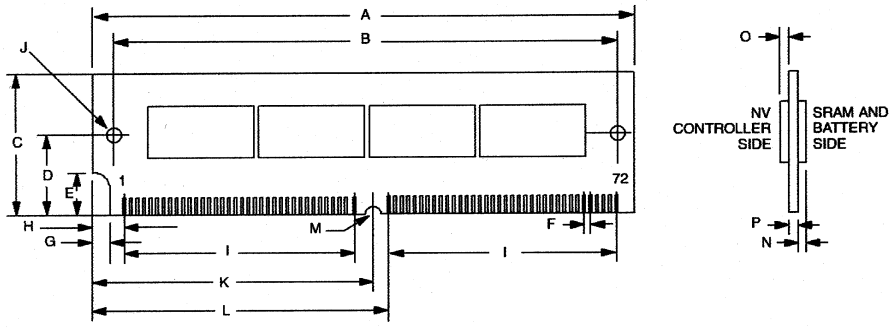
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All Voltages are Referenced to Ground

AC TEST CONDITIONS

Output Load: 100 pF + 1TTL gate
Input Pulse Levels: 0 - 3.0 V
Timing Measurements Reference Levels:
Input - 1.5V
Output - 1.5V
Input Pulse Rise and Fall Times: 5 ns

DS3803 72-PIN SIMM MODULE



DIM	72-PIN	
	MIN	MAX
A	4.245	4.255
B	3.979	3.989
C	0.845	0.855
D	0.395	0.405
E	0.245	0.255
F	0.050 BASIC	
G	0.075	0.085
H	0.245	0.255
I	1.750 BASIC	
J	0.120	0.130
K	2.120	2.130
L	2.245	2.255
M	0.057	0.067
N	-	0.173
O	-	0.110
P	0.047	0.054