NEW

DATEL

6-Bit Video Flash A/D Converter ADC-833

FEATURES

- 6 Bits at 15 MHz
- 200 mW Power Dissipation
- ± ½ LSB Linearity
- Three-State Outputs
- Single Supply Operation
- Internal Zener Reference

GENERAL DESCRIPTION

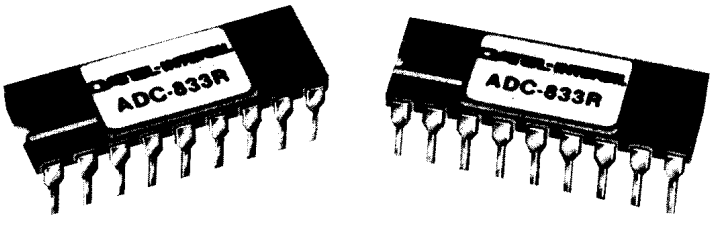
Datel-Intersil's ADC-833 is a video speed, low power, 6 bit flash A/D converter manufactured with CMOS/SOS technology. The ADC-833 is capable of digitizing an analog input signal at conversion rates up to 15 MHz while its power consumption is only 200 mW.

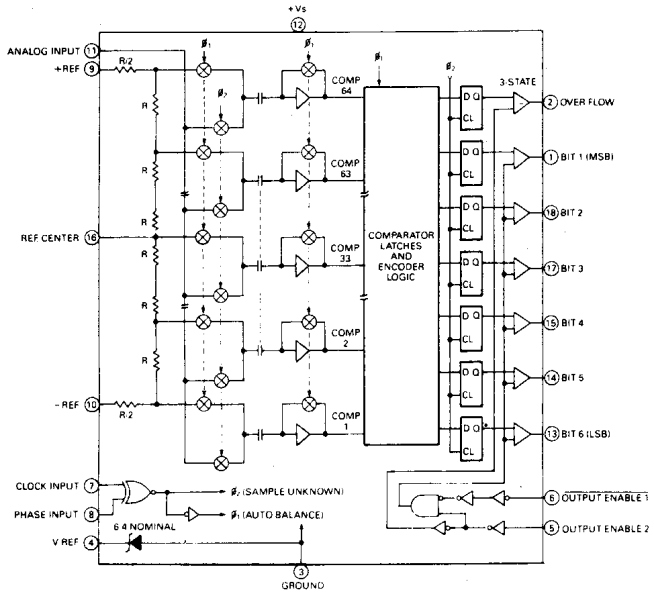
The ADC-833 consists of 64 autobalanced comparators, a resistor ladder network, a zener reference diode, a decoder and seven buffer storage registers. A sequential parallel technique is employed to achieve the high conversion speed, making possible a complete analog to digital conversion in one clock cycle. The analog input voltage range is +2.5V to +10V, and typical differential linearity error is only ± ½ LSB. All digital inputs and outputs are TTL/CMOS compatible.

Outputs are buffered three-state and include an overflow output which allows the user to cascade two units to achieve 7-bit resolution. The buffers are controlled by two enable signals with a typical output enable delay of only 20 nsec. A phase input is provided to allow the user to effectively complement the clock and an onboard 6.4V zener diode is provided for use as a reference voltage.

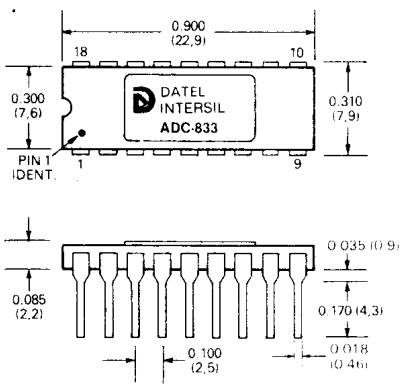
The ADC-833 is ideally suited for applications that require high-speed digitization and low power consumption. Such applications would include CRT graphics, radar pulse analysis, motion signature analysis and optical character recognition.

The ADC-833 is packaged in an 18 pin ceramic DIP and operates over the −25°C to +85°C industrial temperature range.





MECHANICAL DIMENSIONS



INPUT/OUTPUT

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 OUT (MSB)	10	— REFERENCE
2	OVER FLOW OUT	11	ANALOG INPUT
3	GROUND	12	V SUPPLY
4	REFERENCE ZENER	13	BIT 6 OUT (LSB)
5	OUTPUT ENABLE 2	14	BIT 5 OUT
6	OUTPUT ENABLE 1	15	BIT 4 OUT
7	CLOCK INPUT	16	REFERENCE CENTER
8	PHASE INPUT	17	BIT 3 OUT
9	+ REFERENCE	18	BIT 2 OUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-833

Typical at +25°C, V_S = +5 VDC unless otherwise noted.

MAXIMUM RATINGS	
Supply Voltage	−0.5V to +10V
Analog Inputs[1]	−0.5V to (+V_S +0.5V)
Logic Inputs	−0.5V to (+V_S +0.5V)
Input Current, D.C.	±10 mA
Package Dissipation[2]	315 mW
INPUTS	
Analog Input Range	+2.5V to +10V
Analog Input Current, max.	1 mA
Ladder Impedance	1.4kΩ
Input Capacitance	50 pF
Input Logic Level, Vin ("1"), min.[3]	+3.0 V
Input Logic Level, Vin ("0"), max.[4]	+1.5 V
OUTPUTS	
Parallel Output Data	6 parallel lines of data & overflow
Output Logic Level, Vout ("1"),[5]	+4.6 V @ −0.8 mA min.
Output Logic Level, Vout ("0"),[6]	+0.4V @ 1.6 mA min.
Zener Reference, Voltage[7]	6.4 V
Impedance,[7] max.	30 Ω
PERFORMANCE	
Resolution	6 bits
Conversion Speed, min[8]	15 MHz
Nonlinearity, max[9]	±0.8 LSB
Differential Linearity Error, max.[9]	±0.8 LSB
Quantizing Error	±½ LSB
Aperture Time[10]	25 nsec
Output Enable Delay[10]	20 nsec
Gain Tempco[11]	25 ppm/°C
Zener Reference Tempco	±0.5 mV/°C
POWER REQUIREMENT	
Analog Supply Voltage Range	+3V to +10V
Quiescent Current,[12] V_S = +5V	7 mA
V_S = +8V	22 mA
Power Dissipation, V_S = +8V	200 mW
PHYSICAL—ENVIRONMENTAL	
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Type	18 pin ceramic DIP

NOTES:

1. All inputs except Zener Ref. (Pin 4).
2. Specified for T_A = −25°C to +55°C. For T_A = +55°C to +85°C, derate linearly at 3.3 mW/°C.
3. At V_S = +8V, the minimum Input Logic Level, V_{IN} ("1") is +5.5V.
4. At V_S = +8V, the maximum Input Logic Level, V_{IN} ("0") is +2.5V.
5. At V_S = +8V, the Output Logic Level, V_{out} ("1") is 7.5V @ −1.6 mA min.
6. At V_S = +8V, the Output Logic Level, V_{out} ("0") is 0.5V @ 3.2 mA min.
7. Specified at I_Z = 10 mA.
8. Specified at V_S = +8V. At V_S = +5V, the typical sampling rate is 12 MHz.
9. Specified at V_S = +8V, V_{ref} = +7.68V, clk = 15 MHz, with gain adjusted.
10. Specified at V_S = +8V. The aperture time specification for an A/D converter refers to the time uncertainty of the exact instant that the sample is taken at the analog input.
11. Specified at V_S = +8V, clk = 15 MHz.
12. Does not include Zener current and reference ladder current. Specified at V_S = +5V with an 11 MHz clock, at V_S = +8V with a 15 MHz clock. If the clock is held in the "Auto Zero" state, the maximum quiescent current at V_S = +5V is 16 mA, at V_S = +8V, the maximum is 40 ma.

ORDERING INFORMATION

MODEL NO	OPERATING TEMPERATURE RANGE	PRICE (1-24)
ADC-833R	−25°C to +85°C	

TECHNICAL NOTES

1. These are CMOS devices and may be damaged by electrostatic discharge. All inputs and outputs of the ADC-833 have a network for electrostatic protection, however, standard anti-static precaution should be taken to prevent possible damage. To prevent damage to the input protection circuit, input signals should not exceed V_S nor be less than the ground potential on Pin 3. Input currents must not exceed 10 mA even when the power supply is off. All unused input terminals must be grounded or connected to V_S, whichever is appropriate.

2. The ADC-833 may be operated in a pulse mode when sampling high speed nonrecurrent or transient data. The fastest method is to keep the converter in the Sample Unknown phase, Ø2 (see operating theory) during the standby state. The converter can be pulsed through the Auto Balance phase, Ø1, in as little as 33 nsec. The analog input is taken on the leading edge of Ø1 and transferred into the output registers on the trailing edge of Ø1, putting the converter back in the standby state. Another conversion can be started within 33 nsec, but no later than 10 μsec due to the eventual droop of the commutating capacitors. The larger the time ratio between Ø1 and Ø2, the lower the power consumption.

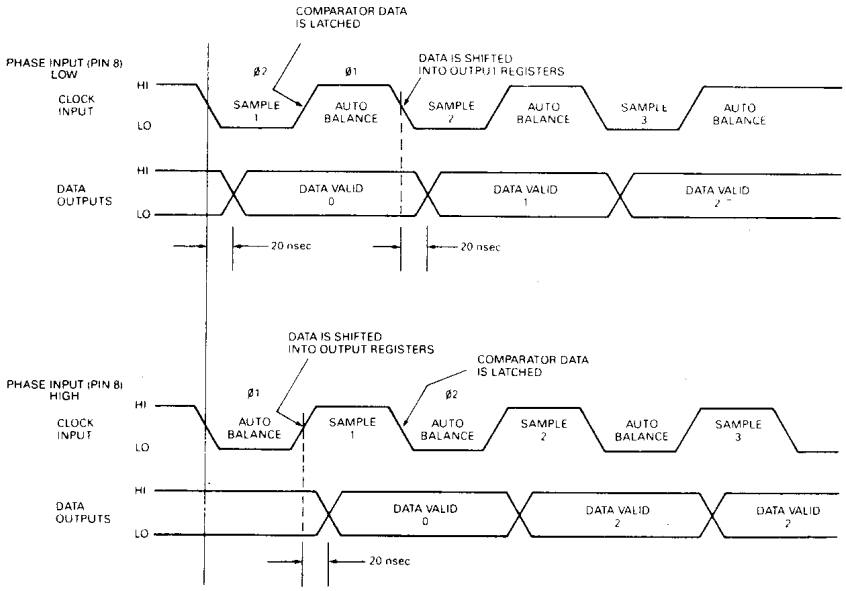
3. For most applications, the accuracy of the ADC-833 should be sufficient without external adjustment. However, where accuracy is of paramount importance, three adjustments can be made; Offset Trim, Gain Trim, and Midpoint Trim.

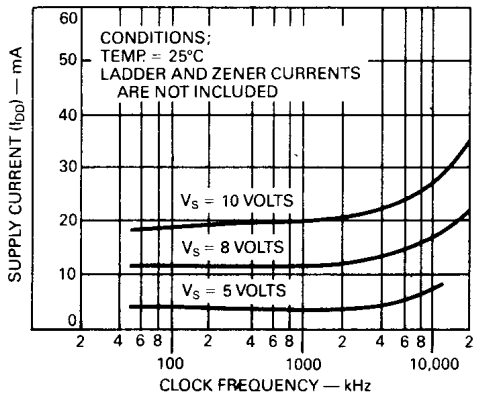
   The offset may be adjusted in the preamp circuitry by introducing a DC shift to the analog input. If this is not possible, the -Ref. pin (pin 10) can be adjusted to set the first transition at its theoretical value, -Vref/128. If the transition is lower than the theoretical, then a single turn 50Ω pot connected between -Ref. and ground will accomplish the adjustment. If the transition is greater than the theoretical, the 50Ω pot should be connected between -Ref. and a negative voltage equal to approximately two LSB's.

   The gain may also be adjusted in the preamp circuitry. The gain can be adjusted at the converter by making an adjustment to the reference voltage. To adjust the gain, first set the offset trim then set the input voltage to the value Vref (127/128). Now adjust Vref until that transition occurs on the output.

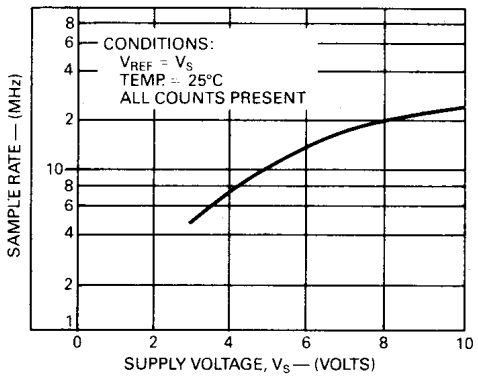
   The midpoint trim should be done after the gain and offset trims. The theoretical input voltage for the half scale transition is 32.5 (Vref/64). A 2 kΩ pot may be connected between + Ref (pin 9) and - Ref (pin 10) with the wiper connected to Ref. center (pin 16). Set Vin to the theoretical half scale voltage and adjust the output for that transition.

TIMING DIAGRAM

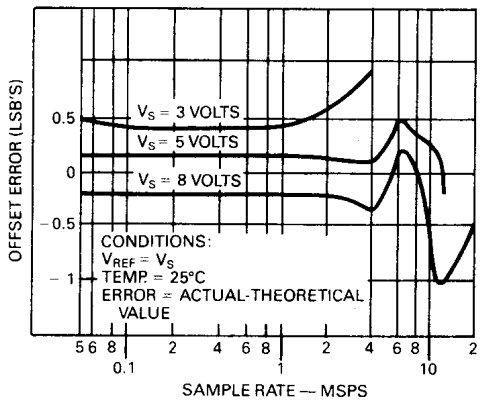




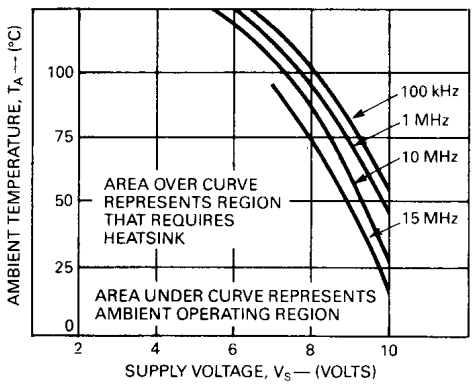
Typical current drain versus sampling rate as a function of supply voltage.



Typical maximum sample rate versus supply voltage.

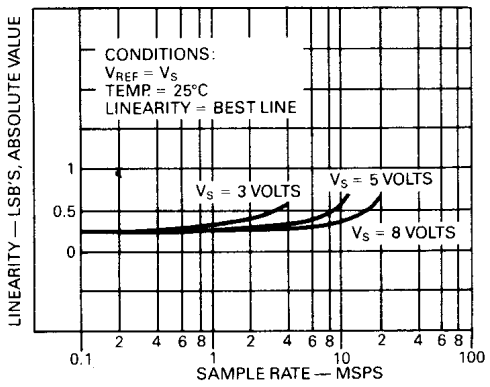


Typical offset error versus sample rate as a function of supply voltage.

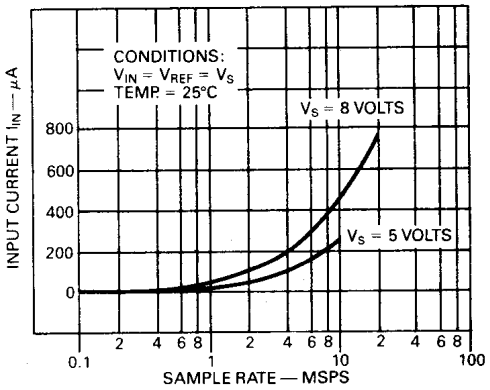


Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)

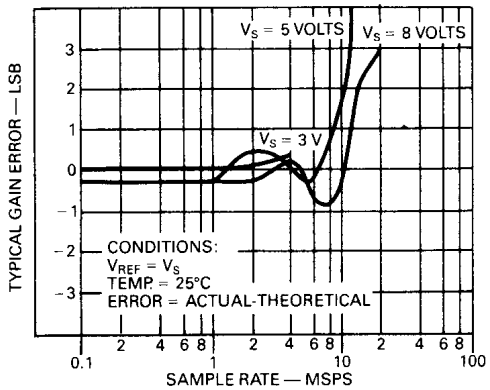
PERFORMANCE



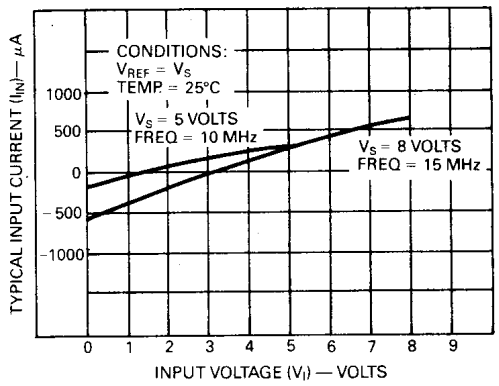
Typical linearity versus sample rate as a function of supply voltage.



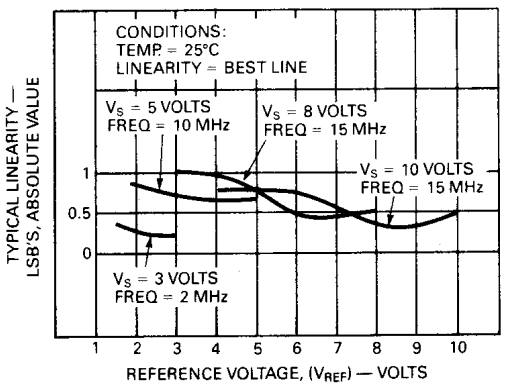
Typical input current versus sample rate as a function of supply voltage.



Typical gain error versus sample rate as a function of supply voltage.

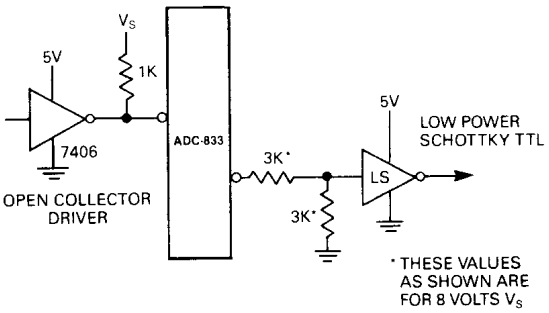


Typical input current versus input voltage as a function of supply voltage.



Typical linearity versus reference voltage as a function of supply voltage.

LOGIC INTERFACE CIRCUITS



TTL interface circuit for V_S >5.5 volts.

THEORY OF OPERATION

The ADC-833 employs a sequential parallel technique, consisting of an "Auto Balance" phase (Ø1) and a "Sample Unknown" phase (Ø2), to achieve its high speed operation. Each conversion takes one clock cycle. With the phase input low (Pin 8), "Auto Balance" (Ø1) occurs during the high period of the clock cycle, and "Sample Unknown" (Ø2) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, 64 commutating capacitors are connected to their associated ladder reference tap through a transmission switch. The tap voltage is equal to V_{tap} (N) = V_{ref} (2N – 1)/128, where: V_{tap} (N) equals the reference ladder tap voltage at point N; V_{ref} equals the voltage across + Ref. (Pin 9) to – Ref. (Pin 10); and N equals the tap number.

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input. The amplifier is biased at its intrinsic trip point, approximately $V_S/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, the ladder tap switches are opened, the comparator amplifiers are no longer shorted, and the analog input (Pin 11) is switched to all 64 capacitors. With the other end of the capacitor looking into what is effectively an open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparators. All comparators with tap voltages greater than the analog input will have a "low" output, comparators with a tap voltage lower than the analog input will have a "high" output.

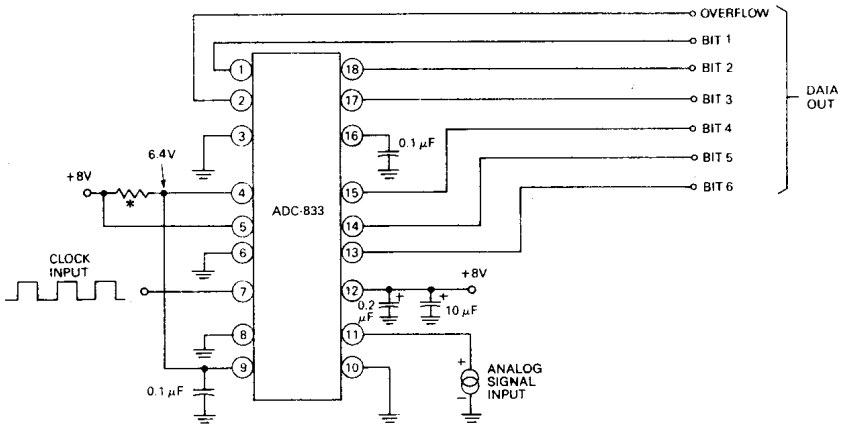
The comparator outputs are stored at the end of the "Sample Unknown" phase by secondary latching amplifiers. Once latched, the outputs are decoded by a 64 to 7 decode array and the result is clocked into a storage register on the rising edge of the next "Sample Unknown" phase.

A three-state buffer is used at the output of the storage registers. The buffer is controlled by two enable signals. Output Enable 1 (Pin 6) will disable Bit 1 through Bit 6 when it is in a high state, Output Enable 2 (Pin 5) will disable Bit 1 through Bit 6 and the overflow output when it is in a low state.

A phase input (Pin 8) is provided to allow the user to effectively complement the clock and an onboard zener is provided for use as a reference voltage.

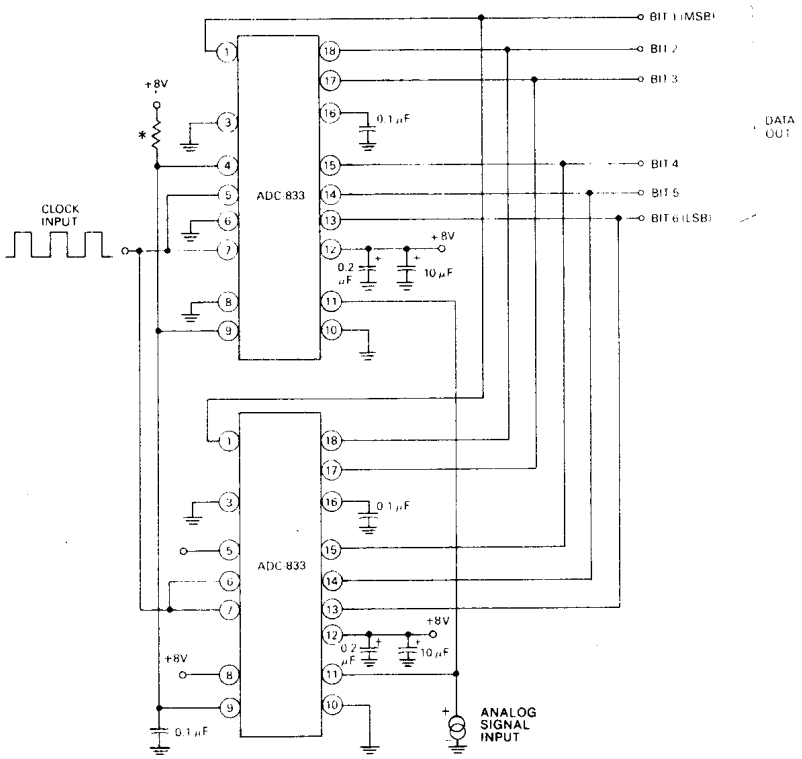
CONNECTION AND APPLICATION

TYPICAL CONNECTION - 6 BITS AT 15 MHz



* RESISTOR MUST BE SELECTED TO PROVIDE A ZENER CURRENT OF 10 mA.

TYPICAL CONNECTION - 6 BITS AT 30 MHz

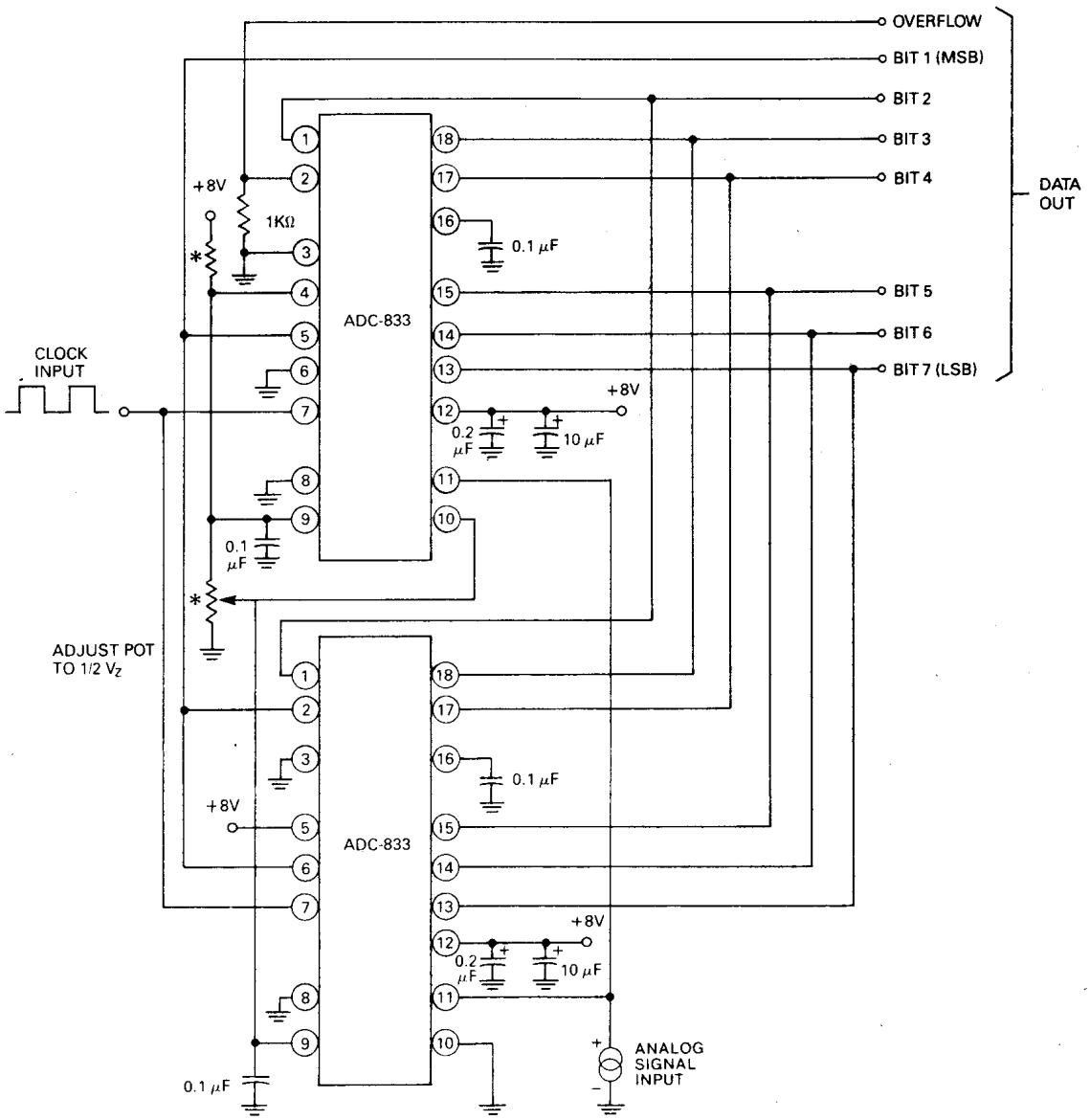


Two ADC-833's may be connected in parallel to increase the conversion speed from 15 MHz to 30 MHz.

* RESISTOR MUST BE SELECTED TO PROVIDE A ZENER CURRENT OF 10 mA.

CONNECTION AND APPLICATION

TYPICAL CONNECTION - 7 BIT RESOLUTION



*RESISTORS MUST BE SELECTED TO PROVIDE A ZENER CURRENT OF 10mA

Two ADC-833's may be connected in series to produce a high speed 7 bit converter. First, the ladder networks are totem-poled. Since the absolute resistance value of each ladder may vary, an external mid-reference voltage trim may be required. The overflow output of the lower device now becomes Bit 7. When it goes high, all counts must come from the upper device, when it goes low, all counts come from the lower device. The three-state outputs of the two devices are connected in parallel to complete the circuit.