

C-Media CMI9761A / 9761A+ 6 Channel AC'97 2.3 Audio Codec

DataSheet, Revision 1.2

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0. Revision History

2003/06/23	Rev 1.0	Initial revision
2003/08/26	Rev 1.1	Fixed some typos.
2004/02/09	Rev 1.2	Change datasheet title for both CMI9761A & 9761A+

1. Product Summary

Product	Dolby® Digital real-time Interactive Content Encoder (DDICE)
9761A+	Yes
9761A	N/A

2. Features

Basic features:

- 6 channel, 16-bits DACs with SNR > 90 dB.
- 2 channel, 16-bits ADCs with SNR > 85 dB.

New features of AC'97 2.3 codec:

- Digital PC Beep support.
- 2 Stereo microphone support.
- Extensive jack detection via proprietary resistors network method that can monitor plugging status of every jack.
- Precise advanced impedance sensing function for audio device class discoverability.

Miscellaneous features:

- Compliant with Intel® AC'97 Rev 2.3 Spec.
- Meeting with Microsoft® PC2001 requirements
- Built-in 14.318MHz to 24.576MHz PLL, which can save the BOM cost of external crystal.
- Advanced power management and power saving capabilities.
- Industry standard 48-lead LQFP package.
- Analog power supply is 5V, digital power supply is 3.3V.

Versatile I/O & functionalities support:

- Stereo Line-in function shared with Surround out.
- Stereo Microphone function shared with Center/LFE out.
- High quality pseudo-differential analog CD Audio input.
- Dual analog & digital PC BEEP support.
- AUX legacy analog I/O support.
- 2 GPIO (General Purpose I/O) support.
- EAPD (External Amplifier Power Down) support.
- S/PDIF I/O function:
Output: 96 / 48 kHz with 24 / 20 / 16 bits
Input: 48 / 44.1 / 32 kHz with 20 / 16 bits
S/PDIF In is featured with interrupt, auto-lock, anti-noise, and anti-distortion functionalities support.

Valuable add-on software technology:

- CMI9761A+ supports Dolby® Digital Interactive Content Encoder (DDICE) for easy-connection with consumer acoustics as media center/game console applications
- Xear3D™ sound support, including Earphone Plus and 5.1CH SPEAKER SHIFTER.
- Sensaura® HRTF 3D positional sound support.
-
- Support most industry standards of PC 3D sound for gaming, including Creative EAX™ 2.0 / 1.0 , Microsoft DirectSound™ 3D, A3D™ 1.0 and more.
- Unique karaoke function support featured with microphone echo, key shifting, and vocal cancellation.
- 10-band equalizer with 12 pre-set settings.
- 27 kinds of listening environments support together with 3 kinds of room sizes emulation.
- Dynamic AGC(auto-gain control) technology.

3. Overview

C-Media CMI9761A/9761A+ is a 6 channel, Intel® AC'97 rev 2.3 compliant audio codec. The applicable M/B chipsets are extensive, including Intel® ICHx series as well as those supplied by SiS®, VIA®, Ali®, and nVidia®. The excellent audio quality (A/A SNR > 90dB) makes CMI9761A/9761A+ ideal for designing Microsoft® PC2001 compliant PC multimedia desktops and notebooks.

The various features implemented within CMI9761A/9761A+ can help users to enjoy the PC audio smoothly without any frustration. The most important of all is jack detection & impedance sensing that can minimize user's intervention and try-and-error during setup. There are also creative applications such as automatically enabling pre-defined equalization for different audio devices. With precise advanced sensing technology, CMI9761A/9761A+ can determine most device classes without miss. CMI9761A/9761A+ can make a fantastic impression on end users and also reduce the cost of support for setup of audio environment. The digital PC Beep support can further improve the quality of analog output by eliminating the traditional noisy analog PC Beep.

The S/PDIF out function makes connection easily from PC to CE products, such as AC3/DTS decoder or Minidisk. The 96 kHz / 24 bits S/PDIF output capability of CMI9761A/9761A+ can easily distribute the premium-quality stereo PCM audio to CE equipments. Combining with value add-on software such as Xear3D™ technology, CMI9761A/9761A+ is able to fulfill the most rigid requirements of audiophiles. Not to mention, CMI9761A/9761A+ can transmit DVD industry standard multi-channel Dolby® Digital audio stream to external decoder utilizing S/PDIF link and enjoy the Home Theater concept.

The built-in PLL and earphone buffer can help our customers to save the BOM cost and create a cost-effective end product. Together with the flexible shared audio function design and dedicated multi-channel output, the design of end products can be as versatile and creative as

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4. Pin Assignment

PIN #	Signal Name	PIN #	Signal Name
1	DVDD1	25	AVDD1
2	XTL_IN	26	AVSS1
3	XTL_OUT	27	VREF
4	DVSS1	28	VRO1
5	SDATA_OUT	29	VRO2
6	BIT_CLK	30	NC
7	DVSS2	31	NC
8	SDATA_IN	32	NC
9	DVDD2	33	FMIC_R
10	SYNC	34	FMIC_L
11	RESET#	35	LINEOUT_L
12	PCBEEP	36	LINEOUT_R
13	SENSE B	37	EXT_R
14	AUX_L	38	AVDD2
15	AUX_R	39	REAROUT_L
16	NC	40	SENSE A
17	NC	41	REAROUT_R
18	CD_L	42	AVSS2
19	CD_C	43	CENTER_OUT
20	CD_R	44	LFE_OUT
21	MIC1	45	HP_ON / GPIO0
22	MIC2	46	XTLSEL / GPIO1
23	LINE_IN_L	47	EAPD / SPDIFI
24	LINE_IN_R	48	SPDIFO

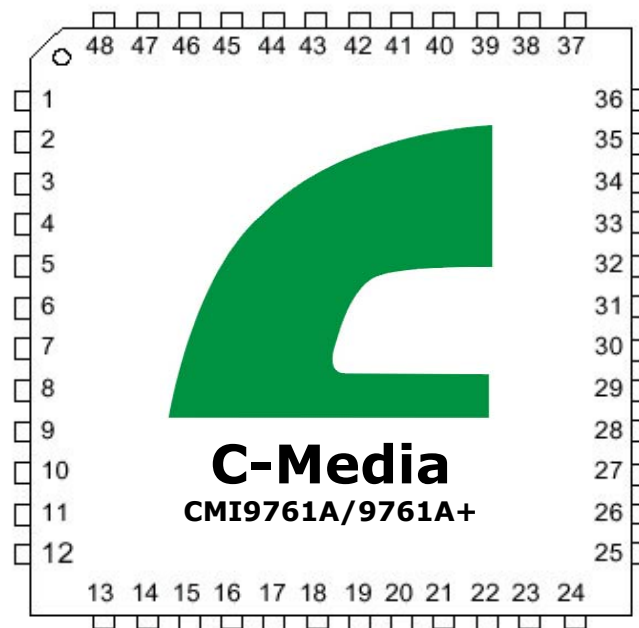


Figure 1. Pin Assignment

5. Pin / Signal Descriptions

5.1 Power / Ground

The digital portion of CMI9761A/9761A+ operates at 3.3V and the analog portion operates at 5V. The grounds should be separated well to assure the best analog audio quality.

Pin No	Signal Name	Type	Description
1	DVDD1	I	Digital VDD (3.3V)
4	DVSS1	I	Digital ground
7	DVSS2	I	Digital ground
9	DVDD2	I	Digital VDD (3.3V)
25	AVDD1	I	Analog VDD (5V)
26	AVSS1	I	Analog ground
38	AVDD2	I	Analog VDD (5V)
42	AVSS2	I	Analog ground

5.2 AC-Link / Clocking

These signals connect CMI9761A/9761A+ to its AC'97 controller counterpart and external crystal / oscillator clock source.

Pin No	Signal Name	Type	Description
2	XTL_IN	I	24.576 MHz crystal input or 14.318 MHz oscillator input
3	XTL_OUT	O	24.576 MHz crystal output or NC (for 14.318 MHz oscillator input)
5	SDATA_OUT	I	Serial, time division multiplexed, input stream from the AC'97 controller.
6	BIT_CLK	O	12.288 MHz bit clock output
8	SDATA_IN	O	Serial, time division multiplexed, output stream to the AC'97 controller.
10	SYNC	I	48 kHz sample sync
11	RESET#	I	AC'97 master H/W reset

Note: # denotes active low

5.3 Digital I/O

These signals are digital inputs and outputs of CMI9761A/9761A+ that includes S/PDIF I/O and GPIO.

Pin No	Signal Name	Type	Description
45	HP_ON/GPIO0	I/O	Headphone ON detection / General Purpose I/O #0
46	XTLSEL/GPIO1	I/O	Clock source selection / General Purpose I/O #1
47	EAPD/SPDIFI	I/O	External Amplifier Power Down or S/PDIF input
48	SPDIFO	O	S/PDIF output

5.4 Analog I/O

These signals connect CMI9761A/9761A+ to analog sources and sinks, including microphones and speakers.

Pin No	Signal Name	Type	Description
12	PCBEEP	I	Analog PCBEEP input
14	AUX_IN_L	I	Aux input left channel
15	AUX_IN_R	I	Aux input right channel
18	CD_L	I	CD audio input left channel
19	CD_C	I	CD audio common channel
20	CD_R	I	CD audio input right channel
21	MIC1	I/O	Stereo microphone left channel / Alternative center channel output
22	MIC2	I/O	Stereo microphone right channel / Alternative LFE channel output
23	LINE_IN_L	I/O	Line-In input left channel / Alternative rear output left channel
24	LINE_IN_R	I/O	Line-In input right channel / Alternative rear output right channel
33	FMIC_R	I	Front panel stereo microphone right channel
34	FMIC_L	I	Front panel stereo microphone left channel
35	LINEOUT_L	O	Line output left channel
36	LINEOUT_R	O	Line output right channel
39	REAROUT_L	O	Dedicated rear output left channel

Pin No	Signal Name	Type	Description
41	REAROUT_R	O	Dedicated rear output right channel
43	CENTER_OUT	O	Dedicated center output channel
44	LFE_OUT	O	Dedicated LFE output channel

5.5 Filter / Reference

These signals of CMI9761A/9761A+ connected to resistors or capacitors.

Pin No	Signal Name	Type	Description
27	VREF	O	Reference voltage
28	VRO1	O	Reference voltage out for MIC2 bias
29	VRO2	O	Reference voltage out for MIC1 bias
37	EXT_R	O	External 1K Ω precision resistor calibration for impedance sensing

5.6 Configuration

These pins utilize C-Media proprietary parallel resistors method for jack detection.

Pin No	Signal Name	Type	Description
13	Sense B	I	Sensing pin B
40	Sense A	I	Sensing pin A

Note: For detailed information, please refer to Sec. 5.1 to facilitate the implementation of resistors network.

6. Jack Detection and Configuration Information

In this section, we describe the resistors network method for jack detection and configuration identification. And also, due to the design of CMI9761A/9761A+ with shared audio function and dedicated multi-channel output, the configuration of audio system can be as versatile as possible.

6.1 Resistors Network Method

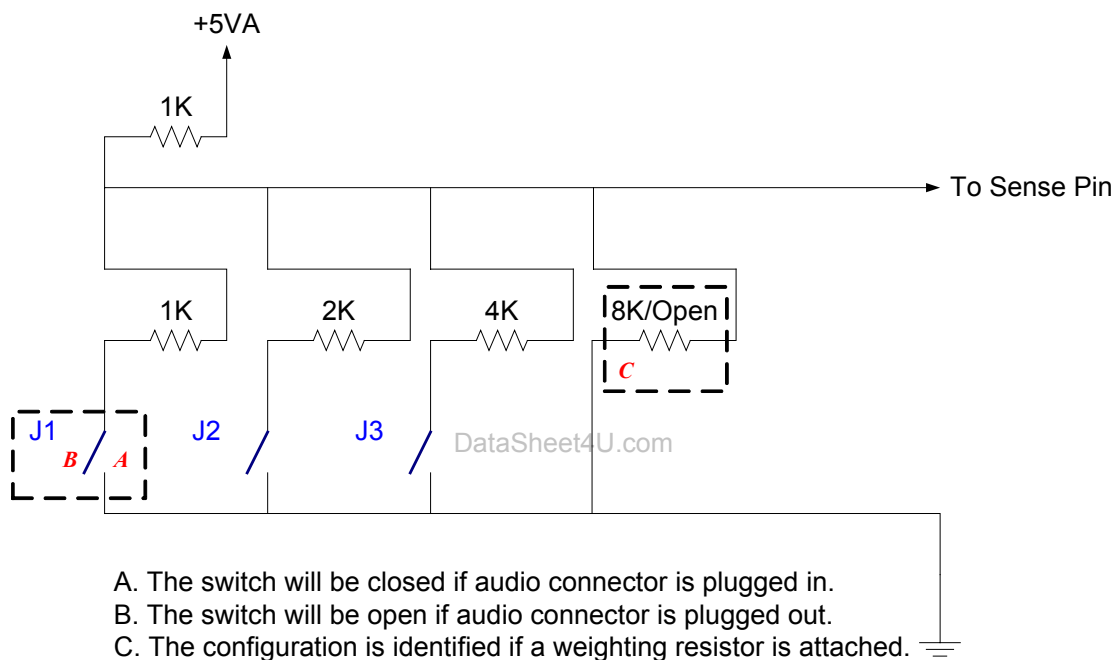


Figure 2. Resistors Network Method for Jack Detection

The sense pin connects to an ADC internally to measure the resistance of the network. CMI9761A/9761A+ is able to monitor the plugging status of each jack according to the resistance measured. To obtain a correct result, the value of each precision resistor should not be modified from the specified schematics provided by C-Media for any reason.

6.2 Configuration Diagram

C-Media CMI9761A - Recommended Configuration Diagram

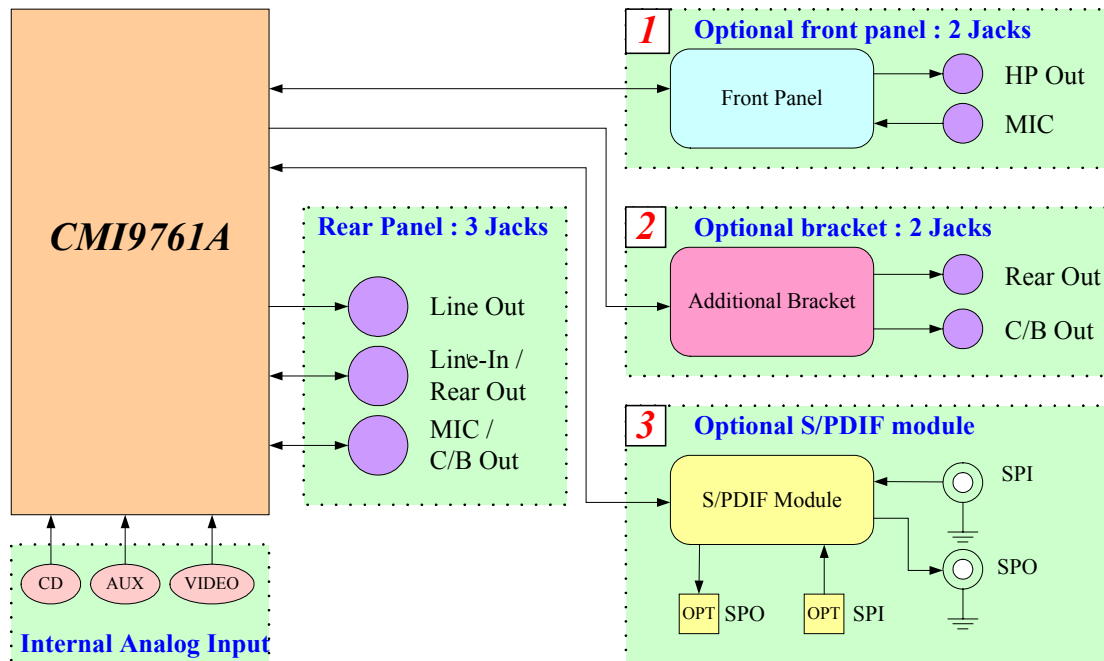


Figure 3. Recommended Configuration Diagram

7. DC Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Digital power supply	DVdd	3.135	3.3	3.465	V
Input voltage range	V_{in}	-0.30	-	DVdd+0.3	V
Low level input voltage	V_{il}	-	-	0.35xDVdd	V
High level input voltage	V_{ih}	0.65xDVdd	-	-	V
High level output voltage	V_{oh}	0.90xDVdd	-	-	V
Low level output voltage	V_{ol}	-	-	0.10xDVdd	V
Input leakage current (AC-Link inputs)	-	-10	-	10	μ A
Output leakage current (Hi-Z'd AC-Link outputs)	-	-10	-	10	μ A
Input/Output Pin Capacitance	-	-	-	7.5	pF

8. AC-Link Timing Characteristics

8.1 Cold Reset Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	μs
REEST# inactive to SDATA_IN or BIT_CLK active delay	$T_{tri2actv}$	-	-	25	ns
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns
BITCLK active to RESET# asserted	$T_{clk2rst}$	0.416	-	-	μs

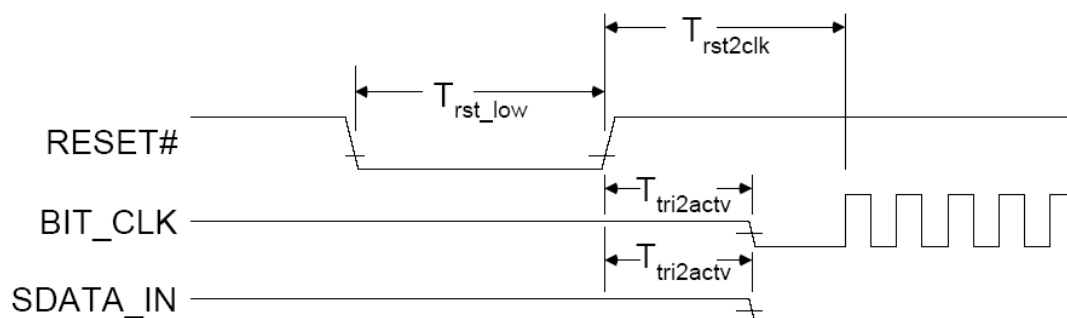


Figure 4. Cold Reset Timing Diagram

8.2 Warm Reset Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	μs
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns

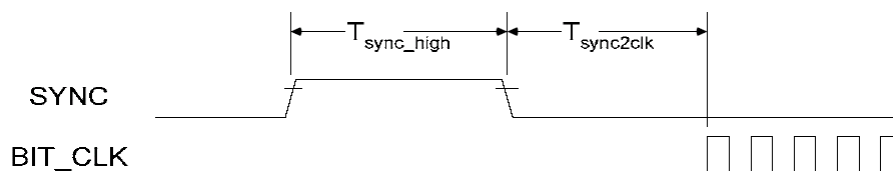


Figure 5. Warm Reset Timing Diagram

8.3 AC-Link Clocks

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750.0	ps
BLT_CLK high pulse width (note 1)	T_{clk_high}	36.0	40.7	45.0	ns
BIT_CLK low pulse width (note 1)	T_{clk_low}	36.0	40.7	45.0	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	μ s
SYNC high pulse width	T_{sync_high}	-	1.3	-	μ s
SYNC low_pulse width	T_{sync_low}	-	19.5	-	μ s

Note 1: Worse case duty cycle restricted to 45/55.

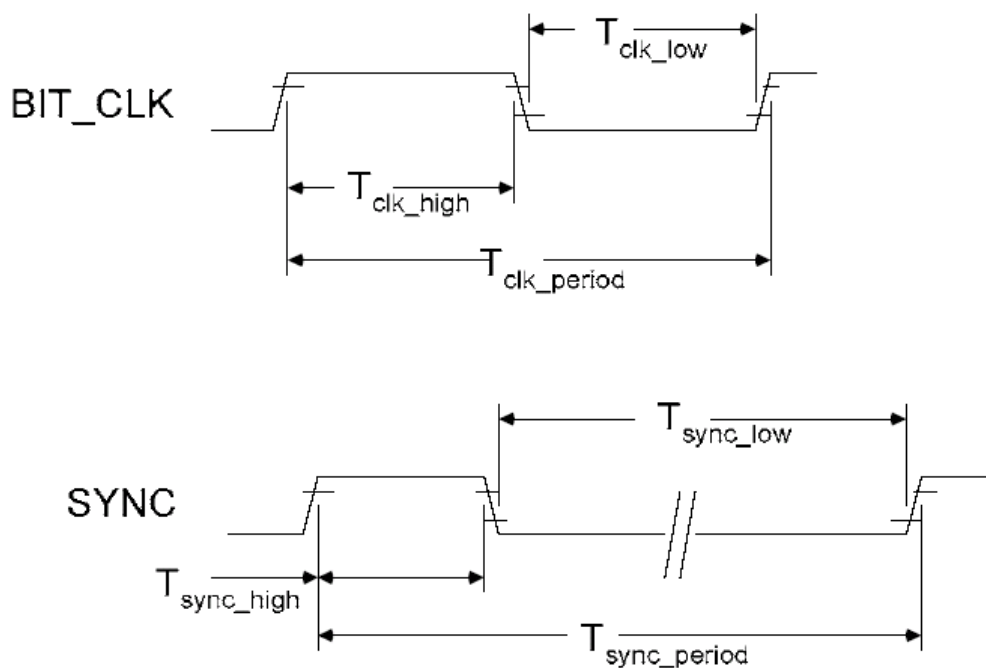


Figure 6. BIT_CLK and SYNC Timing Diagram

8.4 Data Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output valid delay from rising edge of BIT_CLK	T_{co}	-	-	15.0	ns

Note: 50pF external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup to falling edge of BIT_CLK	T_{setup}	10.0	-	-	ns
Input Hold from falling edge of BIT_CLK	T_{hold}	10.0	-	-	ns

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK combined rise or fall plus flight time	-	-	-	7.0	ns
SDATA combined rise or fall plus flight time	-	-	-	7.0	ns

Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.

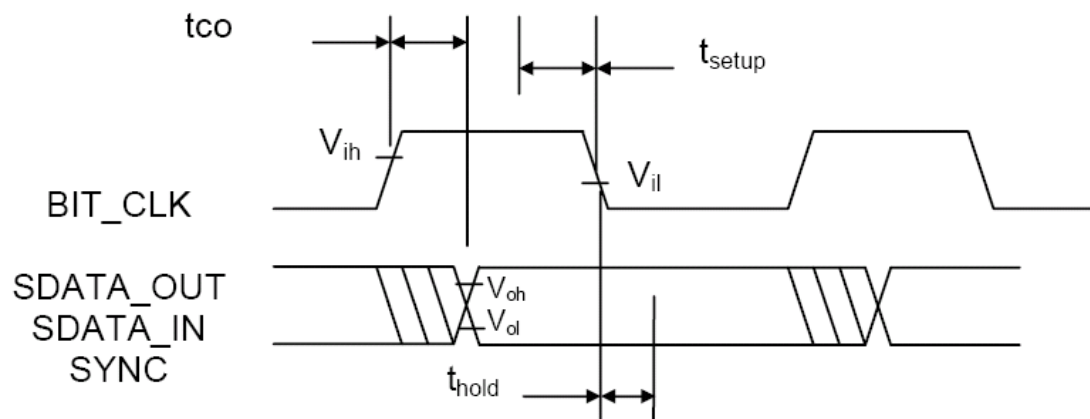


Figure 7. Data Output and Input Timing Diagram

8.5 Signal Rise and Fall Timing

The rise time is from 10% to 90% of VDD (V_{ol} to V_{oh}). The fall time is from 90% to 10% of VDD (V_{oh} to V_{ol}).

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK rise time (note 1)	$T_{rise_{clk}}$	-	-	6.0	ns
BIT_CLK fall time (note 1)	$T_{fall_{clk}}$	-	-	6.0	ns
SYNC rise time (note 1)	$T_{rise_{sync}}$	-	-	6.0	ns
SYNC fall time (note 1)	$T_{fall_{sync}}$	-	-	6.0	ns
SDATA_IN rise time (note 2)	$T_{rise_{din}}$	-	-	6.0	ns
SDATA_IN fall time (note 2)	$T_{fall_{din}}$	-	-	6.0	ns
SDATA_OUT rise time (note 1)	$T_{rise_{dout}}$	-	-	6.0	ns
SDATA_OUT fall time (note 1)	$T_{fall_{dout}}$	-	-	6.0	ns

Note 1: 75pF external load

Note 2: 60pF external load

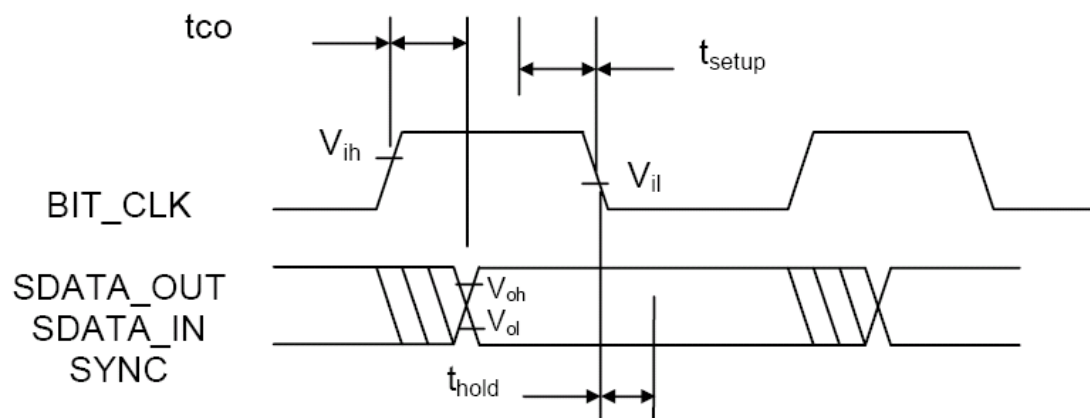


Figure 8. Signal Rise and Fall Timing Diagram

8.6 AC-Link Low Power Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	μs

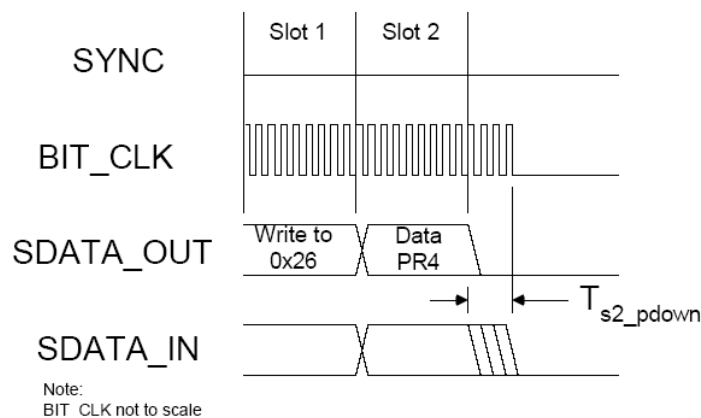


Figure 9. AC-Link Low Power Mode Timing Diagram

8.7 ATE Test Mode

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{\text{setup2rst}}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

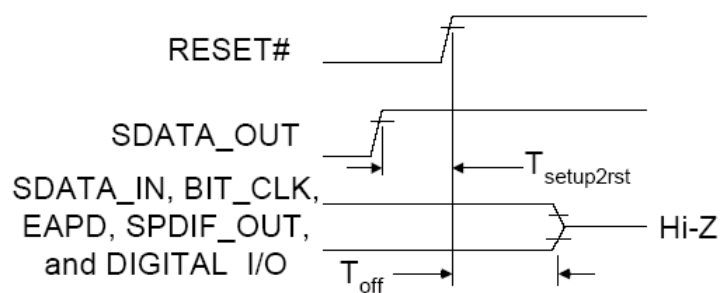


Figure 10. ATE Test Mode Timing Diagram

9. Analog Performance Characteristics

The measurements are performed under the circumstance as:
 $T_{\text{ambient}} = 25^{\circ}\text{C}$, $AV_{\text{dd}} = 5.0\text{V} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{V} \pm 5\%$, $10\text{k}\Omega/50\text{pF}$ external load. Input is 1 kHz sine wave; Sampling frequency = 48 kHz; Bandwidth = 20 to 20 kHz; 0dB attenuation; All sound effects such as 3D effects are disabled.

Parameter	Minimum	Typical	Maximum	Units
Full Scale Input Voltage:				
Line Inputs	-	1.1	1.4	Vrms
Mic Inputs	-	0.1	-	Vrms
Full Scale Output Voltage:				
LINEOUT	-	1.1	1.4	Vrms
REAROUT	-	1.1	-	Vrms
CENTER_OUT / LFE_OUT	-	1.1	-	Vrms
Frequency Response				
A/A	20	-	20,000	Hz
D/A	20	-	20,000	Hz
A/D	20	-	20,000	Hz
Dynamic Range				
A/A	-	96	-	dB
D/A	-	92	-	dB
A/D	-	85	-	dB
SNR				
A/A	-	95	-	dB
D/A	-	92	-	dB
A/D	-	90	-	dB
Total Harmonic Distortion Plus Noise				
A/A	-	92	-	dB
D/A	-	75	-	dB
A/D	-	76	-	dB
Crosstalk between input channels @ 10KHz	-	92	-	dB
Power Supply Current				
AVDD (5.0V)	-	50	-	mA
DVDD (3.3V)	-	10	-	mA
Vrefout	-	2.25	-	V

10. Package Dimension

Dimensions are shown in inches (mm)

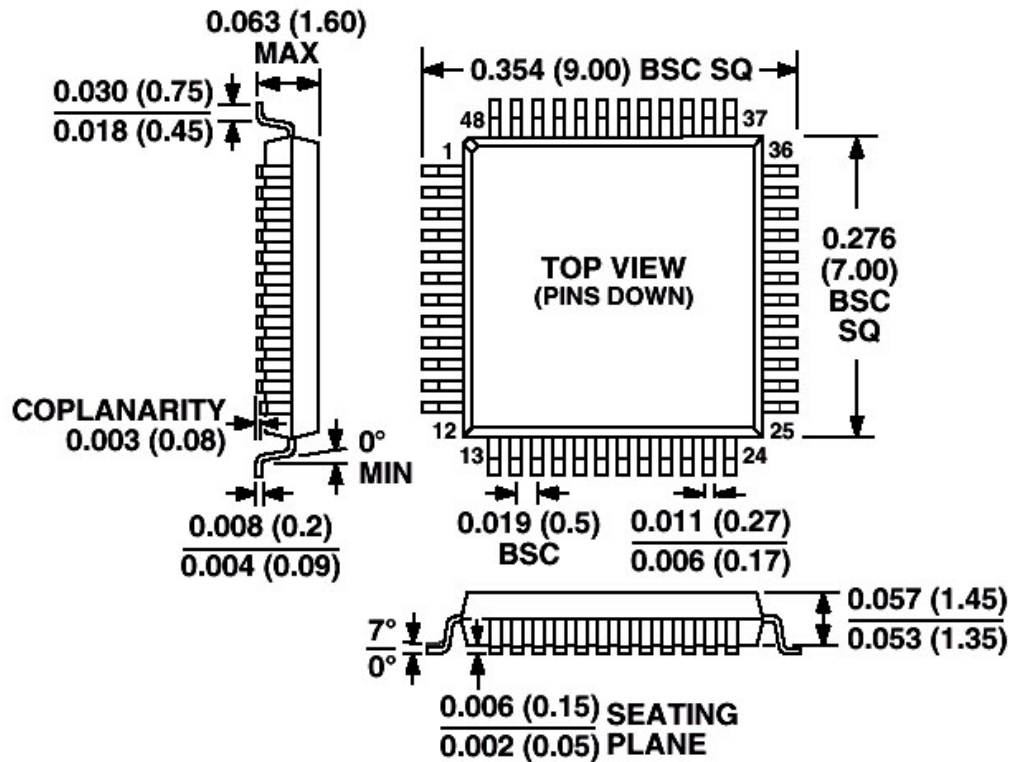


Figure 11. Mechanical Dimension

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