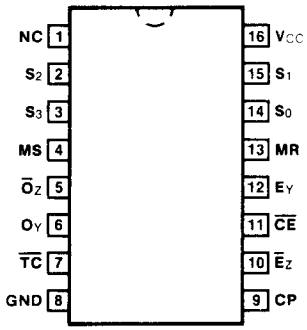
54/74167

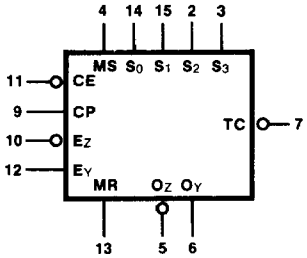
SYNCHRONOUS DECADE RATE MULTIPLIER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '167 contains a synchronous decade counter and four decoding gates that serve to gate the clock through to the output at a sub-multiple of the clock frequency. The output pulse rate, relative to the clock frequency, is determined by signals applied to the Select (S_0 — S_3) inputs. Both true and complement outputs are available, along with an enable input for each. A Count Enable input and a Terminal Count output are provided for cascading two or more packages. Asynchronous Master Reset and Master Set inputs prevent counting and clear the counter or set it to maximum, respectively.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

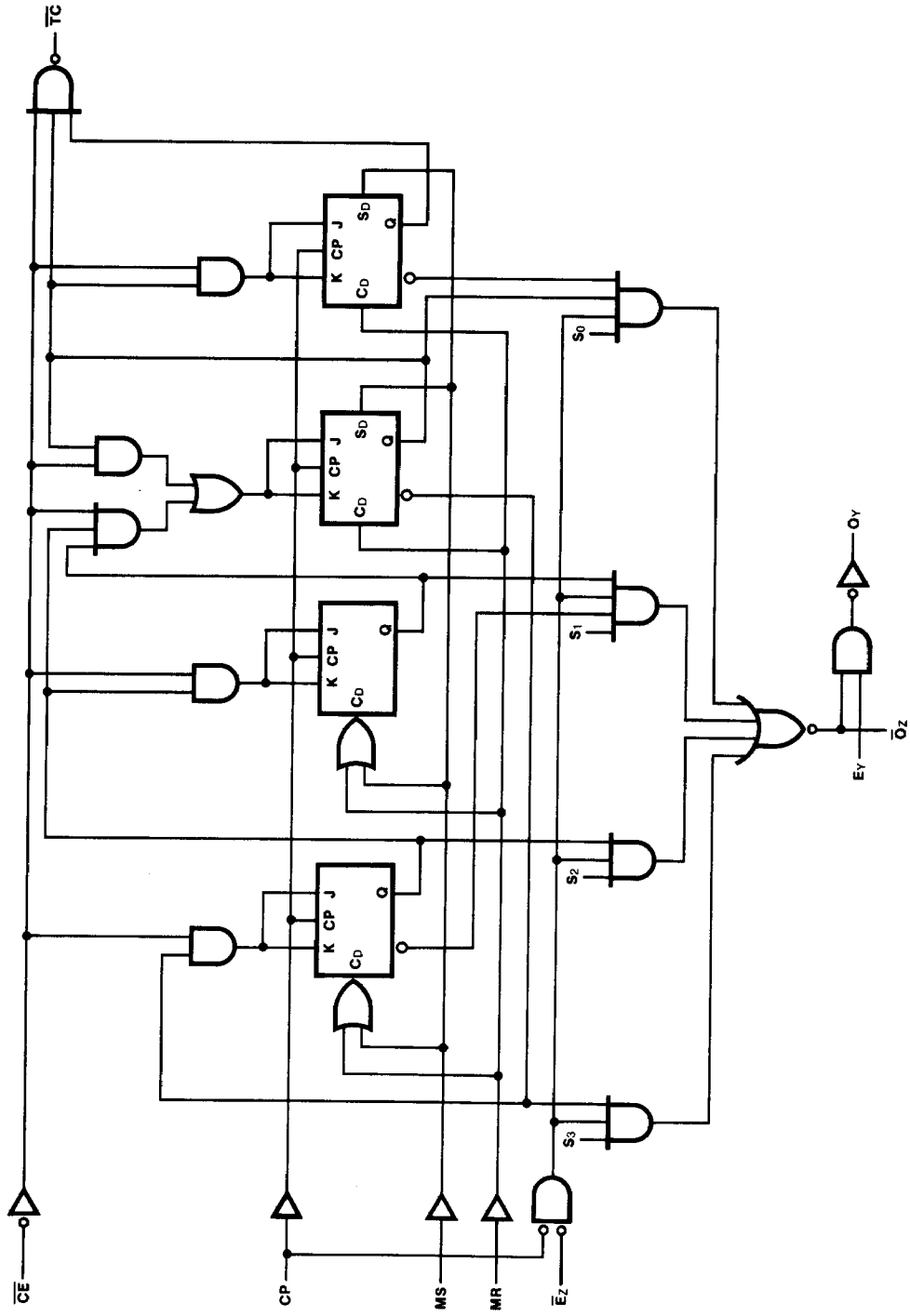
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74167PC		9B
Ceramic DIP (D)	A	74167DC	54167DM	7B
Flatpak (F)	A	74167FC	54167FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
S_0 — S_3	Rate Select Inputs	1.0/1.0
$\overline{E}_Z$	$\overline{O}_Z$ Enable Input (Active LOW)	1.0/1.0
E_Y	O_Y Enable Input	1.0/1.0
$\overline{CE}$	Count Enable Input (Active LOW)	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0
MS	Asynchronous Master Set Input (Active HIGH) (Set to 9)	1.0/1.0
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0
$\overline{O}_Z$	Gated Clock Output (Active LOW)	10/10
O_Y	Complement Output (Active HIGH)	10/10
$\overline{TC}$	Terminal Count Output (Active LOW)	10/10

LOGIC DIAGRAM



TRUTH TABLE

INPUTS									OUTPUTS			
MR	$\overline{CE}$	$\overline{E}_Z$	S_3	S_2	S_1	S_0	CLOCK PULSES	E_Y	O_Y	$\overline{O}_Z$	$\overline{TC}$	NOTES
H	X	H	X	X	X	X	X	H	L	H	H	1
L	L	L	L	L	L	L	10	H	L	H	1	2
L	L	L	L	L	L	H	10	H	1	1	1	2
L	L	L	L	L	H	L	10	H	2	2	1	2
L	L	L	L	L	H	H	10	H	3	3	1	2
L	L	L	L	H	L	L	10	H	4	4	1	2
L	L	L	L	H	L	H	10	H	5	5	1	2
L	L	L	L	H	H	L	10	H	6	6	1	2
L	L	L	L	H	H	H	10	H	7	7	1	2
L	L	L	H	L	L	L	10	H	8	8	1	2
L	L	L	H	L	L	H	10	H	9	9	1	2
L	L	L	H	L	H	L	10	H	8	8	1	2, 3
L	L	L	H	L	H	H	10	H	9	9	1	2, 3
L	L	L	H	H	L	L	10	H	8	8	1	2, 3
L	L	L	H	H	L	H	10	H	9	9	1	2, 3
L	L	L	H	H	H	L	10	H	8	8	1	2, 3
L	L	L	H	H	H	H	10	H	9	9	1	2, 3
L	L	L	H	L	L	H	10	L	H	9	1	4

1. This is a simplified illustration of the clear function. CP and $\overline{E}_Z$ also affect the logic level of O_Y and $\overline{O}_Z$. A LOW signal on E_Y will cause O_Y to remain HIGH.
2. Each rate illustrated assumes $S_0 - S_3$ are constant throughtout the cycle; however, these illustrations in no way prohibit variable-rate operation.
3. These input condtions exceed the range of the decade rate Select inputs.
4. E_Y can be used to inhibit output O_Y.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

PULSE PATTERN TABLE

S_3	S_2	S_1	S_0	m	$\overline{O}_Z$ PULSE PATTERN
L	L	L	H	1	1 1 1 1 0 1 1 1 1 1
L	L	H	L	2	1 1 0 1 1 1 1 0 1 1
L	L	H	H	3	1 1 0 1 0 1 1 0 1 1
L	H	L	L	4	1 0 1 0 1 1 0 1 0 1
L	H	L	H	5	1 0 1 0 0 1 0 1 0 1
L	H	H	L	6	1 0 0 0 1 1 0 0 0 1
L	H	H	H	7	1 0 0 0 0 1 0 0 0 1
H	L	L	L	8	0 0 0 0 1 0 0 0 0 1
H	L	L	H	9	0 0 0 0 0 0 0 0 0 1

H = HIGH Voltage Level
L = LOW Voltage Level

FUNCTIONAL DESCRIPTION — The '167 contains four JK flip-flops connected as a synchronous decade counter with a count sequence of 0-1-2-3-4-8-9-10-11-12. A LOW signal on the Count Enable ($\overline{CE}$) input permits counting, with all state changes initiated simultaneously by the rising edge of the clock. When the count reaches maximum (12) the Terminal Count ($\overline{TC}$) output goes LOW if $\overline{CE}$ is LOW. A HIGH signal on Master Reset (MR) clears the flip-flops and prevents counting, although output pulses can still occur if the clock is running, $\overline{E}_Z$ is LOW and S_3 is HIGH. A HIGH signal on Master Set (MS) prevents counting and sets the counter to 12, the only state in which no output pulses can occur.

The flip-flop outputs are decoded by a 4-wide AND-OR-INVERT gate. Each AND gate also contains the buffered and inverted CP and Z-enable ($\overline{E}_Z$) functions, as well as one of the Select (S_0 — S_3) inputs. The Z output $\overline{O}_Z$ is normally HIGH and goes LOW when CP and $\overline{E}_Z$ are LOW and any of the AND gates has its other inputs HIGH. The AND gates are enabled at different times and different rates relative to the clock. For example, the gate to which S_0 is connected is enabled only when the counter is in state five, assuming that S_0 is HIGH. Thus, during one complete cycle of the counter (10 clocks) the S_0 gate can contribute only pulse to the output rate. The S_1 gate is enabled twice per cycle, the S_2 gate four times per cycle (etc.). The output pulse rate thus depends on the clock rate and which of the S_0 — S_3 inputs are HIGH, as expressed in the following formula.

$$f_{out} = \frac{m}{10} \bullet f_{in}$$

$$\text{where } m = S_3 \bullet 2^3 + S_2 \bullet 2^2 + S_1 \bullet 2^1 + S_0 \bullet 2^0$$

Thus by appropriate choice of signals applied to the S_0 — S_3 inputs, the output pulse rate can range from 1/10 to 9/10 of the clock rate. The select codes, m values and $\overline{O}_Z$ pulse pattern are shown in the Pulse Pattern Table. In the $\overline{O}_Z$ pattern, each column represents a clock period, with the state-12 column on the right. A one indicates that the $\overline{O}_Z$ output will be HIGH during that entire clock period, while a zero indicates that $\overline{O}_Z$ will be LOW when the clock is LOW during that period. Note that the output pulses are evenly spaced only when m is one or two, assuming that the clock frequency is constant, and that no output pulses can occur in state 12 of the counter.

The Y output O_Y is the complement of $\overline{O}_Z$ and is thus normally LOW. A LOW signal on the Y-enable input E_Y disables O_Y. To expand the multiplier to 2-digit rate select, two packages can be cascaded as shown in *Figure a*. Both circuits operate from the basic clock, with the $\overline{TC}$ output of the first acting to enable both counting and the output pulses of the second package. Thus the second counter advances at only 1/10 the rate of the first and a full cycle of the two counters combined requires 100 clocks. Output pulses contributed by the second counter occur only when the first counter is in state 12. All output pulses are opposite in phase to the clock.

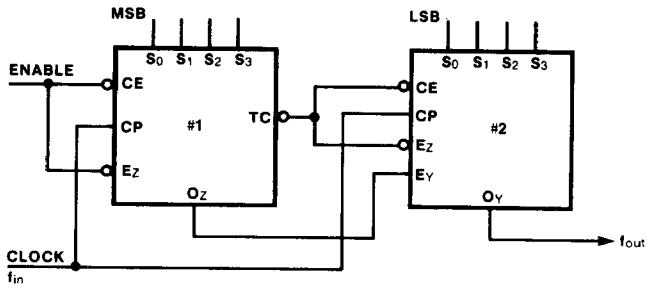


Fig. a Cascading for 2-Digit Rate Select

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	-18	-55	mA	V_{CC} = Max
I_{CC}	Power Supply Current		99	mA	V_{CC} = Max; MS = Gnd Other Inputs = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		30 33	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to O_Y		30 33	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay E_Y to O_Y		14 10	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{O}_Z$		14 10	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to O_Y		39 30	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_Z$ to $\overline{O}_Z$		18 23	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay S_n to O_Y		23 23	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_Z$		18 26	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{TC}$		20 21	ns	
t_{PHL}	Propagation Delay MS to $\overline{TC}$		27	ns	Figs. 3-1, 3-16
t_{PLH}	Propagation Delay MR to O_Y		36	ns	
t_{PHL}	Propagation Delay MR TO $\overline{O}_Z$		23	ns	

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AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = 25° C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t_s (L)	Setup Time LOW $\overline{CE}$ to CP Rising	25		ns	Fig. b
t_h (H)	Hold Time HIGH $\overline{CE}$ to CP Rising	0	t_w CP-10	ns	
t_s (L)	Setup Time LOW $\overline{CE}$ to CP Falling	0	t_w CP-10	ns	Fig. c
t_h (L)	Hold Time LOW $\overline{CE}$ to CP Falling	20	T-10	ns	
t_{inh} (H)	Inhibit Time HIGH $\overline{CE}$ to CP Falling	10		ns	Fig. b
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8
t_w (H)	MR Pulse Width HIGH	15		ns	Fig. 3-16
t_w (H)	MS Pulse Width HIGH	15		ns	

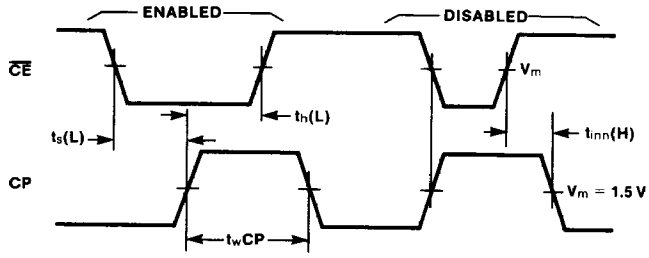

Fig. b

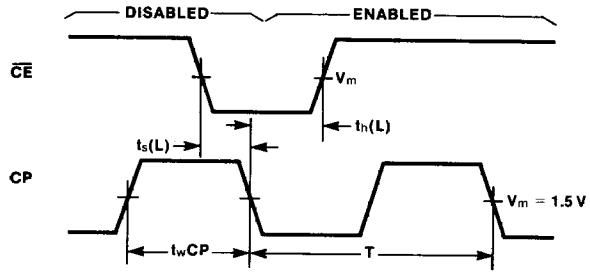

Fig. c