FAIRCHILD SEMICONDUCTOR®

January 2008

74ABT126
Quad Buffer with 3-STATE Outputs

Features

- Non-inverting buffers
- Output sink capability of 64mA, source capability of 32mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

General Description

The ABT126 contains four independent non-inverting buffers with 3-STATE outputs.

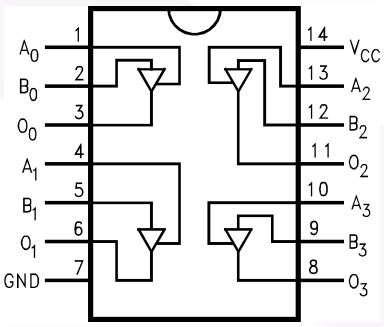
Ordering Information

Order Number	Package Number	Package Description
74ABT126CSC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ABT126CSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT126CMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Function Table

Inputs		Output
A_n	B_n	O_n
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

Z = HIGH Impedance

X = Immaterial

Pin Description

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	–65°C to +150°C
T_A	Ambient Temperature Under Bias	–55°C to +125°C
T_J	Junction Temperature Under Bias	–55°C to +150°C
V_{CC}	V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
V_{IN}	Input Voltage(1)	–0.5V to +7.0V
I_{IN}	Input Current(1)	–30mA to +5.0mA
V_O	Voltage Applied to Any Output	
	Disabled or Power-Off State	–0.5V to 5.5V
	HIGH State	–0.5V to V_{CC}
	Current Applied to Output in LOW State (Max.)	twice the rated I_{OL} (mA)
	DC Latchup Source Current (Across Comm Operating Range)	–300mA
	Over Voltage Latchup (I/O)	10V

Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	–40°C to +85°C
V_{CC}	Supply Voltage	+4.5V to +5.5V
$\Delta V / \Delta t$	Minimum Input Edge Rate	
	Data Input	50mV/ns
	Enable Input	100mV/ns

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage			Recognized HIGH Signal	2.0			V
V_{IL}	Input LOW Voltage			Recognized LOW Signal			0.8	V
V_{CD}	Input Clamp Diode Voltage		Min.	I_{IN} = –18mA			–1.2	V
V_{OH}	Output HIGH Voltage		Min.	I_{OH} = –3mA	2.5			V
				I_{OH} = –32mA	2.0			
V_{OL}	Output LOW Voltage		Min.	I_{OL} = 64mA			0.55	V
I_{IH}	Input HIGH Current		Max.	V_{IN} = 2.7V[2]			1	µA
				V_{IN} = V_{CC}			1	
I_{BVI}	Input HIGH Current Breakdown Test		Max.	V_{IN} = 7.0V			7	µA
I_{IL}	Input LOW Current		Max.	V_{IN} = 0.5V[2]			–1	µA
				V_{IN} = 0.0V			–1	
V_{ID}	Input Leakage Test		0.0	I_{ID} = 1.9µA, All Other Pins Grounded	4.75			V
I_{OZH}	Output Leakage Current		0–5.5V	V_{OUT} = 2.7V, $\overline{OE}_n$ = 2.0V			10	µA
I_{OZL}	Output Leakage Current		0–5.5V	V_{OUT} = 0.5V, $\overline{OE}_n$ = 2.0V			–10	µA
I_{OS}	Output Short-Circuit Current		Max.	V_{OUT} = 0.0V	–100		–275	mA
I_{CEX}	Output HIGH Leakage Current		Max.	V_{OUT} = V_{CC}			50	µA
I_{ZZ}	Bus Drainage Test		0.0	V_{OUT} = 5.5V, All Others GND			100	µA
I_{CCH}	Power Supply Current		Max.	All Outputs HIGH			50	µA
I_{CCL}	Power Supply Current		Max.	All Outputs LOW			15	mA
I_{CCZ}	Power Supply Current		Max.	$\overline{OE}_n$ = V_{CC}, All Others at V_{CC} or Ground			50	µA
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled	Max.	V_I = V_{CC} – 2.1V			1.5	mA
		Outputs 3-STATE		Enable Input V_I = V_{CC} – 2.1V			1.5	mA
		Outputs 3-STATE		Data Input V_I = V_{CC} – 2.1V, All Others at V_{CC} or Ground			50	µA
I_{CCD}	Dynamic I_{CC} No Load[2]		Max.	Outputs OPEN, $\overline{OE}_n$ = GND[3], One-Bit Toggling, 50% Duty Cycle			0.1	mA/ MHz

Notes:

2. Guaranteed, but not tested.

3. For 8-bit toggling, I_{CCD} < 0.8mA/MHz.

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50pF$			$T_A = –40°C$ to $+85°C$ $V_{CC} = 4.5V–5.5V$ $C_L = 50pF$		Units
		Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, Data to Outputs	1.0		4.4	1.0	4.4	ns
t_{PHL}		1.0		4.6	1.0	4.6	
t_{PZH}	Output Enable Time	1.0		6.5	1.0	6.5	ns
t_{PZL}		1.0		6.5	1.0	6.5	
t_{PHZ}	Output Disable Time	1.0		5.8	1.0	5.8	ns
t_{PLZ}		1.0		5.5	1.0	5.5	

Capacitance

Symbol	Parameter	Conditions $T_A = 25°C$	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$	5.0	pF
C_{OUT}(4)	Output Capacitance	$V_{CC} = 5.0V$	9.0	pF

Note:

4. C_{OUT} is measured at frequency f = 1MHz, per MIL-STD-883, Method 3012.

Physical Dimensions

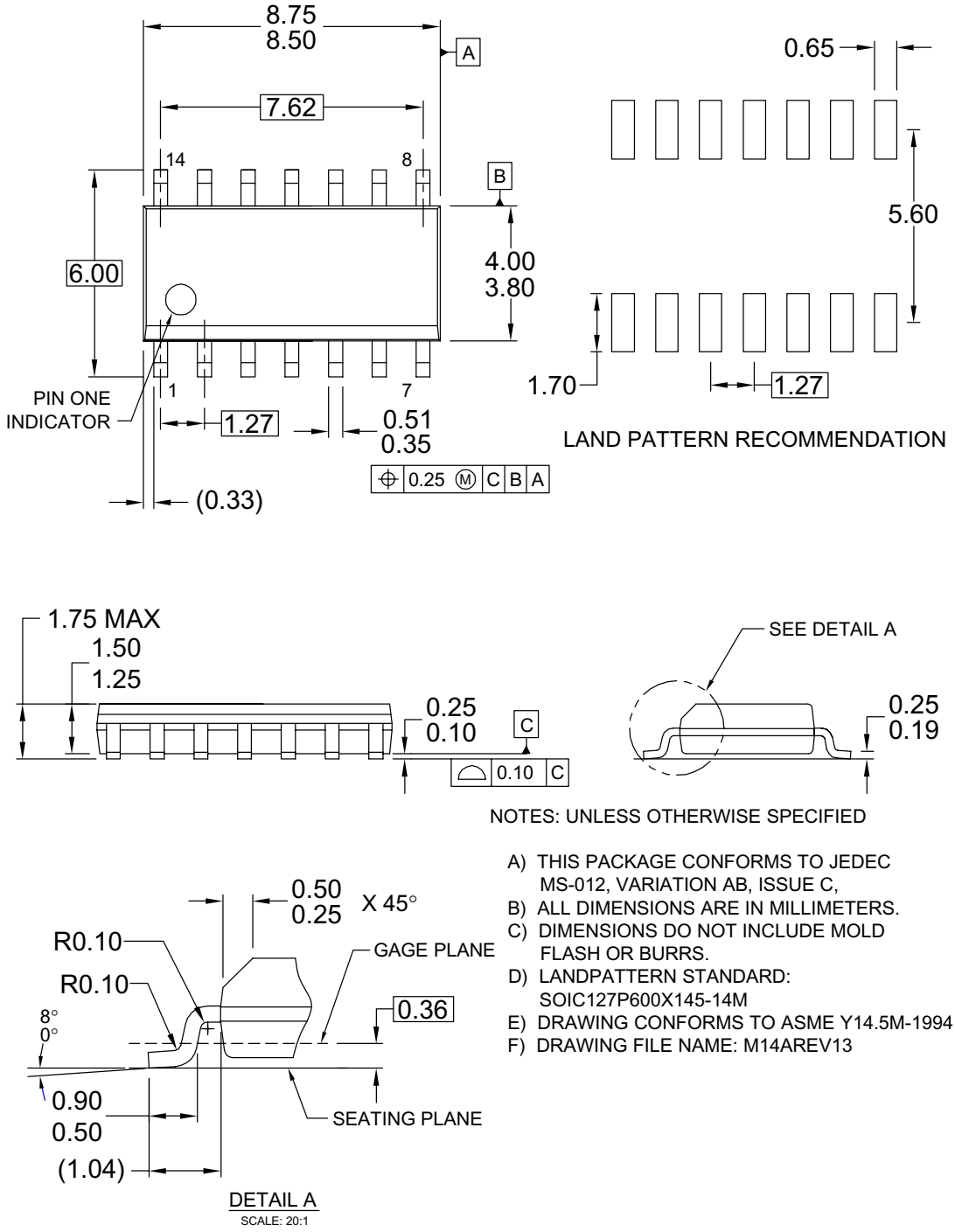


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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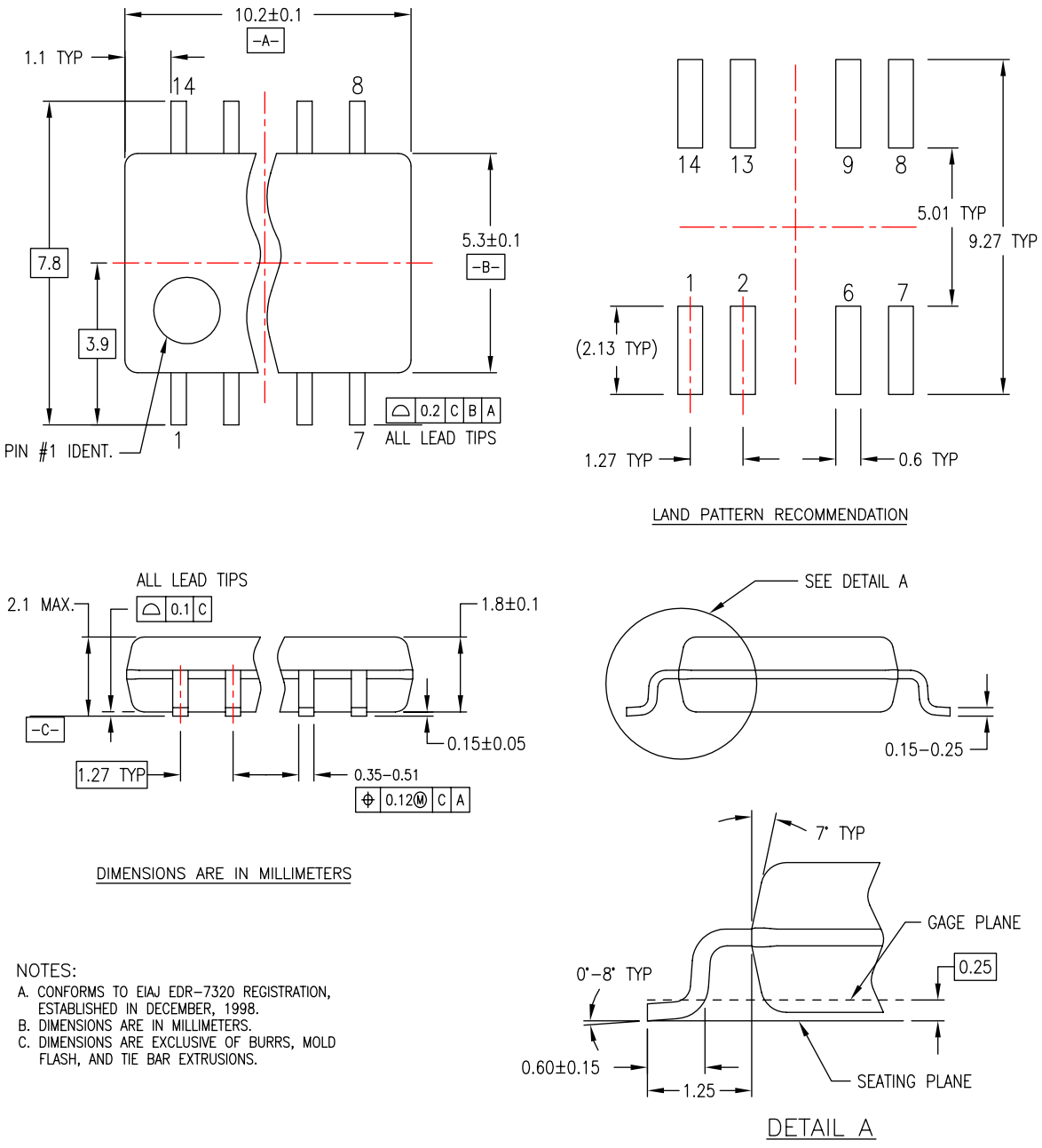
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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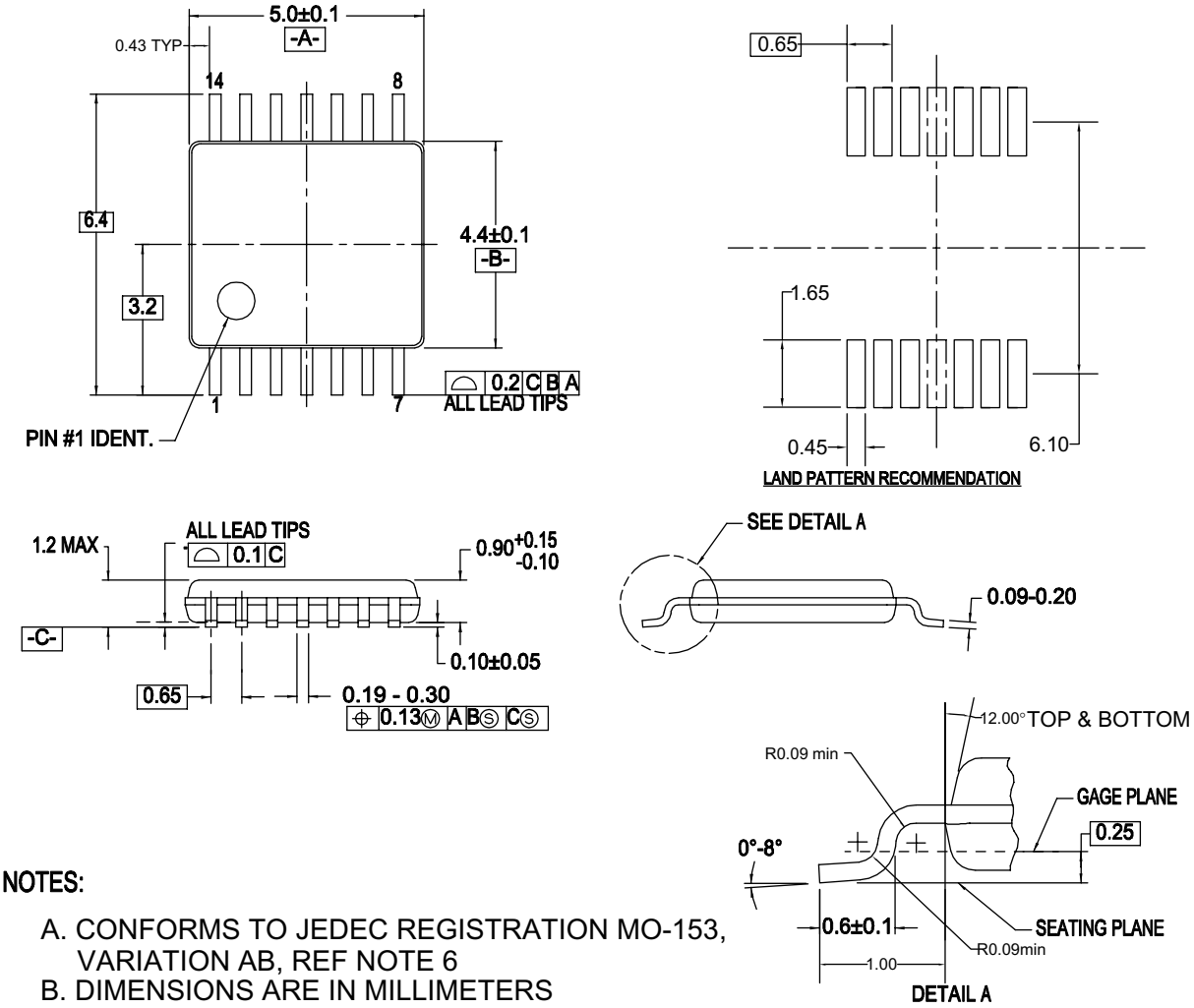
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

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D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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