FAIRCHILD SEMICONDUCTOR™

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DM9328
Dual 8-Bit Shift Register

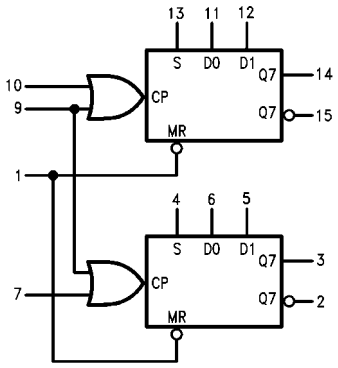
General Description

The DM9328 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers. The multifunctional capability of this device is provided by several features: 1) additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources; 2) the clock of each register may be provided separately or together; 3) both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

Ordering Code:

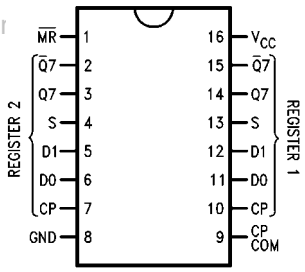
Order Number	Package Number	Package Description
DM9328N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram



Pin Descriptions

Pin Names	Description
S	Data Select Input
D0, D1	Data Inputs
CP	Clock Pulse Input (Active HIGH)
	Common (Pin 9)
	Separate (Pins 7 and 10)
$\overline{MR}$	Master Reset Input (Active LOW)
Q7	Last Stage Output
$\overline{Q}7$	Complementary Output

Functional Description

The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW-to-HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH-to-LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a 2-input multiplexer in front of the serial data input. The two data inputs D0 and D1 are controlled by the data select input (S) following the Boolean expression:

Serial data in: $S_D = SD0 + SD1$

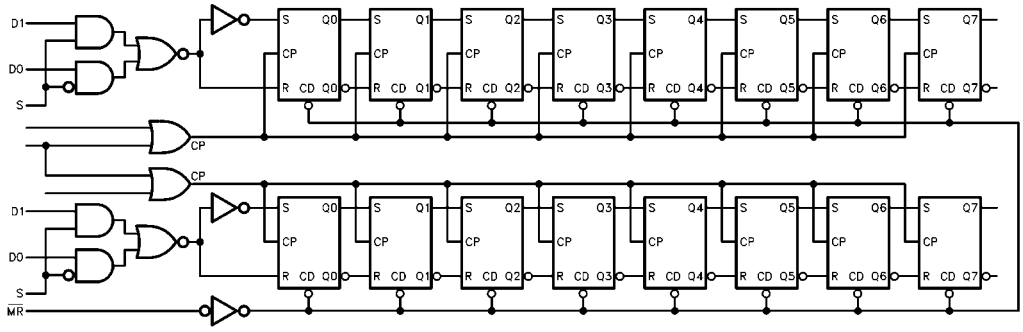
An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all 16 stages independently of any other input signal.

Shift Select Table

INPUTS			OUTPUT
S	**D0**	**D1**	**Q7 (t_{n+8})**
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
n + 8 = indicates state after eight clock pulse

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	0 0			ns
t_w (H) t_w (L)	Clock Pulse Width HIGH or LOW	25 25			ns
t_w (L)	$\overline{MR}$ Pulse Width with CP HIGH	30			ns
t_w (L)	$\overline{MR}$ Pulse Width with CP LOW	40			ns
t_{REC}	Recovery Time $\overline{MR}$ to CP	33			ns

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V $\overline{MR}$, D_n Inputs			40	µA
		CP Inputs			60	
		S Inputs			80	
		CP (COM) Inputs			120	
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V $\overline{MR}$, D_n Inputs			−1.6	mA
		CP Inputs			−2.4	
		S Inputs			−3.2	
		CP (COM) Input			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max			77	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

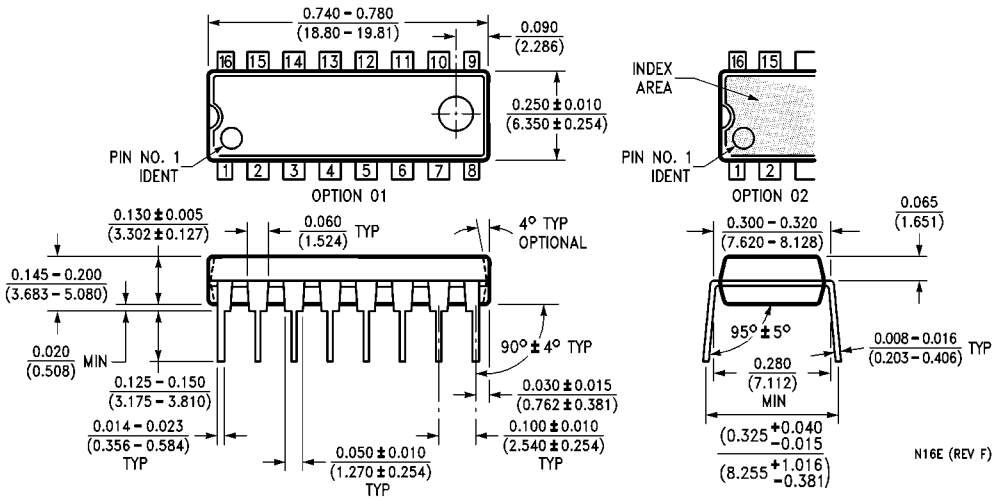
Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	C_L = 15 pF, R_L = 400Ω		Units
		Min	Max	
f_{MAX}	Maximum Shift Right Frequency	20		MHz
t_{PLH}	Propagation Delay		20	ns
t_{PHL}	CP to Q7 or $\overline{Q}$7		35	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q7		50	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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