

FT6116

2K X 8 CMOS SRAM

FORCE

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Features

- ♦ High-speed access and chip select times
 - Military: 120/150ns (max.)
- ♦ Low-power consumption
- ♦ Battery backup operation
 - 2V data retention voltage (Low power version only)
- ♦ Produced with advanced CMOS high-performance technology
- ♦ CMOS process virtually eliminates alpha particle soft-error rates
- ♦ Input and output directly TTL-compatible
- ♦ Static operation: no clocks or refresh required
- ♦ Available in ceramic and plastic 24-pin DIP, 24-pin Thin Dip,

Description

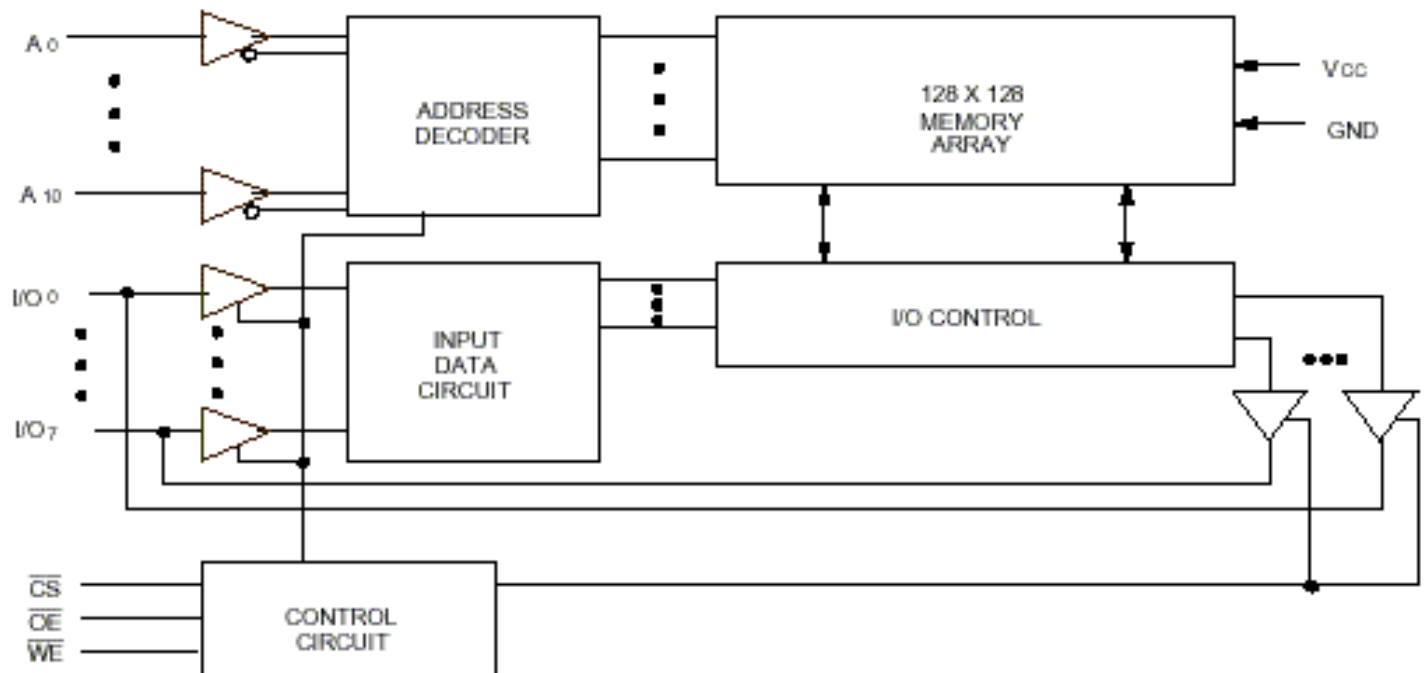
The FT6116 is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using FT's high-performance, high-reliability CMOS technology.

Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When \overline{CS} goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as \overline{CS} remains HIGH. This capability provides significant system level power and cooling savings. The low-power version also offers a battery backup data retention capability where the circuit typically consumes only 1 μ W to 4 μ W operating off a 2V battery.

All inputs and outputs of the FT6116 are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The FT6116 is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP

Functional Block Diagram

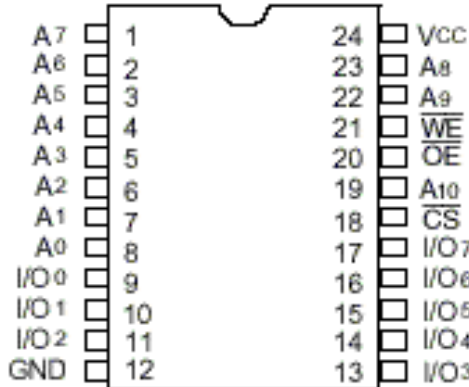


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Pin Configurations



**DIP
Top View**

Pin Description

Name	Description
A ₀ - A ₁₀	Address Inputs
I/O ₀ - I/O ₇	Data Input/Output
CS	Chip Select
WE	Write Enable
OE	Output Enable
VCC	Power
GND	Ground

Capacitance (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{IO}	I/O Capacitance	V _{OUT} = 0V	8	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
V _{TERW} ⁽¹⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V_{RES} must not exceed V_{CC} +0.5V.

Truth Table⁽¹⁾

Mode	CS	OE	WE	I/O
Standby	H	X	X	High-Z
Read	L	L	H	DATA _{OUT}
Read	L	H	H	High-Z
Write	L	X	L	DATA _{IN}

NOTE: www.DataSheet4U.com

1. H = V_{IN}, L = 0V, X = Don't Care.

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Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-45°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5 ¹⁾	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	3.5	Vcc +0.5	V
V _{IL}	Input Low Voltage	-0.5 ²⁾	—	0.8	V

NOTES:

- V_I (min.) = -3.0V for pulse width less than 20ns, once per cycle.
- V_I must not exceed Vcc +0.5V.

DC Electrical Characteristics (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	FT6116		Unit
			Min.	Max.	
I _I	Input Leakage Current	Vcc = Max., V _{IH} = GND to Vcc MIL. COMPL.	—	5 2	μA
I _O	Output Leakage Current	Vcc = Max., CS = V _{IH} , V _{OUT} = GND to Vcc MIL. COMPL.	—	5 2	μA
V _{OL}	Output Low Voltage	I _{OL} = 8mA, Vcc = Min.	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA, Vcc = Min.	4	—	V

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DC Electrical Characteristics⁽¹⁾ (continued)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power					FT6116 120	FT6116 150	Unit
							MI Only	MI Only	
I _{CC1}	Operating Power Supply Current, $\overline{CS} \leq V_{IL}$, Outputs Open V _{CC} = Max., f = 0						90	90	mA
I _{CC2}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open V _{CC} = Max., f = f _{max} ⁽²⁾						100	90	mA
I _{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open V _{CC} = Max., f = f _{max} ⁽²⁾						25	25	mA
I _{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, V _{CC} = Max., V _{IN} < V _{LC} or V _{IN} > V _{HC} , f = 0						10	10	mA

NOTES:

- All values are maximum guaranteed values.
- f_{max} = 1/f_{tc}, only address inputs are toggling at f_{max}, f = 0 means address inputs are not changing.

Data Retention Characteristics Over All Temperature Ranges

(LA Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition	Min.	Typ. ⁽³⁾ V _{CC} @		Max. V _{CC} @		Unit
				2.0V	3.0V	2.0V	3.0V	
V _{DR}	V _{CC} for Data Retention	—	2.0	—	—	—	—	V
I _{CCDR}	Data Retention Current							μA
		MIL	—	0.5	1.5	200	300	
		COMPL.	—	0.5	1.5	20	30	
t _{CDR} ⁽¹⁾	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ V _{IN} > V _{HC} or < V _{LC}	—	0	—	—	—	ns
t _R ⁽²⁾	Operation Recovery Time		t _{tc} ⁽¹⁾	—	—	—	—	ns
I _{I1}	Input Leakage Current		—	—	—	2	2	μA

NOTES:

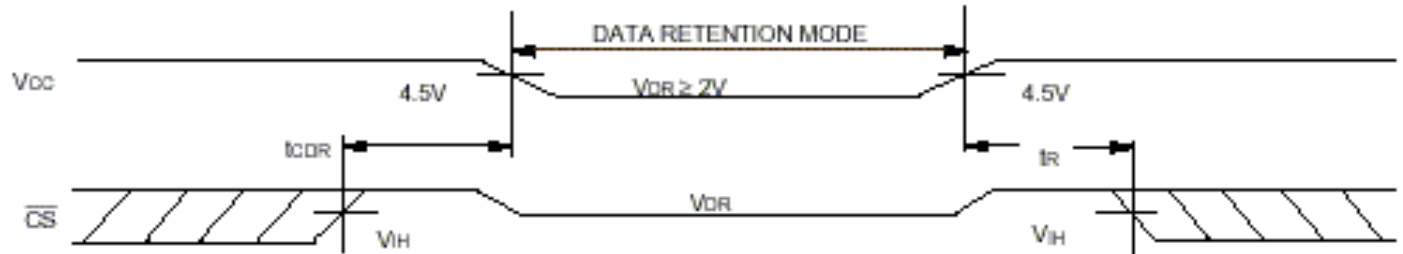
- T_A = +25°C
- t_{tc} = Read Cycle Time.
- This parameter is guaranteed by device characterization, but is not production tested.

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Low Vcc Data Retention Waveform



AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

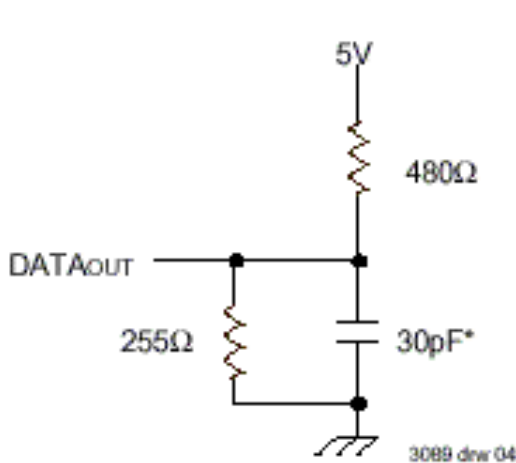


Figure 1. AC Test Load

3089 dwr 04

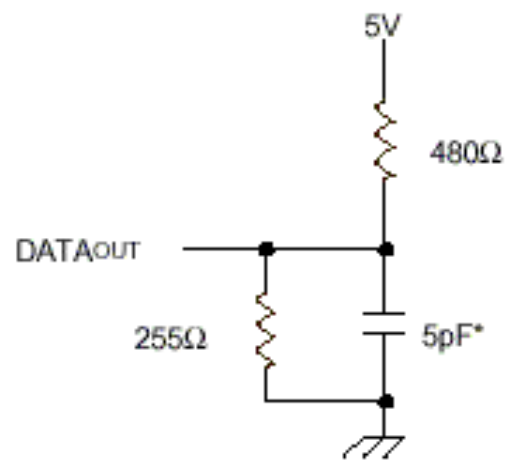


Figure 2. AC Test Load
(for t_{OL2} , t_{CL2} , t_{OH} , t_{BH} , t_{OZ} & t_{W})

*Including scope and jig.

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AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges) (continued)

Symbol	Parameter							FT6116 120 ⁽²⁾		FT6116 150 ⁽²⁾		Unit
								Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time							120	—	150	—	ns
t _{AA}	Address Access Time							—	120	—	150	ns
t _{CS}	Chip Select Access Time							—	120	—	150	ns
t _{OLZ⁽¹⁾}	Chip Select to Output in Low-Z							5	—	5	—	ns
t _{OE}	Output Enable to Output Valid							—	80	—	100	ns
t _{OLZ⁽¹⁾}	Output Enable to Output in Low-Z							5	—	5	—	ns
t _{OD⁽¹⁾}	Chip Deselect to Output in High-Z							—	40	—	40	ns
t _{OD⁽¹⁾}	Output Disable to Output in High-Z							—	40	—	40	ns
t _{OH}	Output Hold from Address Change							5	—	5	—	ns

NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

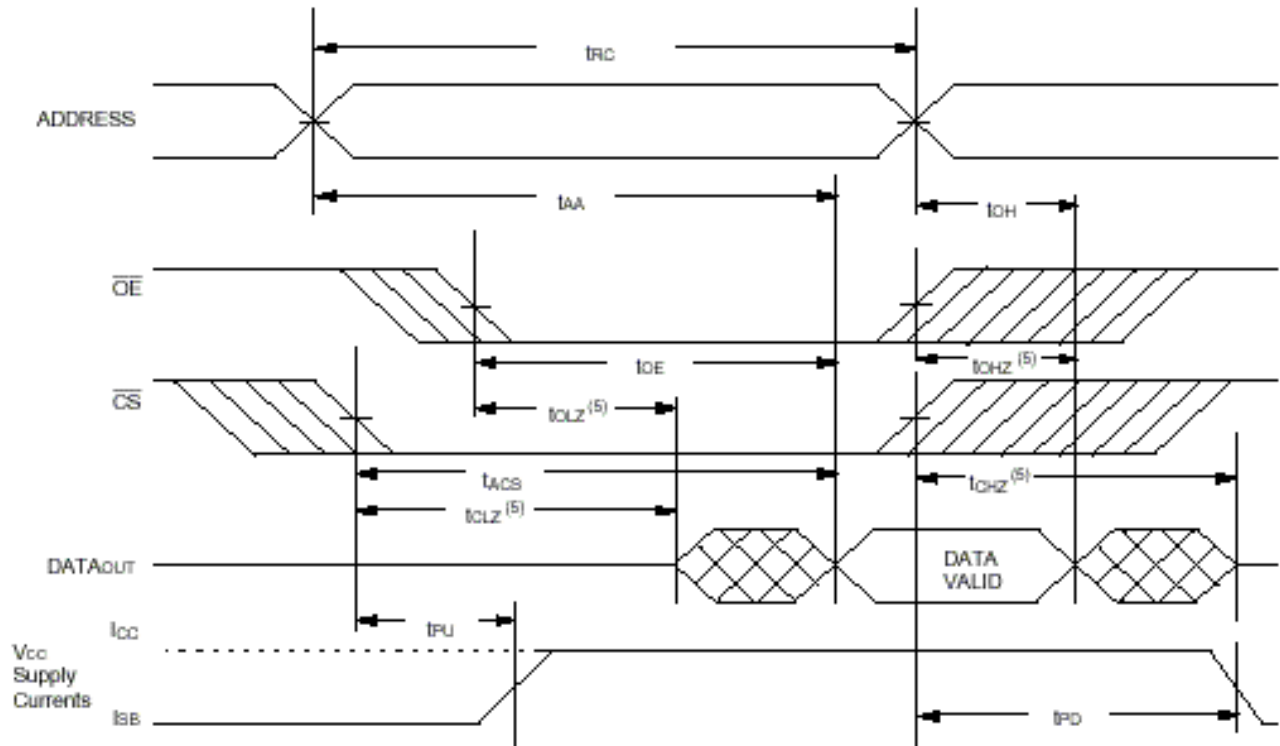
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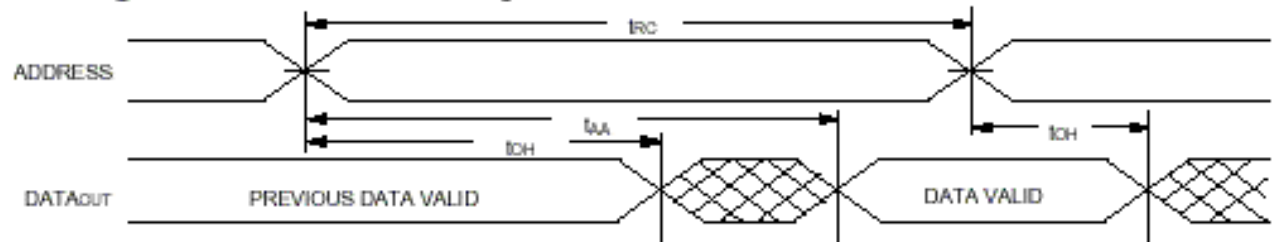
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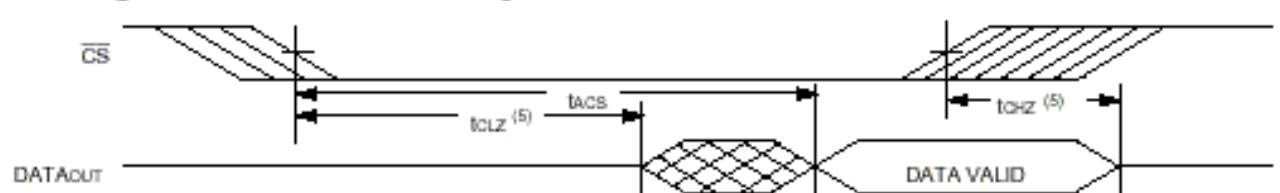
Timing Waveform of Read Cycle No. 1^(1,3)



Timing Waveform of Read Cycle No. 2^(1,2,4)



Timing Waveform of Read Cycle No. 3^(1,3,4)



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NOTES:

1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW.
4. OE is LOW.
5. Transition is measured $\pm 500mV$ from steady state.

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AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	FT6116 120 ⁽²⁾		FT6116̄ 150 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	
Write Cycle						
t _{WC}	Write Cycle Time	120	—	150	—	ns
t _{CS}	Chip Select to End-of-Write	70	—	90	—	ns
t _{AV}	Address Valid to End-of-Write	105	—	120	—	ns
t _{AS}	Address Setup Time	20	—	20	—	ns
t _{WP}	Write Pulse Width	70	—	90	—	ns
t _{WR}	Write Recovery Time	5	—	10	—	ns
t _{WU} ⁽¹⁾	Write to Output in High-Z	—	40	—	40	ns
t _{OW}	Data to Write Time Overlap	35	—	40	—	ns
t _{OH} ⁽¹⁾	Data Hold from Write Time	5	—	10	—	ns
t _{OW} ^(1,2)	Output Active from End-of-Write	0	—	0	—	ns

NOTES:

- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
- The specification for t_{OW} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{OH} and t_{OW} values will vary over voltage and temperature, the actual t_{OH} will always be smaller than the actual t_{OW}.

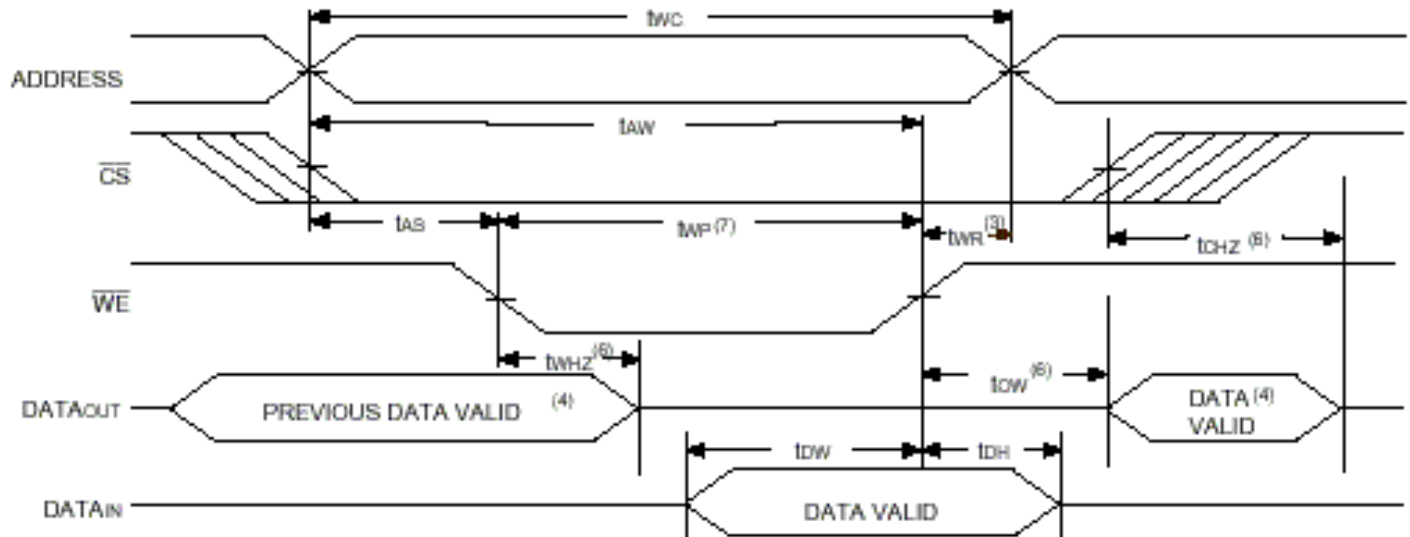
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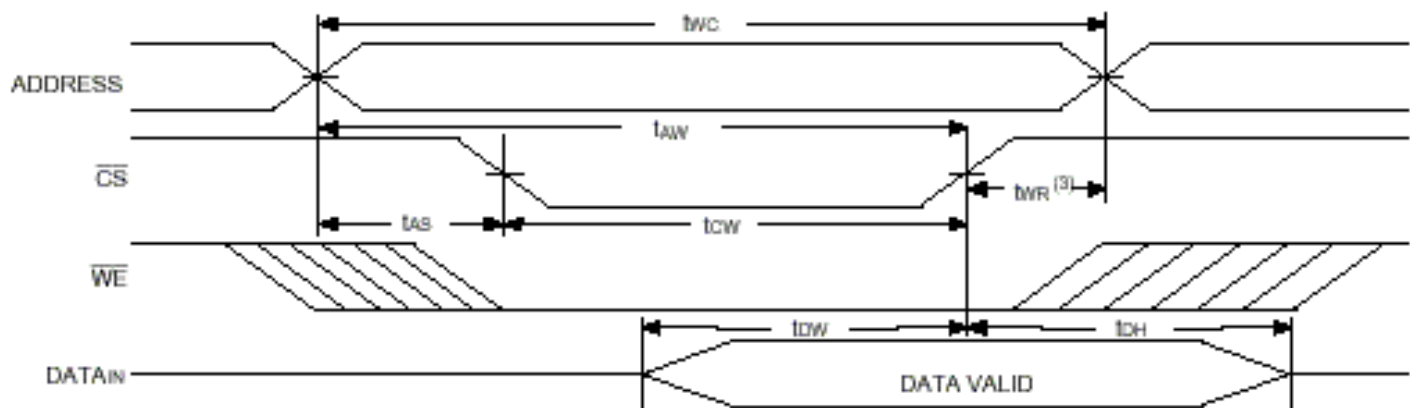
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Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled Timing)^(1,2,5,7)



Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled Timing)^(1,2,3,5,7)



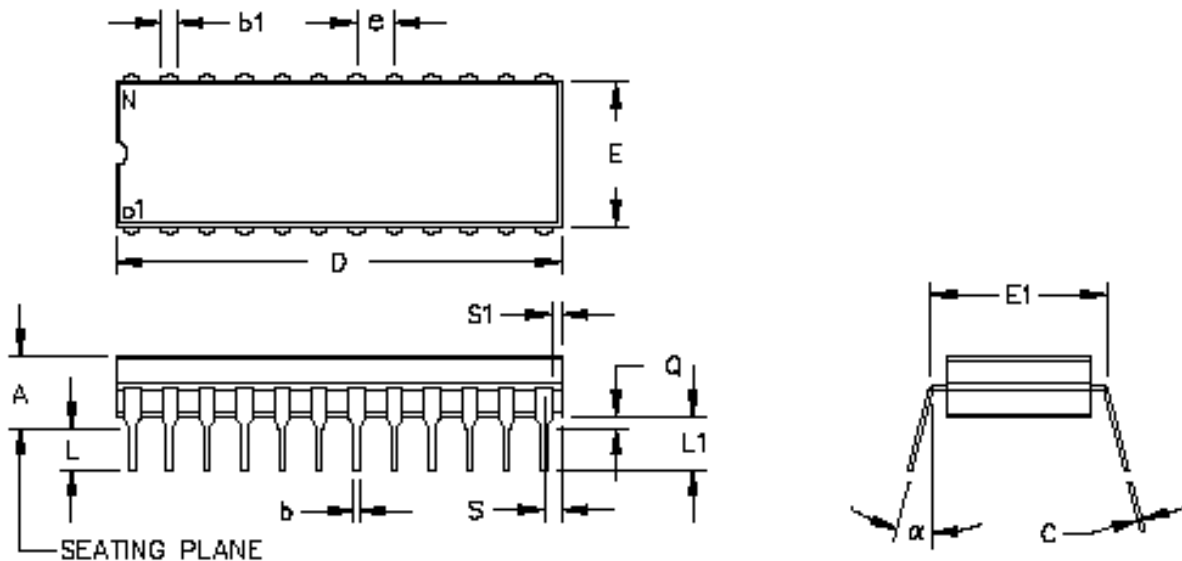
NOTES:

1. \overline{WE} or \overline{CS} must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW \overline{CS} and a LOW \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the \overline{CS} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state.
7. \overline{OE} is continuously HIGH. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{OW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP} . For a \overline{CS} controlled write cycle, \overline{OE} may be LOW with no degradation to t_{AS} .

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REV	DCN	DESCRIPTION	DATE	APPROVED
06	17517	UPDATED TO STANDARDIZE DWG		



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
 2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
 3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D24-1	
SYMBOL	MIN	MAX
A	.140	.200
b	.015	.021
b1	.045	.085
C	.009	.014
D	1.240	1.280
E	.285	.310
E1	.300	.320
e	.100 BSC	
L	.125	.175
L1	.150	-
Q	.015	.080
S	.030	.080
S1	.005	-
α	0°	15°
N	24	

MIL-M-38510		CONFIGURATION	EXCEPTIONS
JEDEC		D-9	NONE
TOLERANCES UNLESS OTHERWISE SPECIFIED FRAC DEC ANGLES ± - ± - ± -		MO-058-AA	NONE
APPROVALS	DATE	24 LD CERDIP MKT DWG (300 MIL)	
DRAWN			
CHECKED			
SCALE	SIZE	DRAWING NO.	REV
N/A	A		06
DO NOT SCALE DRAWING			SHEET 2 OF 2

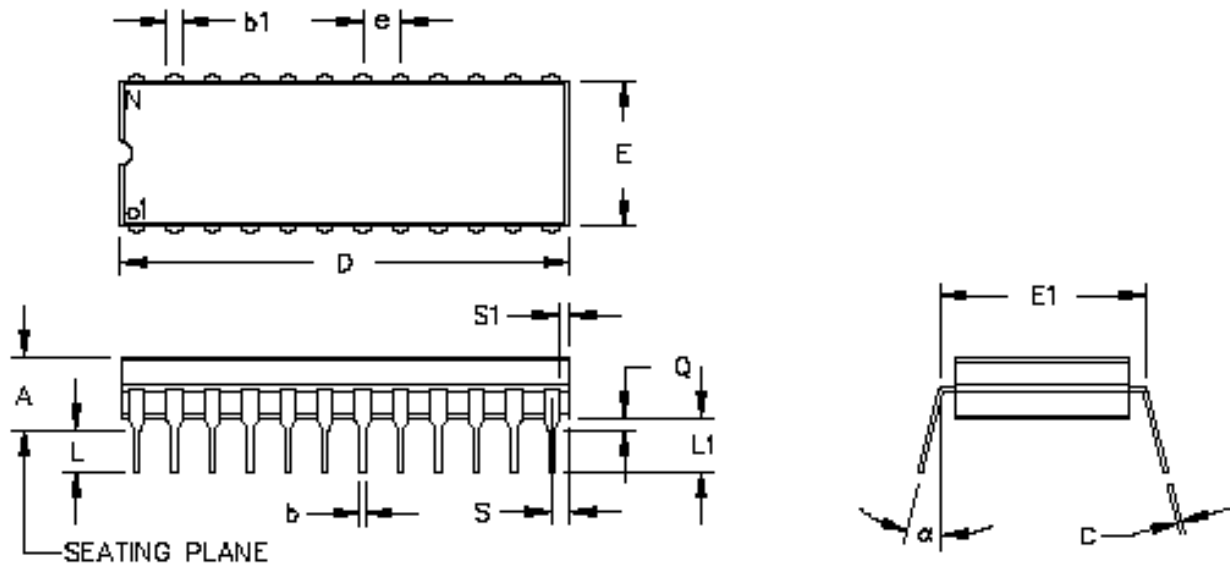
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REV	DCN	DESCRIPTION	DATE	APPROVED
06	17514	UPDATED TO STANDARDIZE DWG		
07	22234	CHANGED b1 MIN DIM		



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
 2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
 3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D24-2				CONFIGURATION	EXCEPTIONS		
SYMBOL	MIN	MAX			D-3	NONE		
A	.090	.190	MIL-M-38510		NOT REGISTERED			
b	.014	.023	JEDEC					
b1	.045	.060	TOLERANCES UNLESS OTHERWISE SPECIFIED FRAC DEC ANGLES ± - ± - ± -					
C	.008	.012	APPROVALS	DATE				
D	1.230	1.290	DRAWN		24 LD CERDIP MKT DWG (600 MIL)			
E	.500	.610	CHECKED					
E1	.590	.620			SCALE	SIZE	DRAWING NO.	REV
e	.100 BSC				N/A	A		07
L	.125	.200			DO NOT SCALE DRAWING		SHEET 2 OF 2	
L1	.150	-						
Q	.015	.060						
S	.030	.080						
S1	.005	-						
alpha	0°	15°						
N	24							