GS8000
DVI / HDMI Extender

GS8000 Data Sheet

Key Features

- extends cable length of the TMDS and DDC channels of a DVI or HDMI link
- DVI 1.0-compliant and HDMI 1.1-compliant input and output signalling
- one device supports a complete single link DVI 1.0 or HDMI interface (two devices for a dual link DVI interface)
- operational at TMDS rates from 252Mb/s to 1.65Gb/s
- supports display resolutions up to UXGA at 60Hz in 24-bit true colour pixel format
- integrated user-tunable input termination resistors
- automatic identification of link inactivity with carrier detect output
- output signal swing adjustable from 200mV to 2000mV differential into 100Ω load
- output enable function
- superior noise immunity
- small footprint (44-pin QFN)

Applications

A DVI or HDMI input that will only be connected to a DVI output with launch amplitude between 800mV and 1200mV differential. Since many DVI graphics cards transmit at amplitudes outside this range, the GS8000 is not recommended for a generic DVI input.

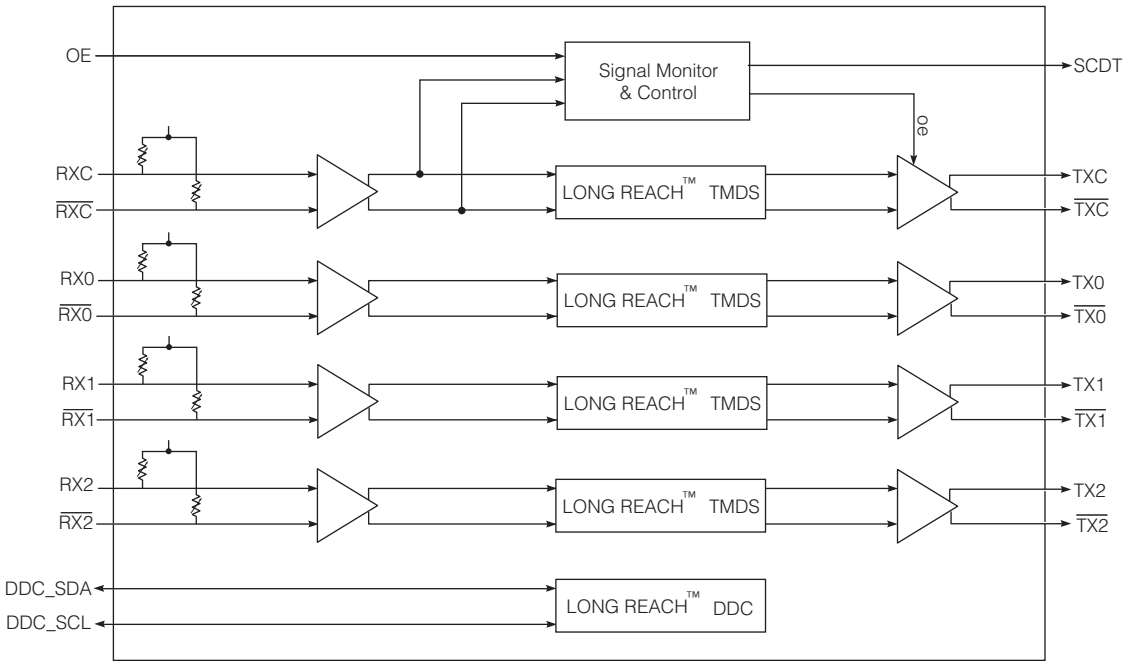
Description

The GS8000 is Gennum's DVI 1.0-compliant and HDMI 1.1-compliant automatic cable extender. When used in front of a DVI/HDMI receiver, it produces a receive solution with longer cable length. A DVI link of 20 to 30 metres at UXGA 60Hz (162Mb/s) can be realized with the GS8000 provided the DVI transmitter is within the DVI specification for jitter and voltage swing and that high quality DVI cable is used.

The GS8000 contains an Output Enable input and Carrier Detect output to allow for auto muting of the clock and data outputs upon link inactivity.

Excellent power supply and common mode noise rejection is employed to ensure robust operation in noisy environments. The differential outputs are adjustable and compatible with the DVI 1.0 and HDMI 1.1 receiver specifications for input common mode voltage and swing.

The GS8000 is designed in a CMOS process requiring a 3.3V power supply. The analog I/O and digital core power supply voltages may be individually provided.

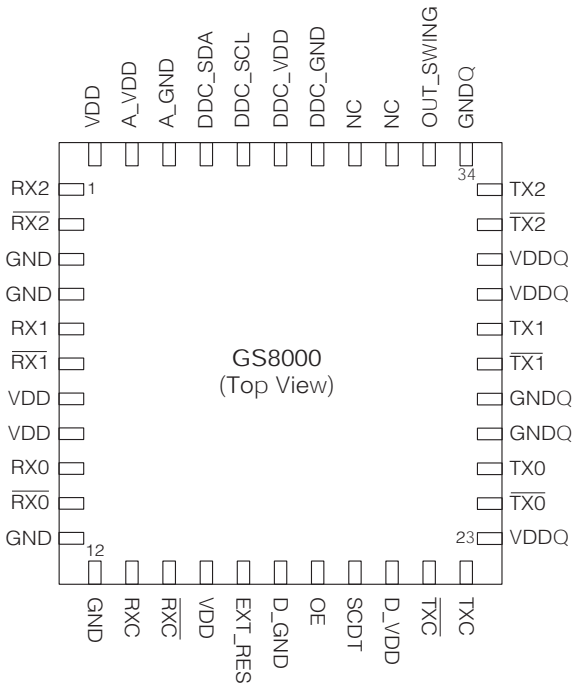


GS8000 Functional Block Diagram

Contents

1. Pin Out

1.1 Pin Assignment



1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1, 2	RX2, $\overline{RX2}$	Analog	Input	Transition minimized differential signal (TMDS) data input 2.
3, 4, 11, 12	GND	Analog	Power	Differential input buffer ground connection.
7, 8, 15, 44	VDD	Analog	Power	Power supply for the differential input buffers. Connect to +3.3V DC.
5, 6	RX1, $\overline{RX1}$	Analog	Input	Transition minimized differential signal (TMDS) data input 1.
9, 10	RX0, $\overline{RX0}$	Analog	Input	Transition minimized differential signal (TMDS) data input 0.
13, 14	RXC, $\overline{RXC}$	Analog	Input	Transition minimized differential signal (TMDS) input clock.
16	EXT_RES	Non Synchronous	Input	Termination for differential inputs. An external resistor connected from this input to D_GND is used to set the input termination. Use 500Ω to set the input termination to 50Ω.
17	D_GND	Non Synchronous	Power	Digital core ground connection.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
18	OE	Non Synchronous	Input	CONTROL SIGNAL INPUT Output enable (active HIGH). When set HIGH, the differential signal outputs will be active. When set LOW, the differential signal outputs will mute.
19	SCDT	Non Synchronous	Output	CONTROL SIGNAL OUTPUT Sync detect (active HIGH). Will be set HIGH when a valid signal has been detected at the RXC/$\overline{\text{RXC}}$ pins. NOTE: The SCDT pin can be connected to the OE pin to enable an auto mute upon link inactivity function.
20	D_VDD	Non Synchronous	Power	Digital core power supply. Connect to +3.3V DC.
21, 22	$\overline{\text{TXC}}$, TXC	Analog	Output	Transition minimized differential signal (TMDS) output clock.
23, 30, 31	VDDQ	Analog	Power	Power supply for the differential output cable drivers. Connect to +3.3V DC.
24, 25	$\overline{\text{TX0}}$, TX0	Analog	Output	Transition minimized differential signal (TMDS) data output 0.
26, 27, 34	GNDQ	Analog	Power	Differential output cable driver ground connection.
28, 29	$\overline{\text{TX1}}$, TX1	Analog	Output	Transition minimized differential signal (TMDS) data output 1.
32, 33	$\overline{\text{TX2}}$, TX2	Analog	Output	Transition minimized differential signal (TMDS) data output 2.
35	OUT_SWING	Analog	Input	Differential output signal amplitude. An external 1% resistor connected from this input to GNDQ is used to set the differential output signal amplitude. Use 2kΩ to set the differential output signal swing to 1V.
36, 37	NC	–	–	No connection - leave floating.
38	DDC_GND	Analog	Power	LONG REACH™ DDC ground connection.
39	DDC_VDD	Analog	Power	LONG REACH™ DDC power supply. Connect to +5V DC.
40	DDC_SCL	Non Synchronous	I/O	Connect to display data channel (DDC) buffered serial clock (SCL).
41	DDC_SDA	Non Synchronous	I/O	Connect to display data channel (DDC) buffered serial data (SDA).
42	A_GND	Analog	Power	Analog GND connection.
43	A_VDD	Analog	Power	Analog power supply. Connect to +3.3V DC.

2. Electrical Characteristics

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.3V to +3.6V
Input Voltage Range (any input)	-2.0V to +5.25V
Operating Temperature Range	-20°C to 85°C
Storage Temperature Range	-50°C to 125°C
Lead Temperature (soldering 10 sec.)	260°C

2.1 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

VDD = 3.0V to 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Level	Notes
System								
Operating Temperature Range	T_A	–	0	25	70	°C	–	1
			-20	–	85	°C	–	2
Supply Voltage	VDD	–	3.0	3.3	3.6	V	1	1
Supply Voltage for LONG REACH™ DDC	DDC_VDD	–	4.75	5.0	5.25	V	1	1
Supply Current	I_D	V_{DD} = 3.3V, T_A = 25°C O/P Swing = 1000mV	–	157	–	mA	1	–
Supply Current for LONG REACH™ DDC	–	DDC_VDD = 5V	–	–	15	mA	1	–
System Power	P_D	V_{DD} = 3.3V, T_A = 25°C O/P Swing = 1000mV	–	519	–	mW	5	–
ESD Protection	–	All pins	2	–	–	kV	–	3

Table 2-2: DC Electrical Characteristics (Continued)

VDD = 3.0V to 3.3V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Level	Notes
Digital I/O								
Input Voltage, Logic LOW (OE)	V_{IL}	–	–	–	0.70	V	1	–
Input Voltage, Logic HIGH (OE)	V_{IH}	–	2.0	–	–	V	1	–
Output Voltage, Logic LOW (SCDT)	V_{OL}	Sync Detect Current = +1.25mA	–	–	0.4	V	1	–
Output Voltage, Logic HIGH (SCDT)	V_{OH}	Sync Detect Current = -1.25mA	2.4	–	–	V	1	–
Differential Signal Inputs								
Common Mode Input Voltage Range	V_{CMIN}	–	VDD-0.4	–	VDD	V	6,7	–
Single Ended Standby Input Voltage	–	Transmitter Disabled or Disconnected	–	VDD	–	V	9	–
Differential Signal Outputs								
Common Mode Output Voltage Range	V_{CMOUT}	–	VDD-0.5	–	VDD	–	6,7	4
Single Ended Standby Output Voltage	–	50Ω Loads, Output Muted	–	VDD	–	V	1	–
Single Ended High Level Output Voltage	–	50Ω Loads	–	VDD	–	V	1	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. All DC and AC electrical parameters within specification.
2. Guaranteed functional.
3. MIL STD 883 ESD protection is applied to all pins on the device.
4. Compatible with far end termination at 3.3V or 1.8V.

2.2 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VDD = 3.0V to 3.6V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Level	Notes
System								
Output High Impedance Response Time	t_{RHIGHZ}	OE = LOW	–	20	–	ns	–	–
Additive Jitter	t_{IJ}	1650Mb/s, 2m cable length	–	–	303	ps	1	2
		1650Mb/s, 20m cable length	–	–	303	ps	1	2
DDC Bus Rate	–	Up to 10kΩ pull-up resistors	–	–	400	kHz	2	–
Differential Signal Input								
Serial Input Date Rate	DR_{RX}	–	250	–	1650	Mb/s	–	–
Differential Input Resistance	R_{IN}	–	–	100	–	Ω	1	1
Input Capacitance	C_{IN}	–	–	2	–	pF	–	1
Differential Signal Output — Data Channels								
Serial Output Data Rate	DR_{TX}	–	250	–	1650	Mb/s	–	–
Serial Output Rise/Fall Time	tr, tf	20% ~ 80%	–	145	–	ps	6,7,9	–
Mismatch in Rise/Fall Time	–	–	–	–	5	%	7	–
Serial Output Overshoot	–	Single-Ended, Normalized to Differential p-p	–	9.5	–	%	7	3
Serial Output Undershoot	–	Single-Ended, Normalized to Differential p-p	–	3.1	–	%	7	3
Inter-Channel Skew	–	1650 Mbps, 0m cable	–	0	–	ps	6	–
Differential Output Signal Swing	ΔV_{TX}	R_{LOAD} = 100Ω	200	–	2000	mV_{p-p}	2	–

Table 2-3: AC Electrical Characteristics (Continued)

VDD = 3.0V to 3.6V, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Test Level	Notes
Differential Signal Output — Clock Channel								
Serial Output Data Rate	–	–	25	–	165	MHz	–	–
Serial Output Rise/Fall Time	tr, tf	20% ~ 80%	–	145	–	ps	6,7,9	–
Mismatch in Rise/Fall Time	–	–	–	–	5	%	7	–
Duty-Cycle Distortion	–	–	–	–	2	%	7	–
Differential Output Signal Swing Range	ΔV_{TXC}	R_{LOAD} = 100Ω Range controlled using external resistor	200	–	2000	mV	2	–

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. Includes pin and bonding parasitics.
2. See Typical Additive Jitter vs. Cable Length graph below
3. Based on Gennum's characterization board

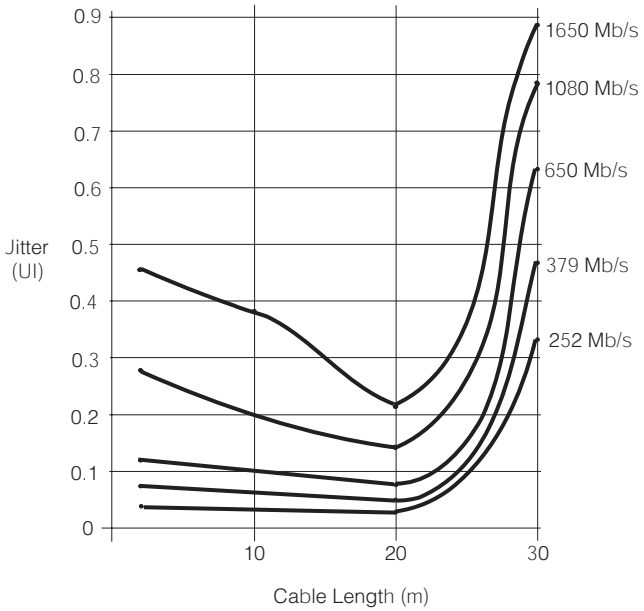


Figure 2-1: Typical Additive Jitter vs. Cable Length

3. Detailed Description

3.1 Differential Inputs

The GS8000 contains four current mode differential signal input buffers. These allow the device to be connected to a DVI 1.0 compliant data stream consisting of three transition minimized differential signals (TMDS) and a clock signal at one tenth the data rate.

All input buffers have internal user programmable input termination pull-up resistors. A resistor value of 500Ω should be connected between the EXT_RES pin and D_GND to set the input termination to 50Ω.

The input buffers use a separate power supply of +3.3V DC (VDD and GND) and have a wide common mode operating point.

3.2 LONG REACH™ DVI / HDMI

3.2.1 LONG REACH™ TMDS

Gennum's patented DVI technology restores the received signals to the input level defined in the DVI 1.0 and HDMI 1.1 specifications.

Four gain stages are provided, three of which extend TMDS data at rates from 250Mb/s to 1.65Gb/s. The fourth gain stage is optimized to extend the clock signal at one tenth the received TMDS data rate.

These stages operate under the assumption that the input signal was launched at an amplitude of between 800mV and 1200mV differential.

3.2.2 LONG REACH™ DDC

The DDC Extend block manages DDC traffic in both directions by restoring incoming signals and boosting outgoing signals to meet the DDC specification.

Connect the DDC_SDA and DDC_SCL pins to the DDC bus at the closest location to the GS8000. See Figure 3-2: LONG REACH™ DVI or HDMI Receive Solution.

NOTE: If a level shifter is necessary, the GS8000 must be placed on the 5V side (connector side) as shown in Figure 3-2: LONG REACH™ DVI or HDMI Receive Solution.

NOTE: The 5V present on the DVI and HDMI connectors can be significantly reduced over long ranges of cable. Therefore, it is recommended that this voltage not be used as the supply voltage for the LONG REACH™ DDC.

3.3 Differential Outputs

The GS8000 contains four current mode differential signal output buffers capable of driving a DVI 1.0-compliant or HDMI 1.1-compliant receiver. The TMDS outputs are compatible with the DVI 1.0 or HDMI 1.1 specifications for input common mode and swing.

The signal swing of each output is adjustable from 200mV to 2000mV differential for a 100Ω load. An external 1% resistor connected from the OUT_SWING pin to GNDQ sets the differential output signal amplitude.

NOTE: The differential outputs are designed to interface directly to a DVI 1.0-compliant or HDMI 1.1-compliant receiver. They are not buffered to drive any cable.

All differential outputs can be muted by setting the OE pin LOW. In this case, the output buffers will become high impedance and device power will be reduced.

The output buffers use a separate power supply of +3.3V DC at the VDDQ and GNDQ pins.

3.4 Signal Monitoring and Control

The signal monitoring and control block analyzes the signal received at the RXC and $\overline{\text{RXC}}$ pins.

3.4.1 Sync Detect Output

When a valid signal is detected at the RXC/$\overline{\text{RXC}}$ pins, the sync detect (SCDT) output pin will be set HIGH.

3.4.2 Output Enable

The GS8000's differential signal outputs may be muted by setting the OE pin LOW. This causes the output buffers to become high impedance.

To implement an auto mute on loss of input function, the SCDT output pin can be connected externally to the OE input.

3.5 System Considerations

3.5.1 Device Power Up

Because the GS8000 was designed to operate in a multi-volt environment, any power up sequence is allowed. The internal core and differential signal I/O buffers may be powered up in any order.

Device pins may also be driven prior to power up without causing damage.

3.5.2 ESD Protection

The GS8000 has 2kV ESD protection on all pins. In addition, the device was designed to work with ESD diodes on the input connectors. These external diodes work with the chip to significantly increase overall system ESD protection.

The ESD diodes used in Gennum's Application Reference Design (4.2 ESD Diodes) provide ESD protection of greater than 8kV through air (test conducted in accordance with IEC 61000-4-2 standard "Electrostatic Discharge Immunity Test").

3.5.3 Cable Use

The GS8000 was designed for best performance when used with DVI 1.0-compliant and HDMI 1.1-compliant cables meeting the approximate loss characteristic shown in Figure 3-1: Cable Loss Characteristic.

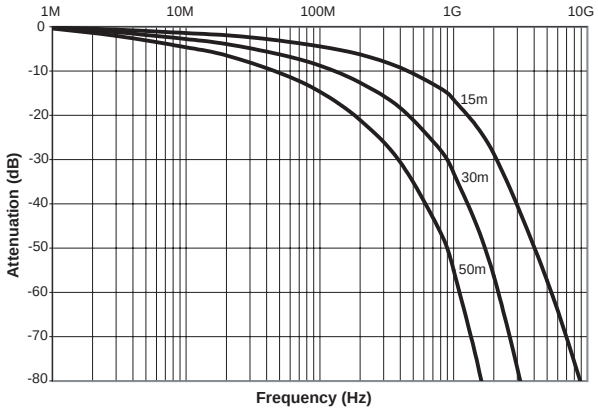


Figure 3-1: Cable Loss Characteristic

While the GS8000 will extend a range of DVI cable types and qualities, the device gives optimum performance when used to extend high-quality cable.

Important parameters to consider when choosing a high quality DVI cable include inter-pair and intra-pair skew. Cable length extension is maximized when cable with low inter-pair and intra-pair skew is used. The GS8000 does not add significant amounts of intra-pair or inter-pair skew. However, the skew added by some long DVI cables can exceed the tolerance of some DVI receivers.

3.5.4 Complete LONG REACH™ Receive Solution

Figure 3-2: LONG REACH™ DVI or HDMI Receive Solution shows a complete DVI / HDMI receive solution implementing the GS8000 with a DVI or HDMI Receiver and local EDID PROM.

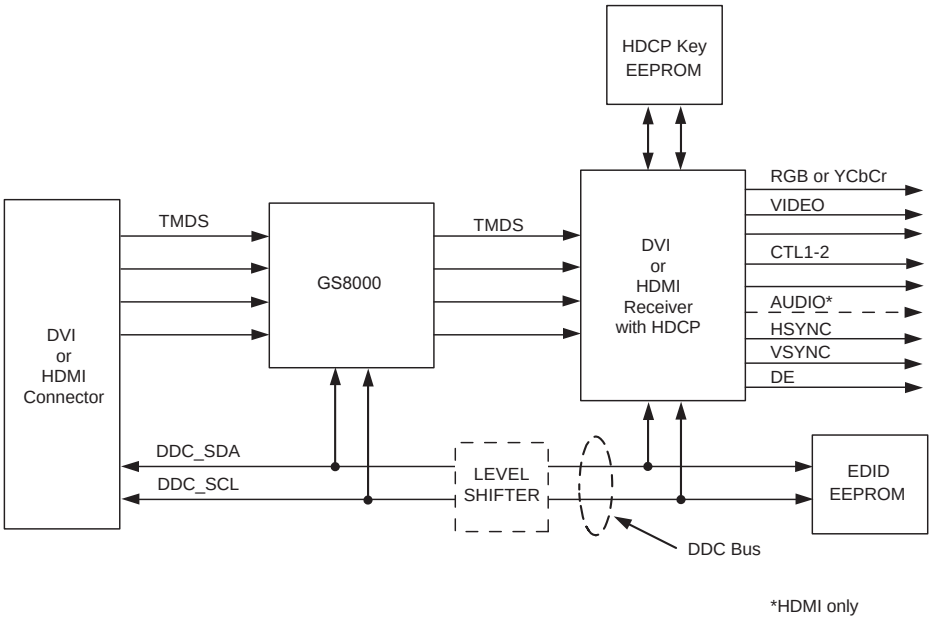
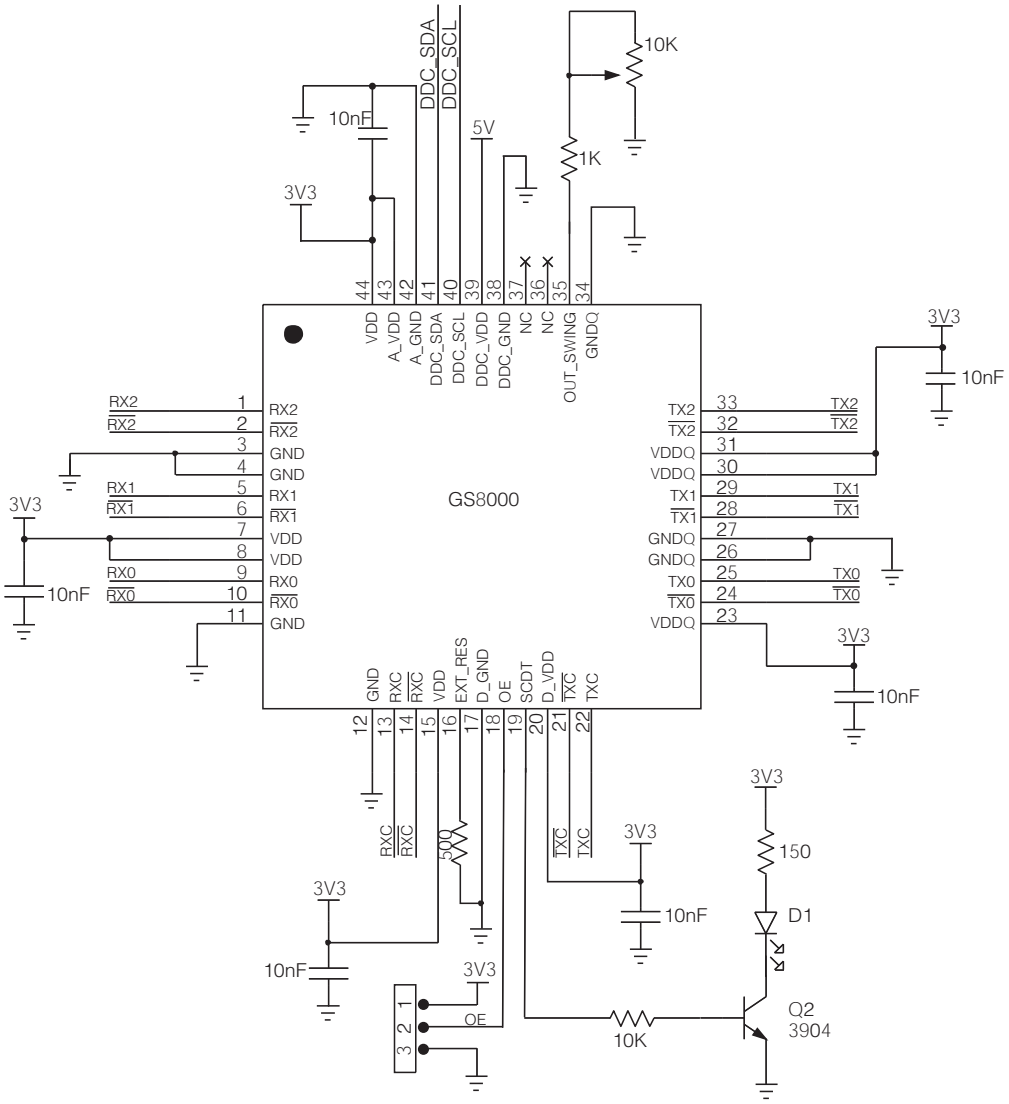


Figure 3-2: LONG REACH™ DVI or HDMI Receive Solution

4. Application Reference Design

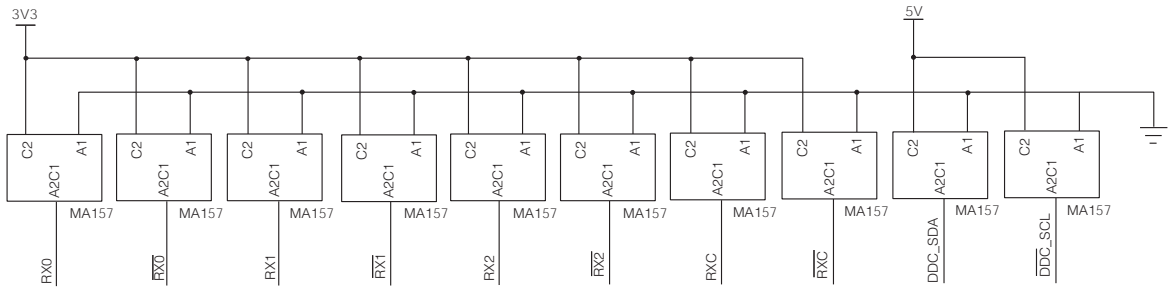
4.1 Typical Application Circuit



Notes
1. The GS8000 must always be used with a DVI receiver. Do not concatenate two equalizers without reclocking in between. If the GS8000 is to be used directly in front of another device with internal equalization, disable the equalization on that device.
2. Adding proper decoupling capacitors between power supplies and ground is critical to the proper performance and operation of the GS8000.

Figure 4-1: Typical application circuit

4.2 ESD Diodes



Note: For the DDC link to be active when the device is powered down, the 5V power to the DDC ESD diodes must be supplied by the DVI transmitter.

4.3 PCB Layout

Special attention must be paid to component layout when designing DVI 1.0-compliant HDMI 1.1-compliant interfaces. The following layout recommendations are to ensure optimal performance of the GS8000.

- Signal traces for TMDS DATA and CLOCK channels must be 100Ω differential controlled impedance traces.
- Differential signal trace spacing should be kept consistent throughout the entire trace length. Traces should be curved to minimize impedance changes.
- An FR-4 dielectric may be used.
- The GS8000 should be placed as close as possible to the input connector, and the trace length from connector to device should be kept as short as possible.
- All differential signal traces should be kept on the same PCB layer as the GS8000.
- External ESD protection diodes should be fast switching with a small terminal capacitance (less than or equal to 2pF). Panasonic's MA157A or similar switching diodes are recommended.
- Placing sufficiently large power and ground planes in board layout is critical to the proper performance and operation of the GS8000.

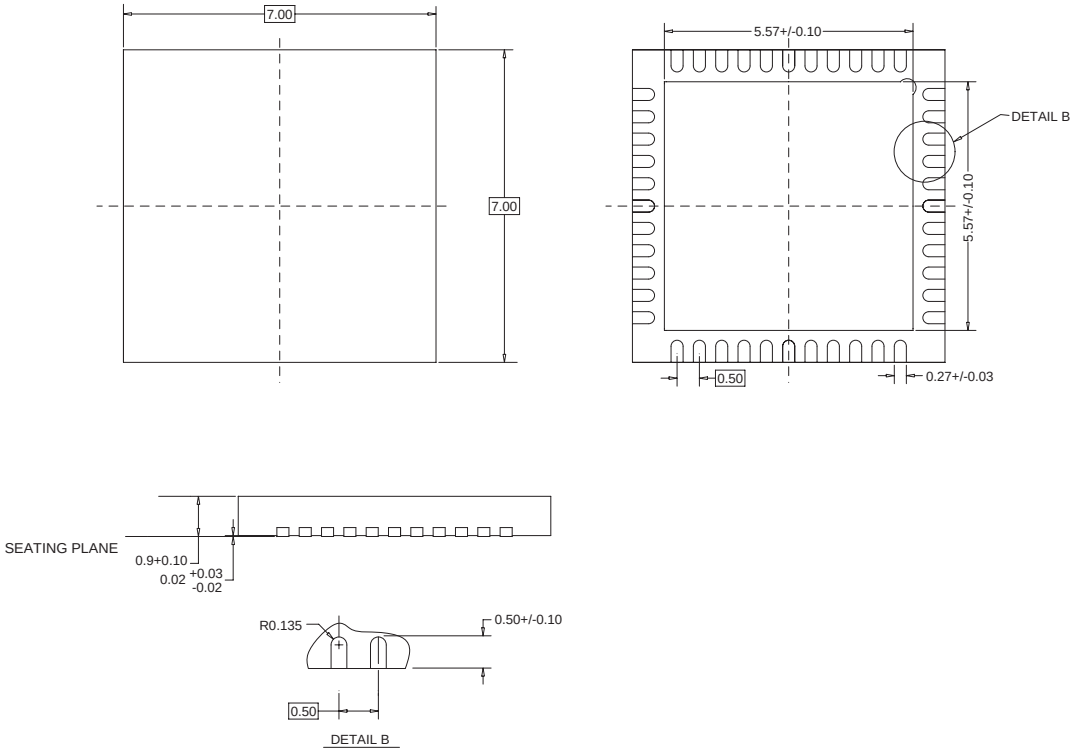
5. References

Digital Visual Interface — DVI (Digital Display Working Group - Revision 1.0, 02 April 1999).

HIgh-Definition Multimedia Interface — HDMI (HDMI Licensing LLC - Revision 1.1, 20 May 2004).

6. Package & Ordering Information

6.1 Package Dimensions



6.2 Ordering Information

Part Number	Package	Temperature Range	Max Pixel Clock Rate
GS8000ACNE3	44-PIN QFN	0°C to 70°C	165 MHz

7. Revision History

Version	ECR	Date	Changes and/or Modifications
0	132311	October 2003	Modify specified values based on characterization. Turn into Preliminary Data Sheet.
1	133756	June 2004	Modify DC Electrical characteristics and Section 3.5.2. Update package dimensions. Add note to Section 3.3 and Section 4.2.
2	134675	September 2004	Included references to HDMI interface in text and in diagrams. Removed hyphens from LONG-REACH trademark text. Added technical information of powerplane and power supply decoupling.
3	135724	May 2005	GS8000 has an ESD Protection of 2kV.

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The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

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