



# CMOS Static RAM 16K (4K x 4-Bit)

**IDT6168SA**  
**IDT6168LA**

## Features

- ◆ High-speed (equal access and cycle time)
  - Military: 25/45ns (max.)
  - Industrial: 25ns (max.)
  - Commercial: 15/20/25ns (max.)
- ◆ Low power consumption
- ◆ Battery backup operation—2V data retention voltage (IDT6168LA only)
- ◆ Available in high-density 20-pin ceramic or plastic DIP and 20-pin leadless chip carrier (LCC)
- ◆ Produced with advanced CMOS high-performance technology
- ◆ CMOS process virtually eliminates alpha particle soft-error rates
- ◆ Bidirectional data input and output
- ◆ Military product compliant to MIL-STD-883, Class B

## Description

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability

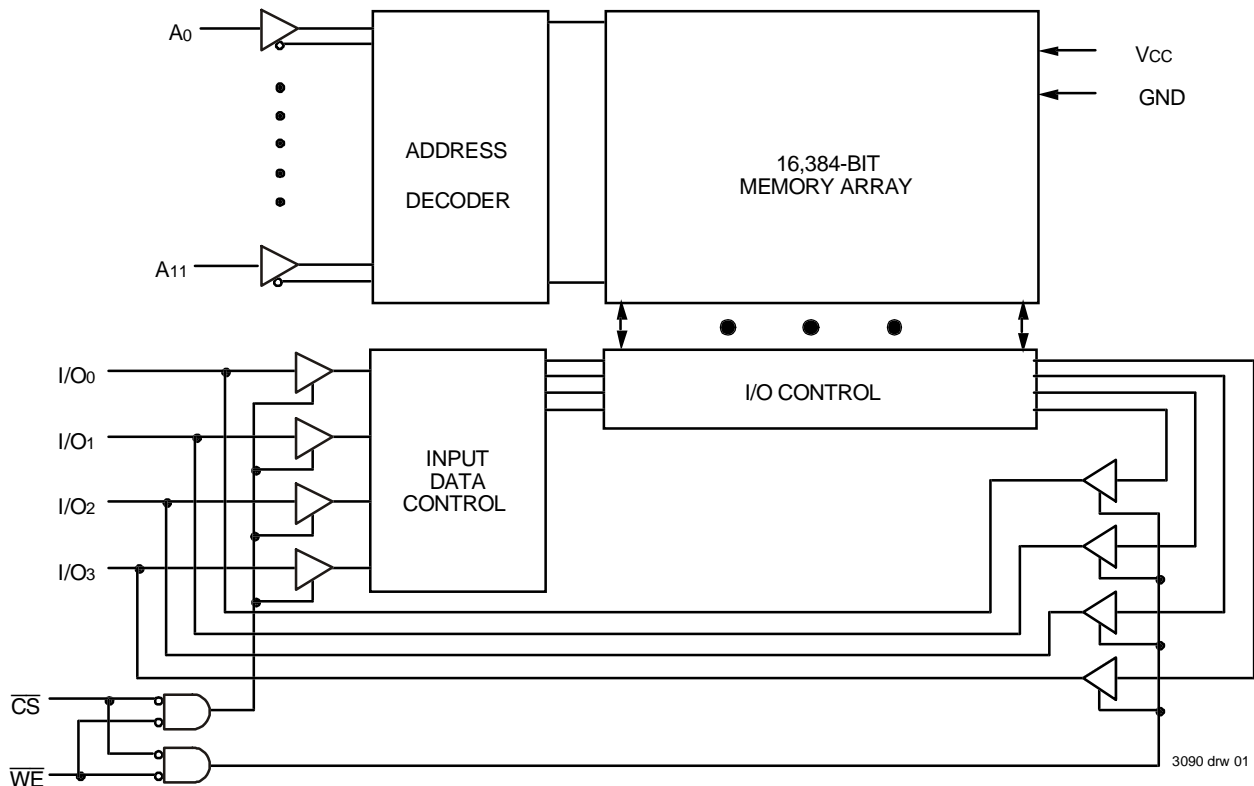
CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

Access times as fast 15ns are available. The circuit also offers a reduced power standby mode. When  $\overline{CS}$  goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as  $\overline{CS}$  remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1 $\mu$ W operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300-mil ceramic or plastic DIP or a 20-pin LCC providing high board-level packing densities.

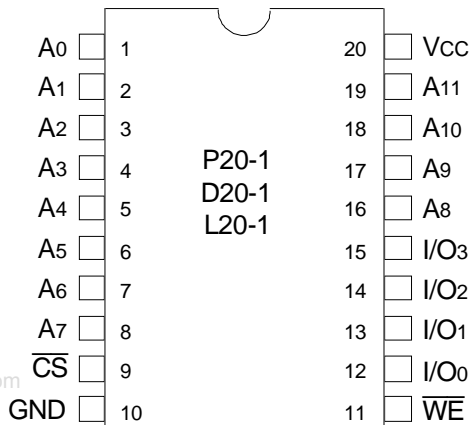
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## Functional Block Diagram



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## Pin Configurations



3090 drw 02

### DIP/LCC Top View

## Pin Descriptions

Name	Description
A <sub>0</sub> - A <sub>11</sub>	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O <sub>0</sub> - I/O <sub>3</sub>	Data Input/Output
V <sub>CC</sub>	Power
GND	Ground

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## Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	7	pF
C <sub>IO</sub>	I/O Capacitance	V <sub>OUT</sub> = 0V	7	pF

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**NOTE:**

- This parameter is determined by device characterization, but is not production tested.

## Truth Table<sup>(1)</sup>

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	D <sub>OUT</sub>	Active
Write	L	L	D <sub>IN</sub>	Active

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**NOTE:**

- H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't Care

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Com'l.	Mil.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

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**NOTE:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

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**NOTE:**

- V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns, once per cycle.

## Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	V <sub>CC</sub>
Military	-55°C to +125°C	0V	5V ± 10%
Industrial	-45°C to +85°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

3090 tbl 06

**DC Electrical Characteristics<sup>(1)</sup>**  
**(V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)**

Symbol	Parameter	Power	6168SA15		6168SA20 6168LA20		6168SA25 6168LA25		6168SA45 6168LA45		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l. & Ind.	Mil.	Com'l.	Mil.	
I <sub>CC1</sub>	Operating Power Supply Current $\overline{CS} \leq V_{IL}$ , Outputs Open V <sub>CC</sub> = Max., f = 0 <sup>(2)</sup>	SA	110	—	90	—	90	100	—	100	mA
		LA	—	—	70	—	70	80	—	80	
I <sub>CC2</sub>	Dynamic Operating Current $\overline{CS} \leq V_{IL}$ , Outputs Open V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>	SA	145	—	120	—	110	120	—	110	mA
		LA	—	—	100	—	90	100	—	80	
I <sub>SB</sub>	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$ , Outputs Open V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>	SA	55	—	45	—	35	45	—	35	mA
		LA	—	—	30	—	25	30	—	25	
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$ , V <sub>CC</sub> = Max., V <sub>IN</sub> ≤ V <sub>LC</sub> or V <sub>IN</sub> ≥ V <sub>HC</sub> , f = 0 <sup>(2)</sup>	SA	20	—	20	—	3	10	—	10	mA
		LA	—	—	0.5	—	0.5	0.3	—	0.3	

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NOTES:

- All values are maximum guaranteed values.
- f<sub>MAX</sub> = 1/trc, only address inputs are cycling at f<sub>MAX</sub>. f = 0 means no address inputs are changing.

**DC Electrical Characteristics**  
**V<sub>CC</sub> = 5.0V ± 10%**

Symbol	Parameter	Test Conditions	IDT6168SA		IDT6168LA		Unit
			Min.	Max.	Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	—	10 2	—	5 2	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS} = V_{IH}$ , V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	10 2	—	5 2	μA
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.	—	0.5	—	0.5	V
		I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	—	0.4	—	0.4	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	—	2.4	—	V

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### Data Retention Characteristics (LA Version Only)

$V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$

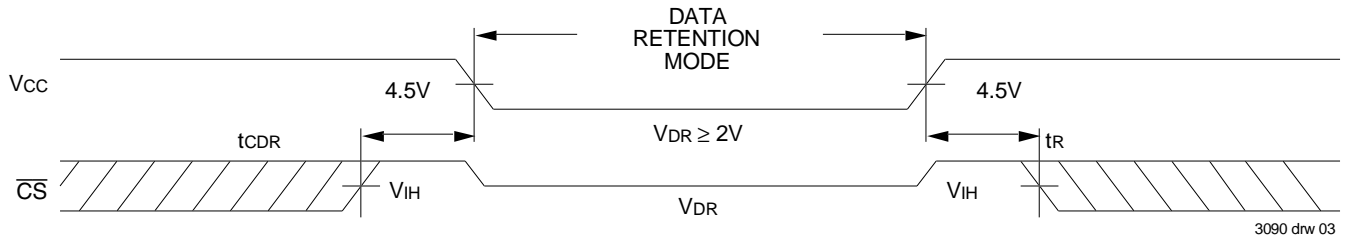
Symbol	Parameter	Test Condition	IDT6168LA			Unit	
			Min.	Typ. <sup>(1)</sup>	Max.		
$V_{DR}$	$V_{CC}$ for Data Retention	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	2.0	—	—	V	
$I_{CDR}$	Data Retention Current		MIL.	—	0.5 <sup>(2)</sup> 1.0 <sup>(3)</sup>	100 <sup>(2)</sup> 150 <sup>(3)</sup>	$\mu A$
			COM'L.	—	0.5 <sup>(2)</sup> 1.0 <sup>(3)</sup>	20 <sup>(2)</sup> 30 <sup>(3)</sup>	$\mu A$
$t_{CDR}^{(5)}$	Chip Deselect to Data Retention Time		0	—	—	ns	
$t_{R}^{(5)}$	Operation Recovery Time		$t_{RC}^{(4)}$	—	—	ns	

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**NOTES:**

1.  $T_A = +25^\circ C$ .
2. at  $V_{CC} = 2V$
3. at  $V_{CC} = 3V$
4.  $t_{RC}$  = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

### Low $V_{CC}$ Data Retention Waveform

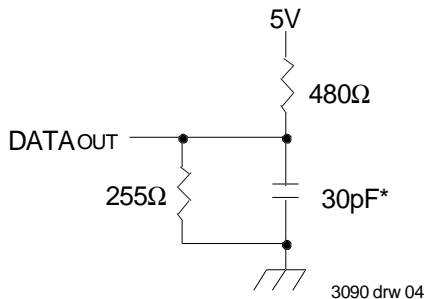


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### AC Test Conditions

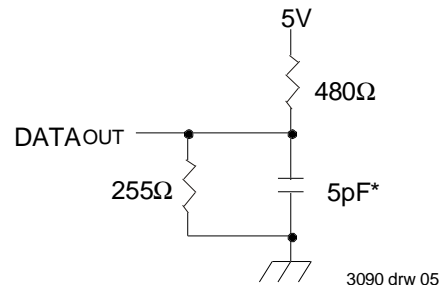
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

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Figure 1. AC Test Load



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Figure 2. AC Test Load  
(for tCHZ, tCLZ, tWHZ and tOW)

\*Includes scope and jig capacitances

### AC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%, All Temperature Ranges)

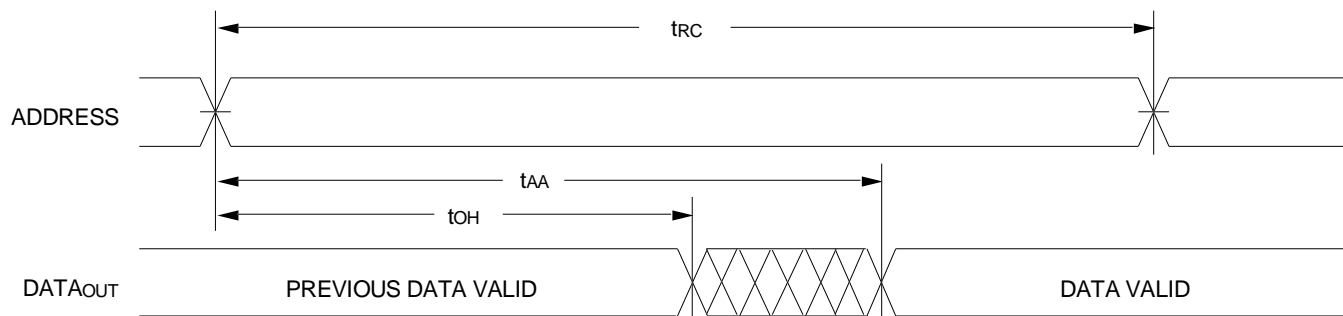
Symbol	Parameter	6168SA15 <sup>(1)</sup>		6168SA20 <sup>(1)</sup> 6168LA20 <sup>(1)</sup>		6168SA25 6168LA25		6168SA45 <sup>(2)</sup> 6168LA45 <sup>(2)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	15	—	20	—	25	—	45	—	ns
t <sub>AA</sub>	Address Access Time	—	15	—	20	—	25	—	45	ns
t <sub>ACS</sub>	Chip Select Access Time	—	15	—	20	—	25	—	45	ns
t <sub>CLZ</sub> <sup>(3)</sup>	Chip Select to Output in Low-Z	3	—	5	—	5	—	5	—	ns
t <sub>CHZ</sub> <sup>(3)</sup>	Chip Deselect to Output in High-Z	—	8	—	10	—	10	—	25	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t <sub>PU</sub> <sup>(3)</sup>	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(3)</sup>	Chip Deselect to Power Down Time	—	35	—	20	—	25	—	40	ns

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**NOTES:**

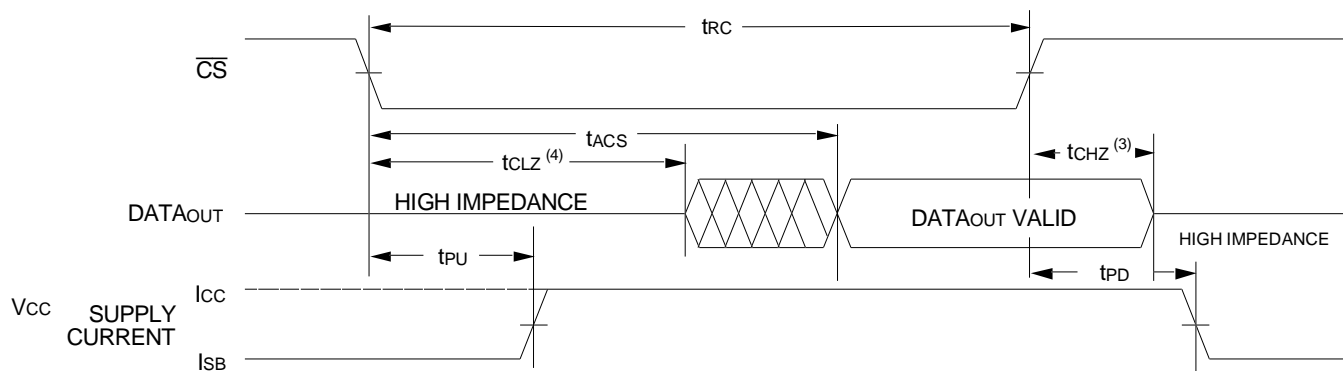
- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter is guaranteed with AC Test load (Figure 2) by device characterization, but is not production tested.

### Timing Waveform of Read Cycle No. 1<sup>(1, 2)</sup>



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### Timing Waveform of Read Cycle No. 2<sup>(1, 3)</sup>



3090 drw 07

**NOTES:**

- $\overline{WE}$  is HIGH for Read cycle.
- $\overline{CS}$  is LOW for Read cycle.
- Device is continuously selected,  $\overline{CS}$  is LOW.
- Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
- Transition is measured ±200mV from steady state.

### AC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%, All Temperature Ranges)

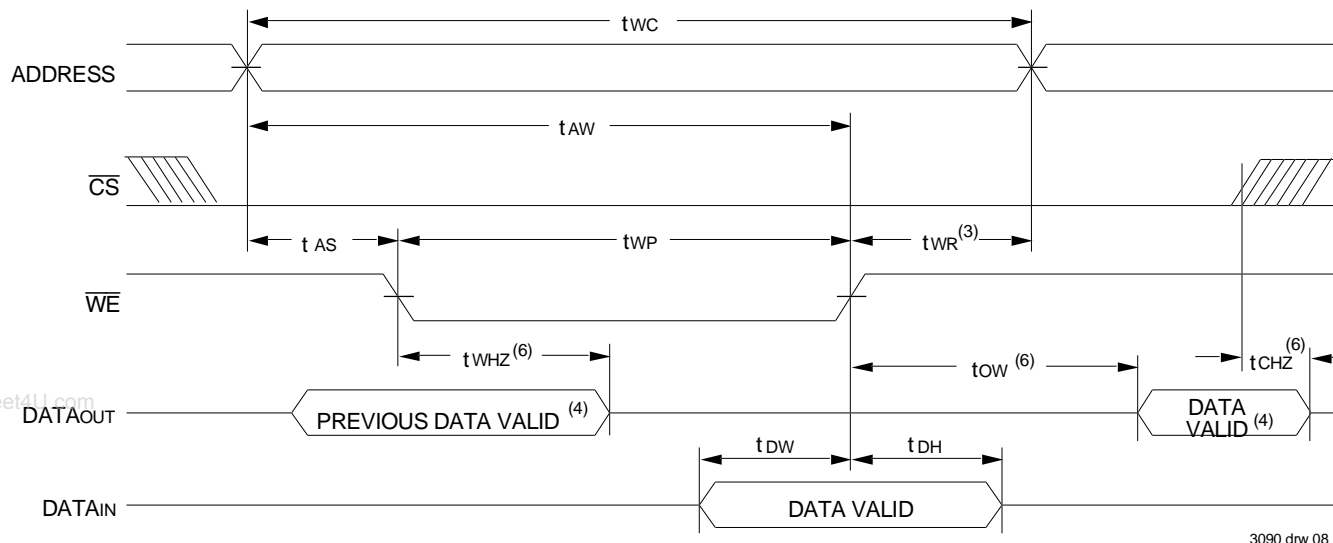
Symbol	Parameter	6168SA15 <sup>(1)</sup>		6168SA20 <sup>(1)</sup> 6168LA20 <sup>(1)</sup>		6168SA25 6168LA25		6168SA45 <sup>(2)</sup> 6168LA45 <sup>(2)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Cycle</b>										
t <sub>WC</sub>	Write Cycle Time	15	—	20	—	20	—	40	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	15	—	20	—	20	—	40	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	15	—	20	—	20	—	40	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	15	—	20	—	20	—	40	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data to Valid to End-of-Write	9	—	10	—	10	—	20	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	3	—	ns
t <sub>WHZ</sub> <sup>(3)</sup>	Write Enable to Output in High-Z	—	6	—	7	—	7	—	20	ns
t <sub>OW</sub> <sup>(3)</sup>	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

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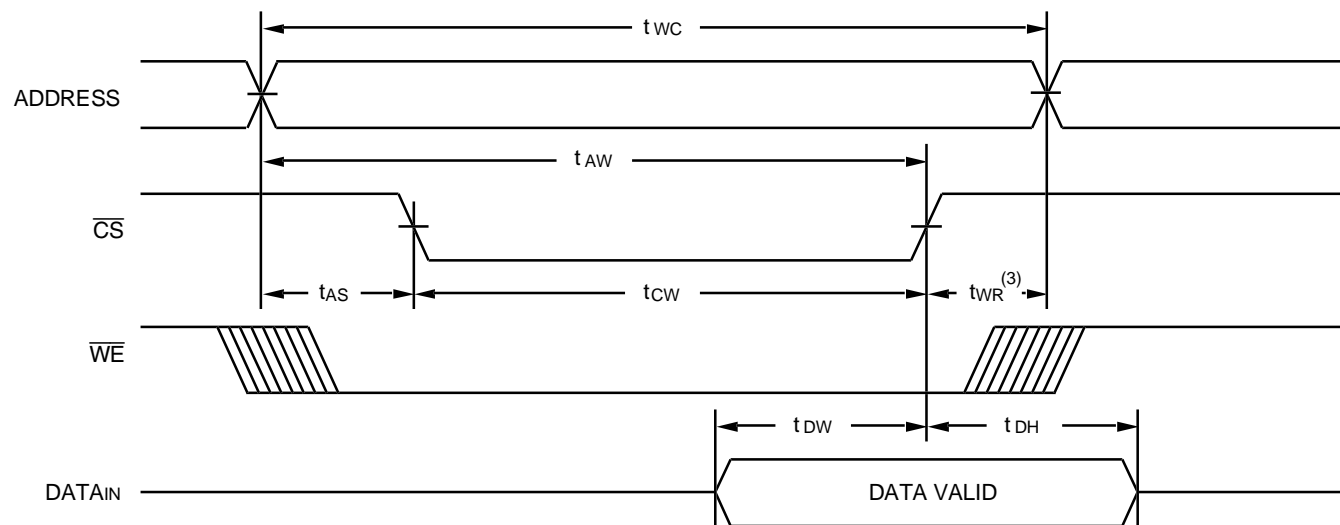
**NOTES:**

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

### Timing Waveform of Write Cycle No. 1 ( $\overline{WE}$ Controlled Timing)<sup>(1,2,5)</sup>



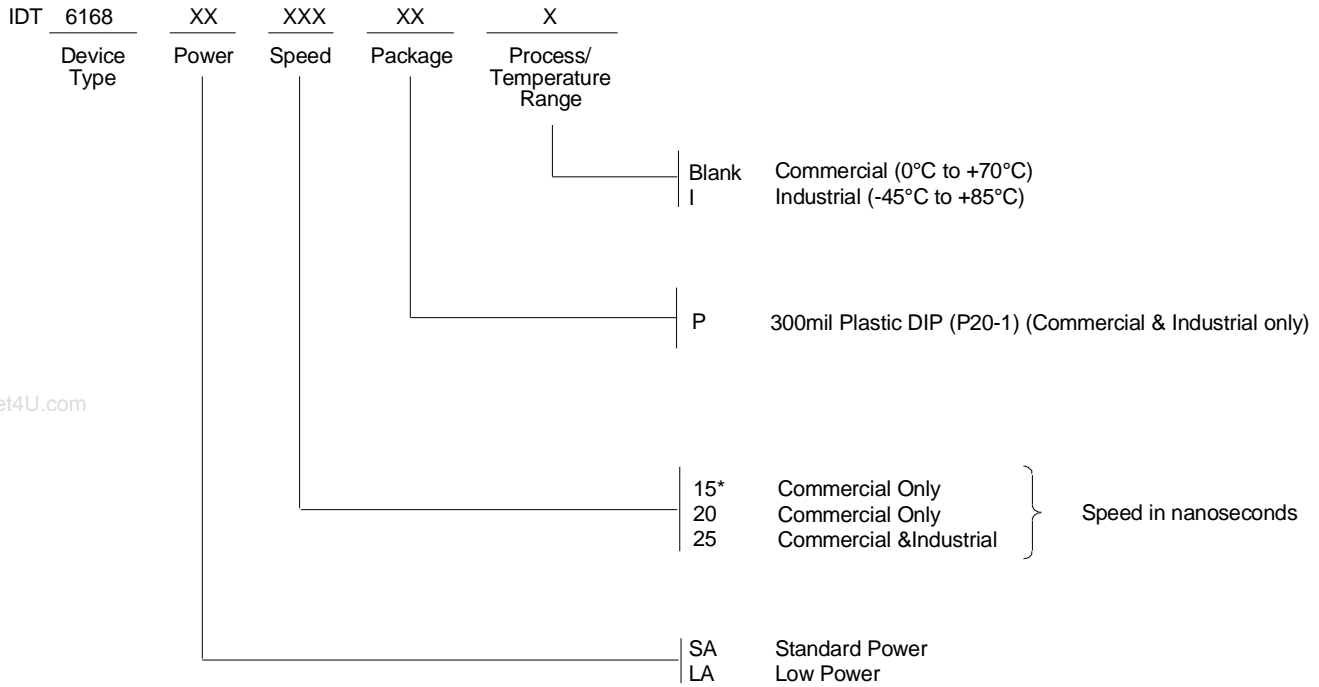
### Timing Waveform of Write Cycle No. 2 ( $\overline{CS}$ Controlled Timing)<sup>(1,2,5)</sup>



**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in the high impedance state.
6. Transition is measured  $\pm 200\text{mV}$  from steady state.

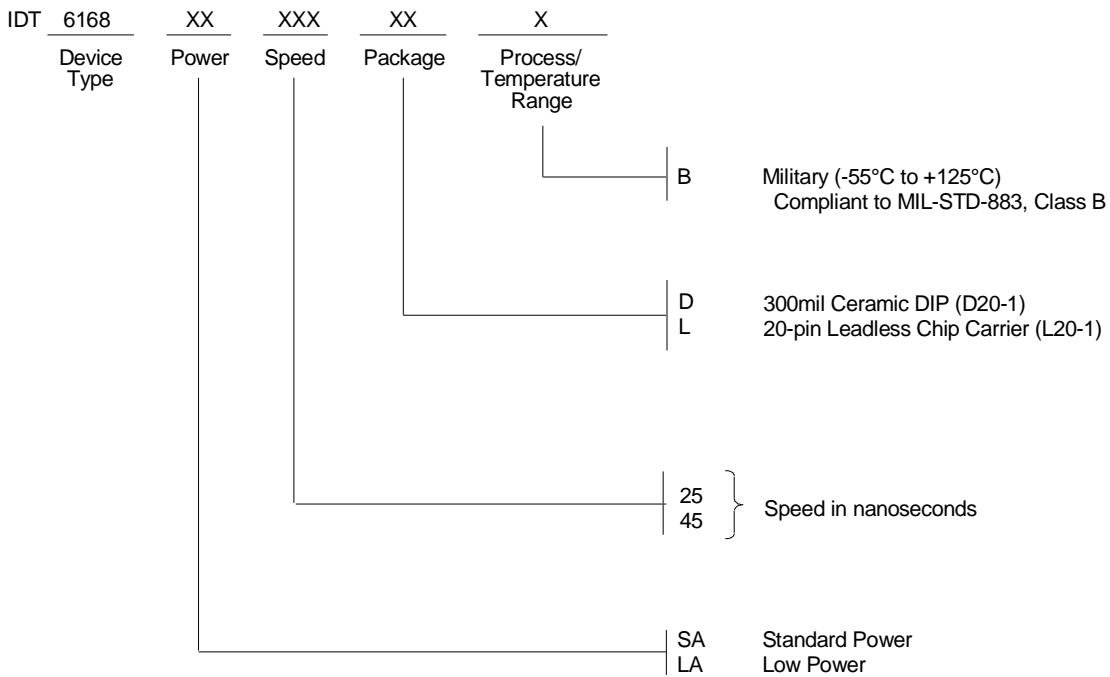
### Ordering Information -- Commercial & Industrial



\*Standard power only.

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### Ordering Information -- Military



\*Standard power only.

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## Datasheet Document History

11/22/99		Updated to new format
	Pg. 8	Added Datasheet Document History
	Pg. 1, 2, 3, 5, 6, 8	Added Industrial Temperature range offerings
01/07/00		Revised package offerings
08/09/00	Pg. 1, 2, 8	Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"



**CORPORATE HEADQUARTERS**  
2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**  
800-345-7015 or 408-727-6116  
fax:408-492-8674  
www.idt.com

**for Tech Support:**  
sramhelp@idt.com  
800 544-7726, x4033

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