Voltage Detector with ON/OFF Control of the Watchdog

FEATURES

- Detect Voltage Range 1.6 V – 5.0 V in 0.1 V increments
- Accuracy ± 2%
- Hysteresis 5% (typical)
- Low Power Consumption
  0.4 µA (Detect at V_{IN} = 1.0 V)
  0.6 µA (Release at V_{IN} = 1.0 V)
- Operating Voltage Range 1.0 V – 6.0 V
- Detect Voltage Temperature Drift ±100 ppm/^{0}C
- Output Configuration - N-channel Open Drain
- Watchdog with ON/OFF Control
- Pre-programmed Release Time of 3.13, 50, 100, 200, and 400 ms
- Pre-programmed Watchdog Time of 50, 100, 200, 400, 800, and 1600 ms
- Operating Ambient Temperature - 40 + 85^{0}C
- Packages : USP-6C and SOT-25
- EU RoHS Compliant, Pb Free

APPLICATIONS

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors

DESCRIPTION

The IXD5121/22/23/24 are highly precise, low power consumption, CMOS voltage detectors with watchdog function, manufactured using laser trimming technology.

The series consists of a reference voltage source, delay circuit, comparator, and output driver. With the built-in delay circuit, this series does not require any external components.

The $\overline{RESET}$ output is active LOW, when voltage below V_{DFL} is detected.

The EN ($\overline{EN}$) pin controls the ON/OFF state of the watchdog functions. This pin in an active state disables the watchdog function, while the voltage detector remains operational.

The IXD5122 and IXD5124 series have internal pull-up/down resistors respectively that allows use these IC with watchdog function active, while EN ($\overline{EN}$) pins are left open.

The detect voltages are internally fixed in the range of 1.6 V to 5.0 V in 0.1 V increments.

Six watchdog timeout periods are available in a range of 50 ms to 1.6 s.

Five release delay times are available in a range of 3.13 ms to 400 ms.

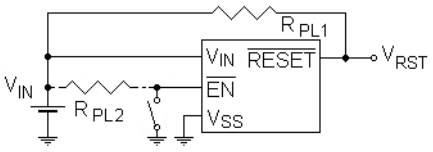
With low power consumption and high accuracy, the series is suitable for precision mobile equipment.

The IXD5121/22/23/24 in ultra small packages are ideally suited for high-density PC boards.

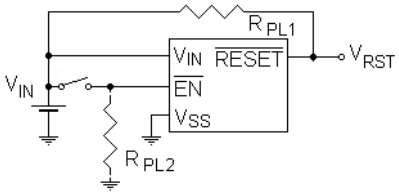
The IXD5121/22/23/24 is available in N-channel open drain output configuration only.

These detectors are available in USP-6C and SOT-25 packages.

TYPICAL APPLICATION CIRCUIT



IXD5121/22 Application Circuit (R_{PL2} is used with IXD5121 only)



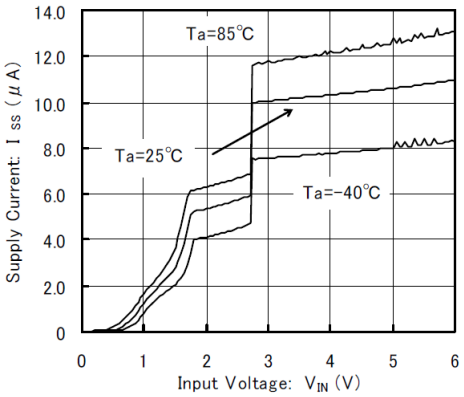
IXD5123/24 Application Circuit (R_{PL2} is used with IXD5123 only)

TYPICAL PERFORMANCE CHARACTERISTIC

Supply Current vs. Input Voltage

IXD5121 - 4

V_{DF} = 2.7 V



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	– 0.3 ~ +7.0	V
Output Current		I_{OUT}	20	mA
Output Voltage		V_{RST}	– 0.3 ~ +7.0	V
EN/($\overline{EN}$) Pin Voltage		V_{EN}	– 0.3 ~ V_{IN} + 0.3 ≤ 7.0	V
WD Pin Voltage		V_{WD}	– 0.3 ~ +7.0	
Power Dissipation	USP-6C	P_D	120	mW
	SOT-25		250	
Operating Temperature Range		T_{OPR}	– 40 ~ + 85	^{0}C
Storage Temperature Range		T_{STG}	– 55 ~ +125	^{0}C

All voltages are in respect to V_{SS}

ELECTRICAL OPERATING CHARACTERISTICS

Ta = 25 ^{0}C

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
Operating Voltage	V_{IN}	$V_{DF(T)}$ = 0.8 – 5.0 V[1]		1.0		6.0	V	①
Detect Voltage	V_{DF}	Watchdog disabled		$V_{DFL(T}$ x 0.98$_{)}$	$V_{DFL(T)}$	$V_{DFL(T)}$ x 1.02	V	①
Hysteresis Width	V_{HYS}	Watchdog disabled		V_{DFL} x 0.02	V_{DFL} x 0.05	V_{DFL} x 0.08	V	①
Supply Current[2]	I_{SS}	WD = Open	V_{IN} = V_{DFL} x 0.9 V		5	11	µA	②
			V_{IN} = V_{DFL} x 1.1 V		10	16		
			V_{IN} = 6.0 V		12	18		
Output Current	I_{OUT}	V_{DS} = 0.5 V N-channel MOSFET	V_{IN} = 1.0 V	0.15	0.5		mA	③
			V_{IN} = 2.0 V, $V_{DFL(T)}$ > 2.0 V	2.0	2.5			
			V_{IN} = 3.0 V, $V_{DFL(T)}$ > 2.0 V	3.0	3.5			
			V_{IN} = 4.0, $V_{DFL(T)}$ > 2.0 V	3.5	4.0			
Leakage Current	I_{LEAK}	V_{IN} = V_{RST} = 6.0 V			-0.01	0.1	µA	③
Detect Voltage Temperature Characteristics	$\frac{\Delta V_{DF}}{V_{DF} * \Delta T_{OPR}}$	- 40 ^{0}C ≤ T_{OPR} ≤ 85 ^{0}C			± 100		ppm/^{0}C	①
Release Delay Time[1]	t_{DR}	V_{DFL} ≤ 1.8 V		2.00	3.13	5.00	ms	④
				37	50	63		
				75	100	125		
				150	200	250		
				300	400	500		
Release Delay Time[2]	t_{DR}	V_{DFL} ≥ 1.9 V		2.00	3.13	5.00	ms	④
				37	50	63		
				75	100	125		
				150	200	250		
				300	400	500		
Detect Delay Time[8]	t_{DF}	WD = Open			5.5	33	µs	④
Watchdog Timeout[4]	t_{WD}	V_{DFL} ≤ 1.8 V		37	50	63	ms	⑤
				75	100	125		
				150	200	250		
				300	400	500		
				600	800	1000		
				1200	1600	2000		
Watchdog Timeout[4]	t_{WD}	V_{DFL} ≥ 1.9 V		37	50	63	ms	⑤
				75	100	125		
				150	200	250		
				300	400	500		
				600	800	1000		
				1200	1600	2000		
Watchdog Minimum Pulse Width	T_{WDIN}	V_{IN} = 6.0 V, Pulse Amplitude = 6.0 V		300			ns	⑥
WD Pin Voltage Level	High	V_{WDH}	V_{IN} = V_{DFL} x 1.1 V – 6.0 V	V_{IN} x 0.7		6.0	V	⑥
	Low	V_{WDL}	V_{IN} = V_{DFL} x 1.1 V – 6.0 V	0		V_{IN} x 0.3		
WD Pin Resistance	R_{WD}	V_{IN} = 6.0 V, R_{WD} = V_{WD}/I_{WD}		300	600	900	kΩ	⑦

ELECTRICAL OPERATING CHARACTERISTICS (CONTINUED)

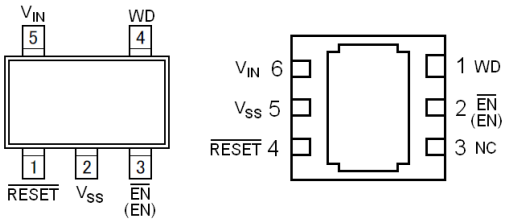
Ta = 25 °C

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	CIRCUIT
EN Pin Voltage Level	High	V_{ENH}	$V_{IN} = V_{DFL}$ x 1.1 V – 6.0 V	1.3		V_{IN}	V	⑧
	Low	V_{ENL}	$V_{IN} = V_{DFL}$ x 1.1 V – 6.0 V	0		0.35		
EN Pull-up Resistance[3]		R_{EN}	V_{IN} = 6.0 V, V_{EN} = 0, $R_{EN} = V_{EN}/I_{EN}$	1.0	1.6	2.4	MΩ	⑨
$\overline{EN}$ Pull-down Resistance[4]		R_{EN}	V_{IN} = 6.0 V, V_{EN} = 6.0 V, $R_{EN} = V_{EN}/I_{EN}$	1.0	1.6	2.4	MΩ	⑨

NOTE:

In case, where no EN/ ($\overline{EN}$) pin's condition is written in the test condition field, $V_{EN} = V_{IN}$ for EN pin and V_{EN} = 0 V for $\overline{EN}$ pin.

1) $V_{DF(T)}$ is a nominal detect voltage
2) Watchdog is in ON state. At watchdog in off state, Supply current increases by EN/ ($\overline{EN}$) pin leakage current, if it is tied to V_{IN}.
3) IXD5122 series only
4) IXD5124 series only



The dissipation pad for the USP-6C package should be solder-plated in reference mount pattern and metal masking to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the VSS (No. 5) pin.

PIN CONFIGURATION

SOT-25
(TOP VIEW)

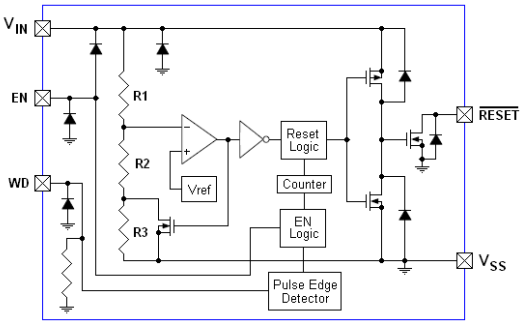
USP-6C
(BOTTOM VIEW)

PIN ASSIGNMENT

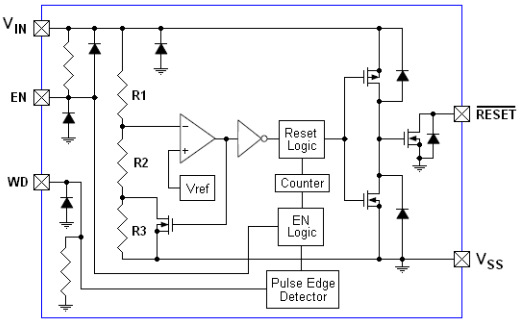
PIN NUMBER		PIN NAME	FUNCTIONS
USP-6C	SOT-25		
4	1	$\overline{RESET}$	Output Voltage (Detect "LOW")
5	2	V_{SS}	Ground
2	3	EN ($\overline{EN}$)	Watchdog Enable Input
1	4	WD	Watchdog Input
6	5	V_{IN}	Power Input
3		NC	No Connection

BLOCK DIAGRAMS

IXD5121

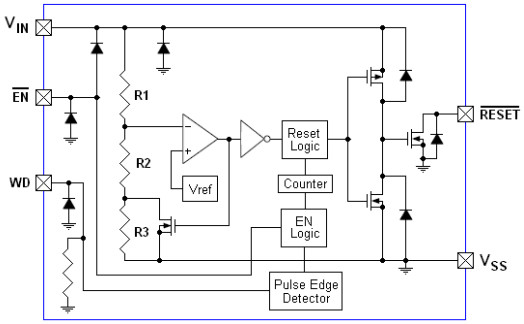


IXD5122

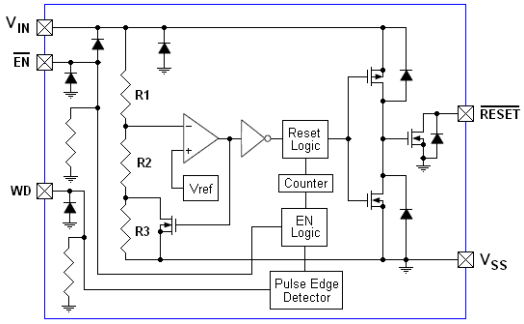


BLOCK DIAGRAMS (CONTINUED)

IXD5123



IXD5124



Diodes inside the circuits are ESD protection diodes and parasitic diodes.

BASIC OPERATION

The error amplifier compares the internal reference voltage with the voltage divided by resistors R1, R2, and R3 connected to the V_{IN} pin of the IXD5121 – 4 (see block diagrams above). The resulting output signal from the error amplifier activates the watchdog logic, delay circuit, and the output driver. When the V_{IN} voltage becomes equal or below detect voltage, the $\overline{RESET}$ output goes from high to low state.

$\overline{RESET}$ Pin Output Signal

The $\overline{RESET}$ pin output goes from high to low state whenever the V_{IN} pin voltage becomes equal or below the detect voltage. The $\overline{RESET}$ pin remains in low state during the Release Delay Time t_{DR} after the V_{IN} voltage becomes equal or above the release voltage. When Release Delay Time t_{DR} elapsed, the $\overline{RESET}$ pin goes into high state, if no rising or falling signals appear on the WD pin within the watchdog timeout period.

Hysteresis

When the internal comparator output is high, the N-channel MOSFET transistor connected in parallel to R3 turns ON, activating the hysteresis circuit. The difference between the release and detect voltages represents the hysteresis width, as shown by the following calculations:

V_{DFL} (detect voltage) = (R1+R2+R3) x Vref / (R2+R3)

V_{DR} (release voltage) = (R1+R2) x Vref / (R2)

V_{HYS} (hysteresis width) =V_{DR}-V_{DFL} (V) = V_{DFL} x 0.05 (typical)

Watchdog (WD) Pin

A watchdog timer enables detection of malfunction or “runaway” of the microprocessor. If no rising or falling signals from the microprocessor appear at the WD pin within the Watchdog Timeout period, the $\overline{RESET}$ pin output remains in the low state during the Release Delay Time (t_{DR}), and thereafter the $\overline{RESET}$ pin goes to high state.

The WD pin has an internal pull-down resistor connected to the V_{SS}. When the watchdog pin is open, or connected to V_{SS}, and watchdog is active, a reset signal comes out after the Watchdog Timeout period (t_{WD}), which is available at 1.6 s, 800 ms, 400 ms, 200 ms, 100 ms, and 50 ms value.

EN Pin

If the watchdog function is not used, the EN pin should be in logic low state. This disables watchdog function only, while the detect voltage circuit remains operational.

The EN pin should be logic high to activate watchdog function. The watchdog function activates immediately, when the EN pin voltage goes from low to high level and the input voltage is higher than the release voltage. (Refer to the TIMING DIAGRAM 1-②.)

However, if the EN pin voltage goes high, when the $\overline{RESET}$ pin is in detection state, the $\overline{RESET}$ pin output maintains this state during the Release Delay Time (t_{DR}) after V_{IN} becomes equal or above V_{DR}. (Refer to the TIMING DIAGRAM 1-①.)

A protection diode is connected between the EN and V_{IN} pins. If the EN pin voltage exceeds V_{IN}, the current will flow to V_{IN} through the diode. To avoid any damage to the IC, EN voltage should not exceed maximum ratings (V_{SS} -0.3 ~ V_{IN} +0.3 V).

$\overline{EN}$ Pin

If the watchdog function is not used, the $\overline{EN}$ pin should be in logic high state. This disables watchdog function only, while the detect voltage circuit remains operational.

The $\overline{EN}$ pin should be logic low to activate the watchdog function. The watchdog function activates immediately, when the $\overline{EN}$ pin voltage goes from high to low level and the input voltage is higher than the release voltage. (Refer to the TIMING DIAGRAM 2-②.)

However, if the $\overline{EN}$ pin voltage goes low, when the $\overline{RESET}$ pin is in detection state, the $\overline{RESET}$ pin output maintains this state during the Release Delay Time (t_{DR}) after V_{IN} becomes equal or above V_{DR}. (Refer to the TIMING DIAGRAM 2-①.)

A protection diode is connected between $\overline{EN}$ and V_{IN} pins. If the $\overline{EN}$ pin voltage exceeds V_{IN}, the current will flow to V_{IN} through the diode. To avoiding any damage to the IC, $\overline{EN}$ pin voltage should not exceed maximum ratings (V_{SS} - 0.3 ~ V_{IN} +0.3 V).

Release Delay Time

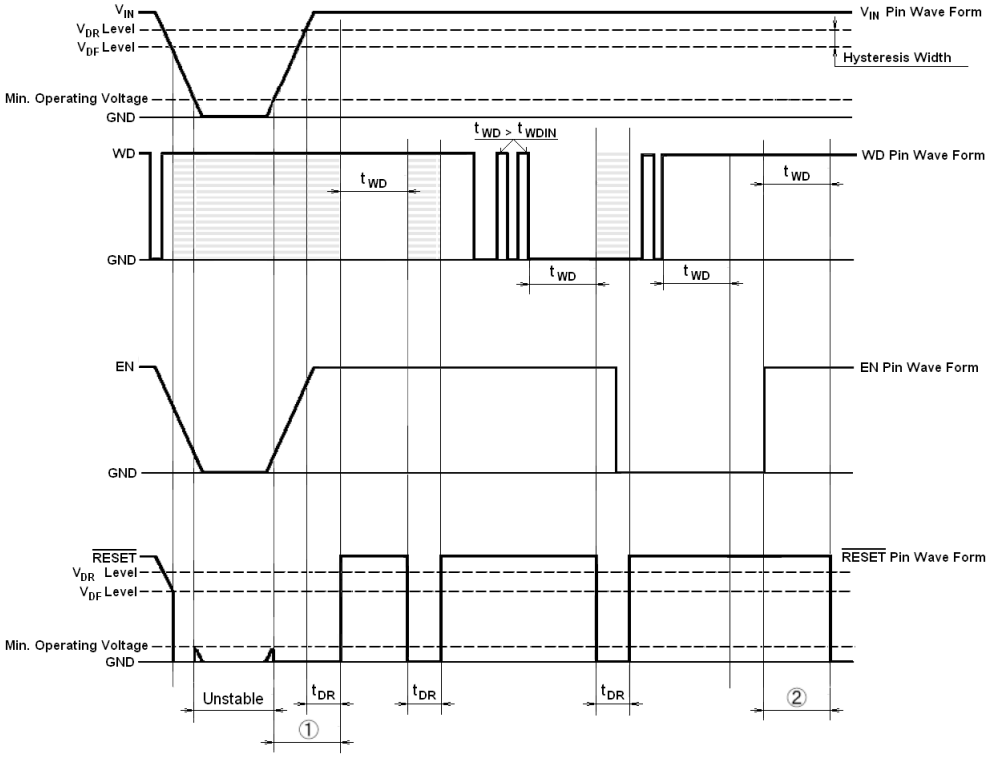
Release Delay Time (t_{DR}) is the time from the moment the V_{IN} pin becomes equal or above the release voltage V_{DR}, until the $\overline{RESET}$ pin output changes state. When the Watchdog Timeout period expires with no rising signal applied to the WD pin, the same Release Delay Time (t_{DR}) should elapse, until the $\overline{RESET}$ pin output changes state. Five release delay times (t_{DR}) are available at 400ms, 200ms, 100ms, 50ms, and 3.13ms.

Detect Delay Time

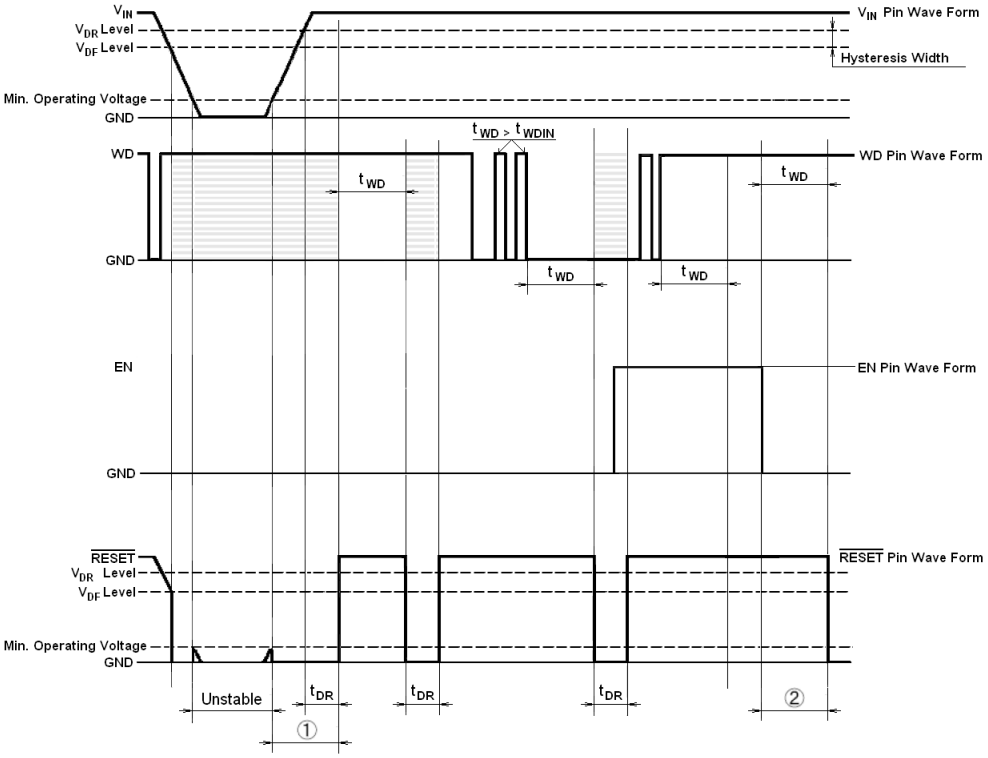
Detect Delay Time (t_{DF}) is the time from the moment the V_{IN} pin voltage becomes equal or below the detect voltage until the $\overline{RESET}$ pin output goes into the detection state.

TIMING DIAGRAMS

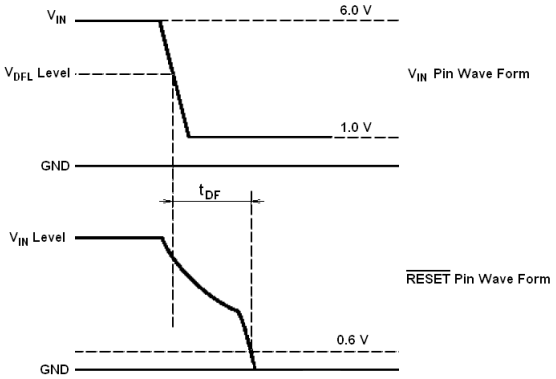
Timing Diagram 1. IXD5121/2 Series



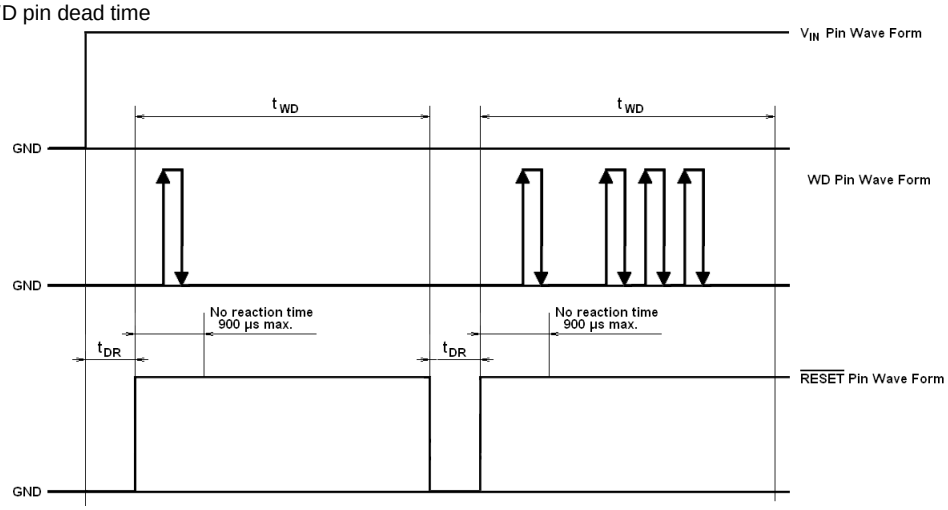
Timing Diagram . IXD5123/4 Series



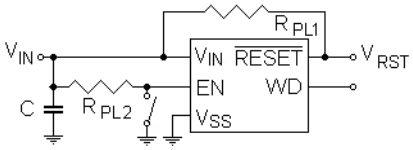
Timing Diagram 3. $\overline{\text{RESET}}$ Pin output voltage with R_{PULL} = 100 kΩ

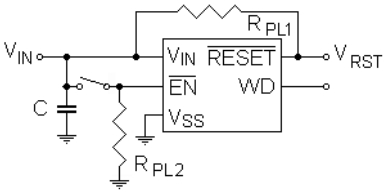


Timing Diagram 4. WD pin dead time



TYPICAL





APPLICATION CIRCUIT

IXD5121/22 IXD5123/4

Resistors RPL2 are used with IXD5121 and IXD5123 series only.

LAYOUT AND USE CONSIDERATIONS

1. The IC may malfunction if absolute maximum ratings are exceeded.
2. High impedance V_{IN} power supply may cause IC malfunction, if V_{IN} voltage falls below minimum operating level due current consumption, when IC output changes state. In addition, the $\overline{RESET}$ pin voltage at "High" state reflects every variations of V_{IN} voltage.
3. High impedance V_{IN} power supply may cause IC oscillations, if voltage drop at power supply's internal resistance exceeds IC hysteresis.
4. Note that a rapid and high amplitude fluctuation of the V_{IN} pin voltage, as well as a power supply noise, may cause a wrong IC operation. The capacitor of 0.22 µF between V_{IN} and GND pins should be used to minimize noise impact.
5. Watchdog Timer has a dead time of less than 900 µs after activation. Signals applied to WD pin during this dead time are ignored (see Timing Diagram 4 above).
6. Internal pull-up/ down resistors at EN/$\overline{EN}$ pins of the IXD5122/4 series allows use watchdog function with these pins open. IXD5121/23 series require EN/$\overline{EN}$ pins to be pulled up/down respectively to activate watchdog function.

PIN LOGIC STATE ASSIGNMENT

PIN NAME	CONDITIONS	ASSIGNED LOGIC STATE
V_{IN}	$V_{IN} \geq V_{DFL} + V_{HYS}$	H
	$V_{IN} \leq V_{DFL}$	L
EN/$\overline{EN}$	$V_{EN} \geq 1.3$ V	H
	$V_{EN} \leq 0.35$ V	L
WD	$V_{WD} \geq V_{WDH}$ for more than t_{WD}	H
	$V_{WD} \leq V_{WDL}$ for more than t_{WD}	L
	$V_{WD} = V_{WDL} \rightarrow V_{WDH}$ at 300 ns $\leq t_{WDIN} \leq t_{WD}$	L → H
	$V_{WD} = V_{WDH} \rightarrow V_{WDL}$ at 300 ns $\leq t_{WDIN} \leq t_{WD}$	H → L

NOTE:

V_{DFL} - Detect Voltage
V_{HYS} - Hysteresis
V_{WDH} - WD Pin High Level Voltage
V_{WDL} - WD Pin Low Level Voltage
t_{WDIN} - WD Pin Input Pulse Width
t_{WD} - Watchdog Timeout Period
(See Electrical Characteristics for details of each parameter)

LOGIC FUNCTION

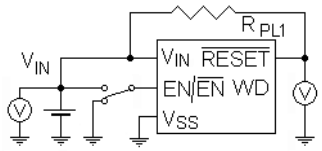
PIN LOGIC STATES							
IXD5121/22 Series				IXD5123/24 Series			
V_{IN}	V_{EN}	WD	V_{RST}	V_{IN}	V_{EN}	WD	V_{RST} [2)]
H	H	Static H	Repeating transitions H → L → H	H	L	Static H	Repeating transitions H → L → H
H	H	Static L	Repeating transitions H → L → H	H	L	Static L	Repeating transitions H → L → H

H	H	Transitions L ↔ H	H	H	L	Transitions L ↔ H	H
H	L	X[1)]	H	H	H	X	H
L	L	X	L	L	H	X	L

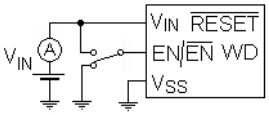
1) X – any logic state
2) V_{RST} state is undefined if 0.35 V < V_{EN} < 1.3 V
3) EN pin OPEN state for IXD5122 is equal H state, while $\overline{EN}$ pin OPEN state for IXD5124 is equal L state. IXD5121 and IXD5123 do not allow these pins in OPEN state.

TEST CIRCUITS

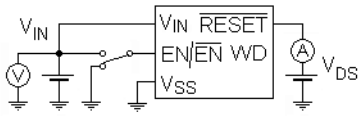
Circuit ①



Circuit ②

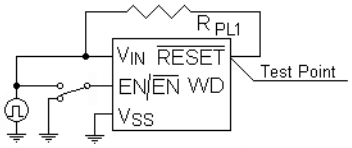


Circuit ③

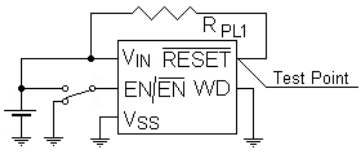


V_{DS} = 0.5 V (V_{DS} = 6.0 V at Leakage Current Measurement

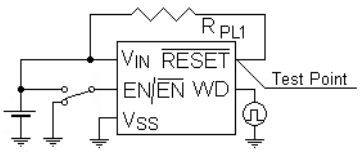
Circuit ④

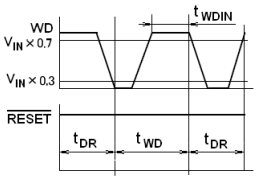


Circuit ⑤

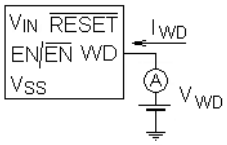


Circuit ⑥

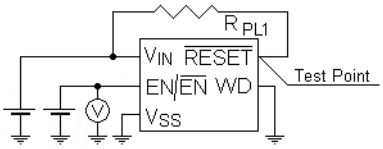


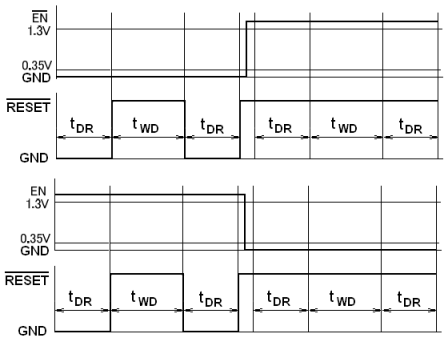


Circuit ⑦

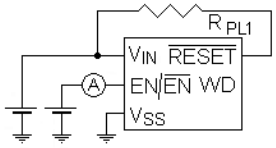


Circuit ⑧





Circuit ⑨

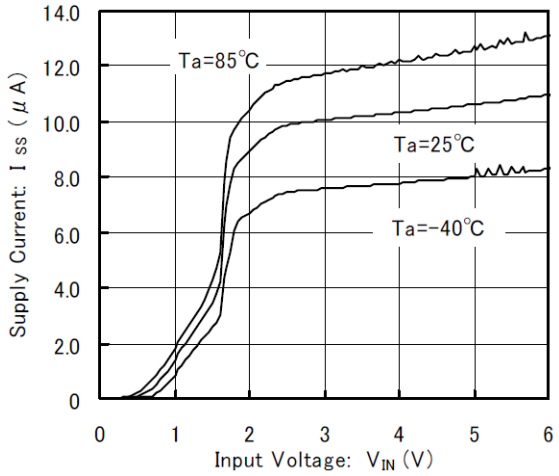


Pull-up Resistor R_{PL1} = 100 kΩ

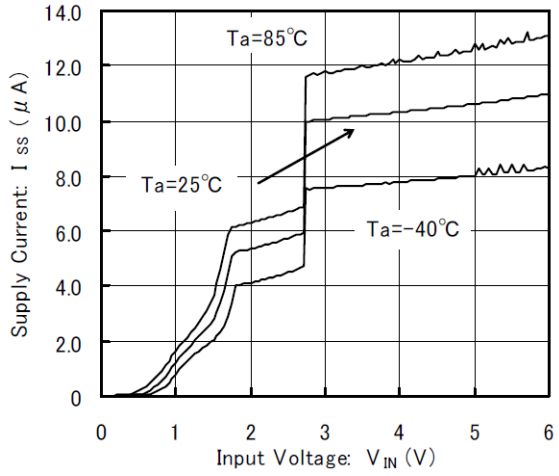
TYPICAL PERFORMANCE CHARACTERISTICS

(1) Supply Current vs. Input Voltage

IXD5121 – 4
V_{DF} = 1.6 V



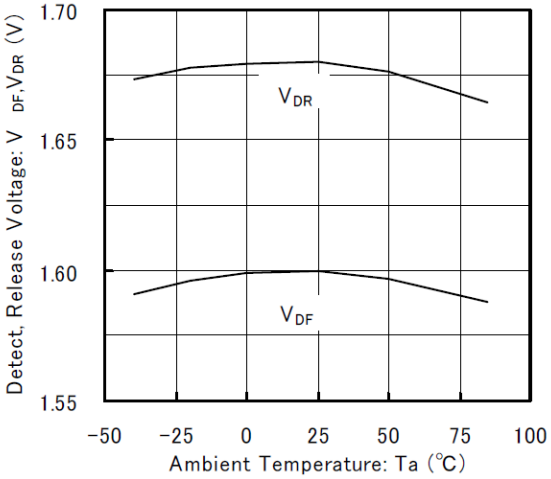
IXD5121 - 4
V_{DF} = 2.7 V



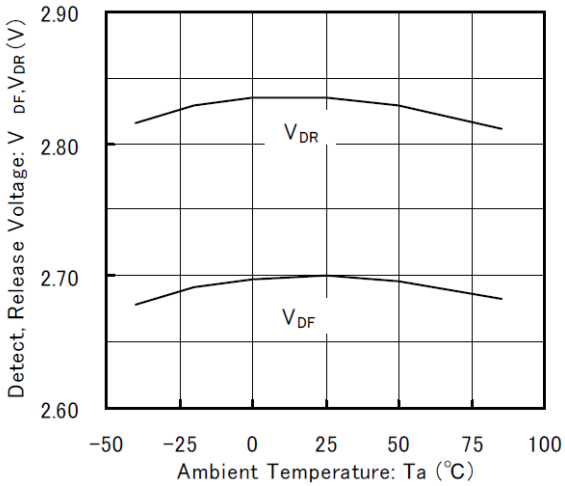
IXD5121 - 4
V_{DF} = 5.0 V

(2) Detect/Release Voltage vs. Ambient Temperature

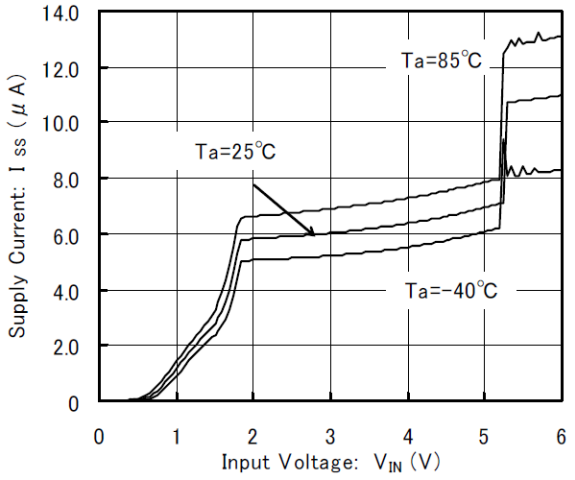
IXD5121 – 4
V_{DF} = 1.6 V

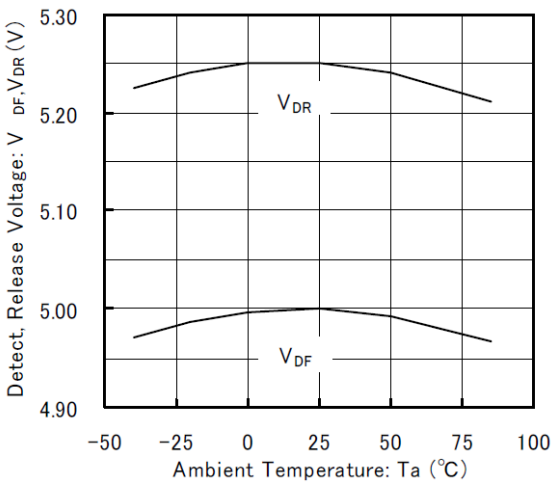


IXD5121 - 4
V_{DF} = 2.7 V



IXD5121 - 4
V_{DF} = 5.0 V

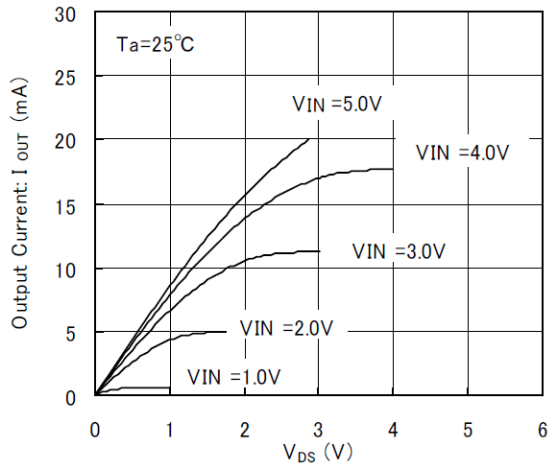




TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

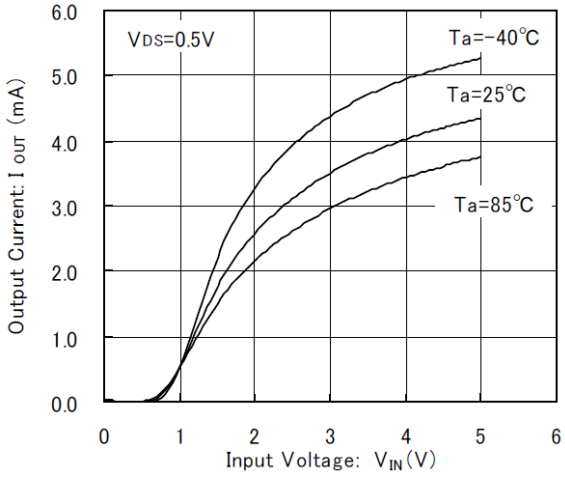
(3) N-channel MOSFET Output Current vs V_{DS} Voltage

IXD5121 - 4



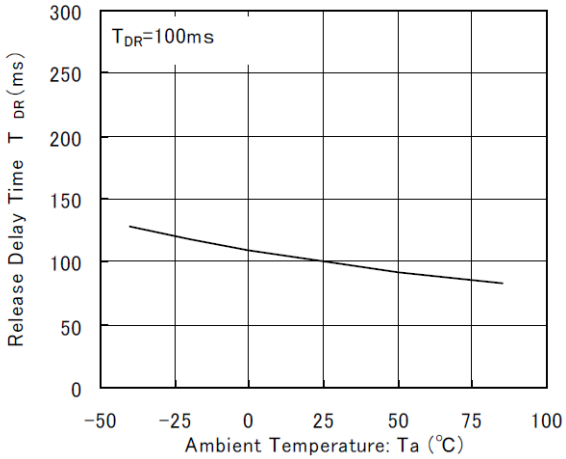
(4) Output Current vs. Input Voltage

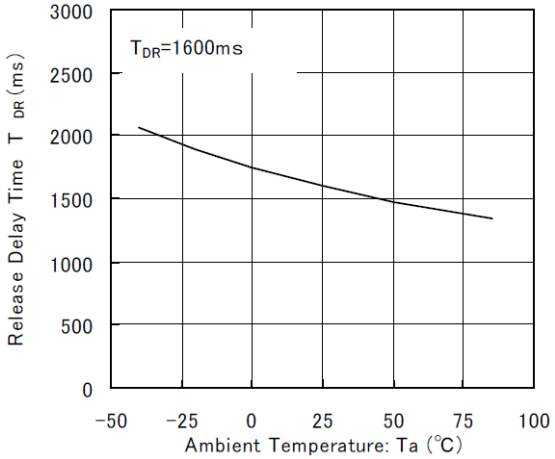
IXD5121 - 4



(5) Release Delay Time vs. Ambient Temperature

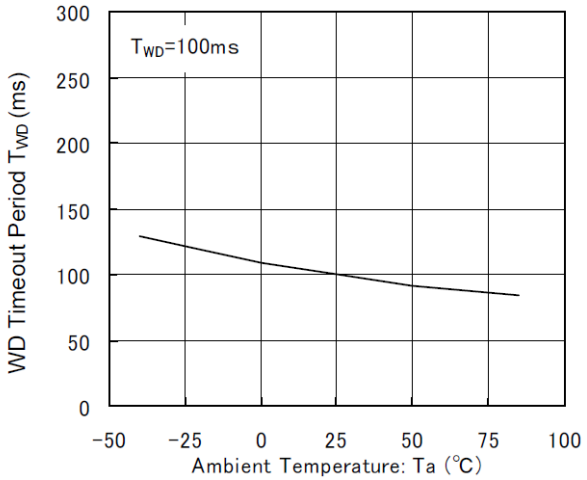
IXD5121 - 4

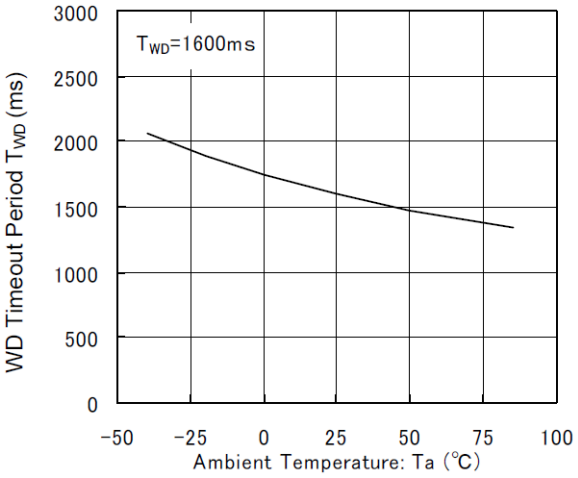




(6) Watchdog Timeout vs. Ambient Temperature

IXD5121 - 4

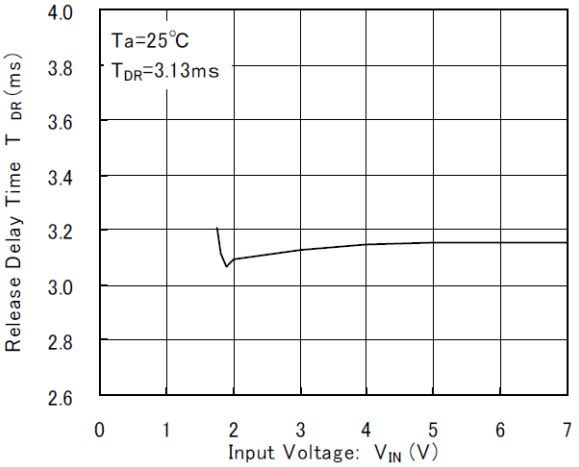




TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

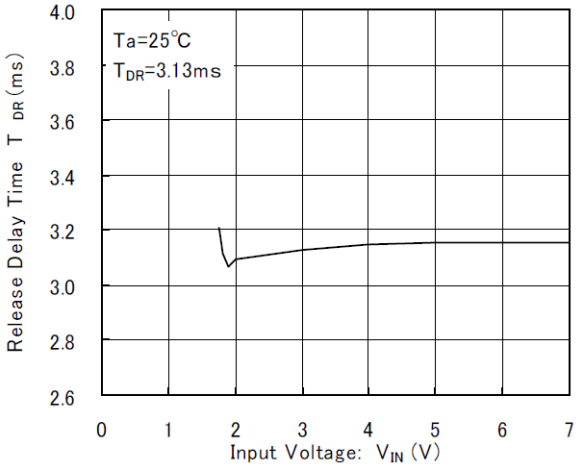
(7) Release Delay Time vs Input Voltage

IXD5121 - 4



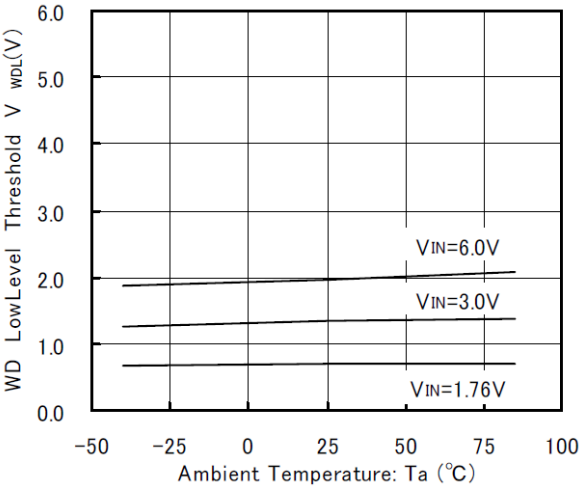
(8) Watchdog Timeout vs. Input Voltage

IXD5121 - 4



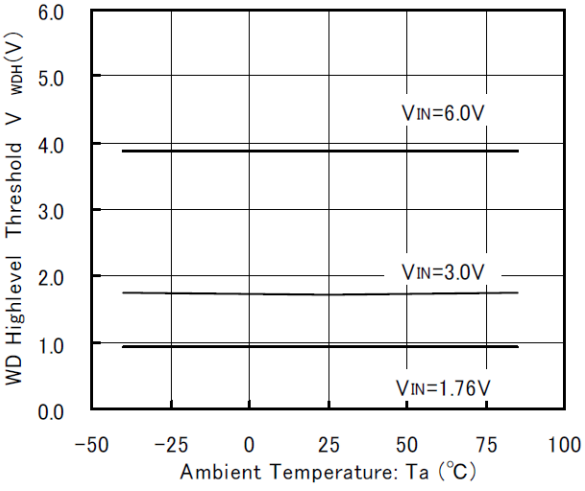
(9) WD Pin LOW Voltage vs. Ambient Temperature

IXD5121 - 4



(10) WD Pin HIGH Voltage vs. Ambient Temperature

IXD5121 - 4

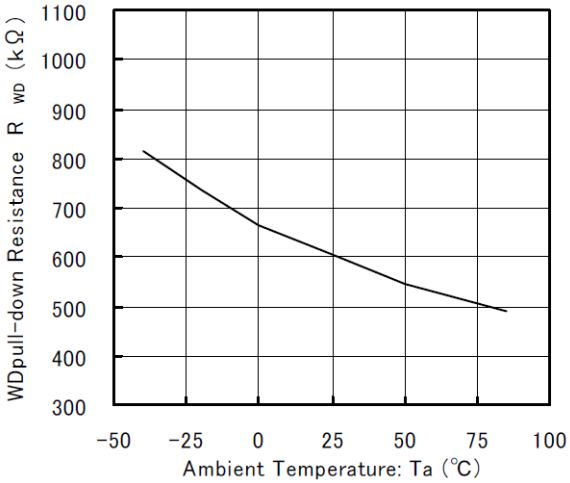


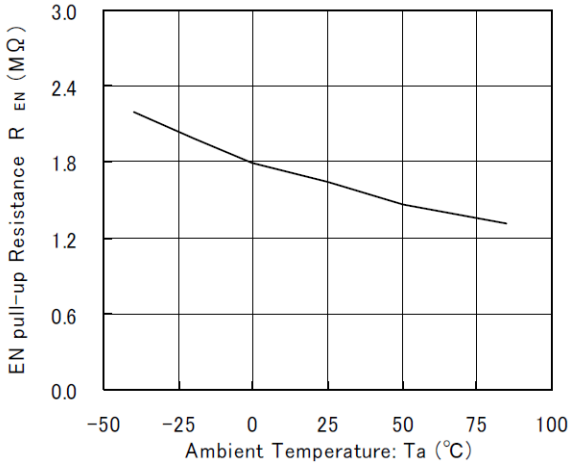
(11) WD Pin Pull-down Resistance vs. Ambient Temperature

IXD5121 - 4

(12) EN Pin Pull-up Resistance vs. Ambient Temperature

IXD5121 - 4

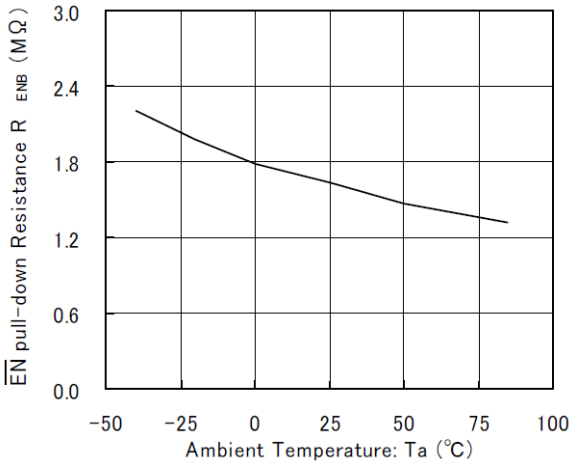




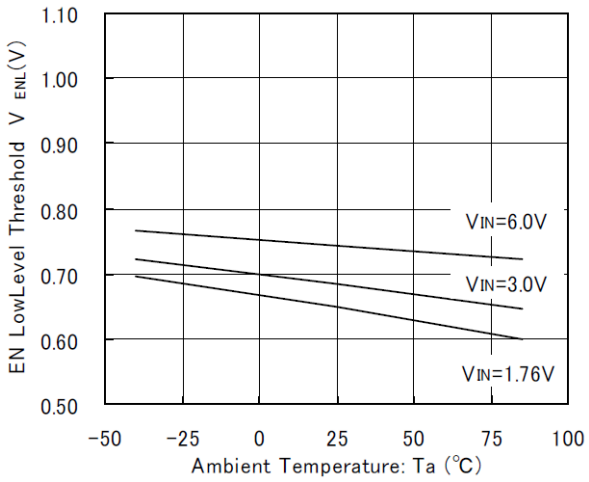
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(13) $\overline{EN}$ Pin Pull-down Resistance vs Ambient Temperature (14) EN Pin LOW Voltage vs. Ambient Temperature

IXD5121 - 4

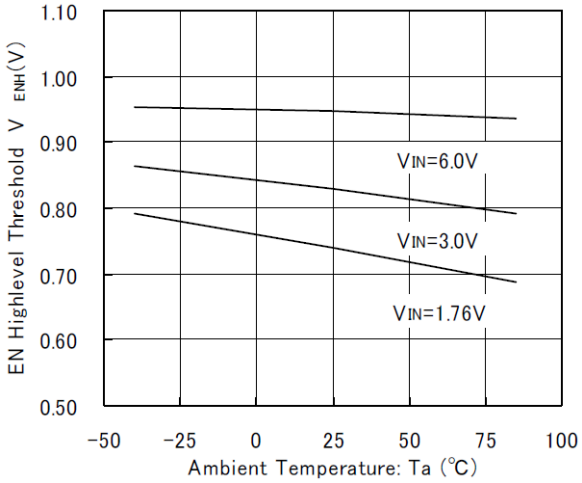


IXD5121 - 4

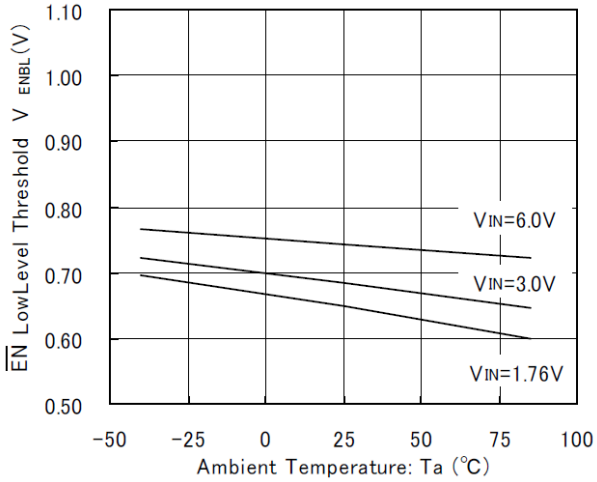


(15) EN Pin HIGH Voltage vs. Ambient Temperature (16) $\overline{EN}$ Pin LOW Voltage vs. Ambient Temperature

IXD5121 - 4

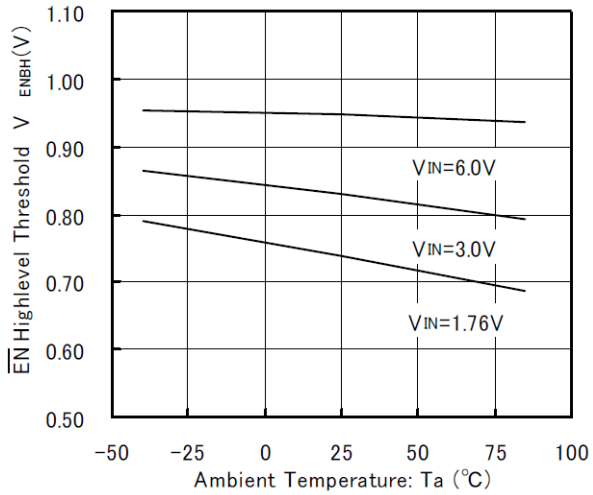


IXD5121 - 4



(17) $\overline{EN}$ Pin HIGH Voltage vs. Ambient Temperature

IXD5121 - 4



ORDERING INFORMATION

IXD5121①②③④⑤⑥-⑦ - EN Pin without pull-up resistor
IXD5122①②③④⑤⑥-⑦ - EN pin with pull-up resistor
IXD5123①②③④⑤⑥-⑦ - $\overline{EN}$ pin without pull-down resistor
IXD5124①②③④⑤⑥-⑦ - $\overline{EN}$ pin with pull-down resistor

DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Release Delay Time[1)]	A	3.13 ms
		C	50 ms
		D	100 ms
		E	200 ms
		F	400 ms
②	Watchdog Timeout	2	50 ms
		3	100 ms
		4	200 ms
		5	400 ms
		6	1.6 s
		7	800 ms
③④	Detect Voltage (V_{DF})	16 - 50	Detect Voltage Range: 1.6 V～5.0 V, e.g. 4.2 V - ③ = 4, ④ = 2
⑤⑥-⑦[(2)]	Packages (Order Unit)	MR	SOT-25 (3000/Reel)
		MR-G	SOT-25 (3000/Reel)
		ER	USP-6C (3000/Reel)
		ER-G	USP-6C (3000/Reel)

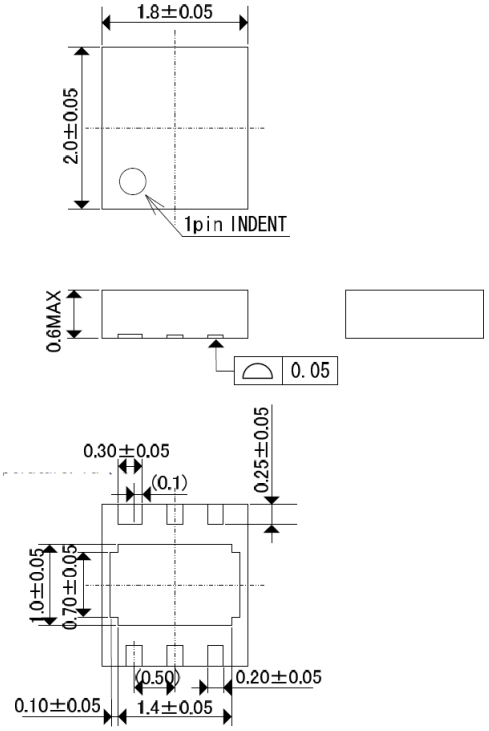
NOTE:

1) Release Delay Time should be equal or shorter than watchdog timeout, i.e. if ① = D, acceptable values for ② are from 3 to 7.
2) The “-G” suffix denotes Halogen and Antimony free as well as being fully RoHS compliant

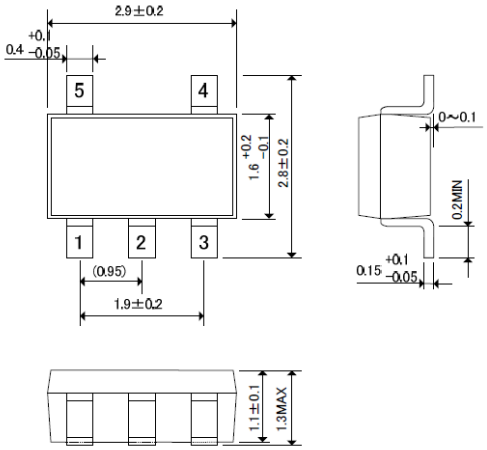
.

PACKAGE DRAWING AND DIMENSIONS

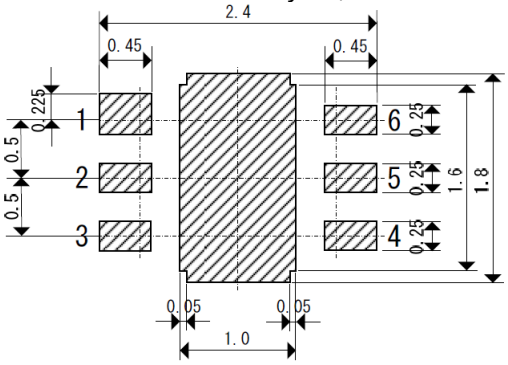
USP-6C, Units: mm



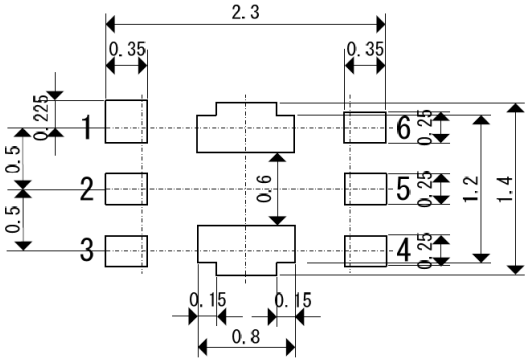
SOT-25, Units: mm



USP-6C Reference Pattern Layout, Units: mm

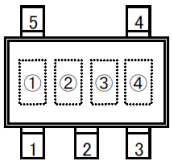


USP-6C Reference Metal Mask Design



MARKING

SOT-25



① Represents product series

MARK	PRODUCT SERIES
E	IXD5121xxxxxx
F	IXD5122xxxxxx
H	IXD5123xxxxxx
K	IXD5124xxxxxx

② Represents release delay time and watchdog timeout

IXD5121

MARK	RELEASE DELAY TIME	WATCHDOG TIMEOUT	PRODUCT SERIES
0	3.13 ms	50 ms	IXD5121A2****
1	3.13 ms	100 ms	IXD5121A3****
2	3.13 ms	200 ms	IXD5121A4****
3	3.13 ms	400 ms	IXD5121A5****
4	3.13 ms	800 ms	IXD5121A7****
5	3.13 ms	1.6 s	IXD5121A6****
6	50 ms	50 ms	IXD5121C2****
7	50 ms	100 ms	IXD5121C3****
8	50 ms	200 ms	IXD5121C4****
9	50 ms	400 ms	IXD5121C5****
A	50 ms	800 ms	IXD5121C7****
B	50 ms	1.6 s	IXD5121C6****
H	100 ms	100 ms	IXD5121D3****
C	100 ms	200 ms	IXD5121D4****
L	100 ms	400 ms	IXD5121D5****
D	100 ms	800 ms	IXD5121D7****
M	100 ms	1.6 s	IXD5121D6****
E	200 ms	200 ms	IXD5121E4****
R	200 ms	400 ms	IXD5121E5****
F	200 ms	800 ms	IXD5121E7****
S	200 ms	1.6 s	IXD5121E6****
T	400 ms	400 ms	IXD5121F5****
K	400 ms	800 ms	IXD5121F7****
U	400 ms	1.6 s	IXD5121F6****

IXD5122 -4

MARK	RELEASE DELAY TIME	WATCHDOG TIMEOUT	PRODUCT SERIES
N	3.13 ms	50 ms	IXD512*A2****
P	3.13 ms	100 ms	IXD512*A3****
R	3.13 ms	200 ms	IXD512*A4****
S	3.13 ms	400 ms	IXD512*A5****
T	3.13 ms	800 ms	IXD512*A7****
U	3.13 ms	1.6 s	IXD512*A6****
V	50 ms	50 ms	IXD512*C2****
X	50 ms	100 ms	IXD512*C3****
Y	50 ms	200 ms	IXD512*C4****
Z	50 ms	400 ms	IXD512*C5****
A	50 ms	800 ms	IXD512*C7****
B	50 ms	1.6 s	IXD512*C6****
A	100 ms	100 ms	IXD512*D3****
C	100 ms	200 ms	IXD512*D4****
B	100 ms	400 ms	IXD512*D5****
D	100 ms	800 ms	IXD512*D7****
C	100 ms	1.6 s	IXD512*D6****
D	200 ms	200 ms	IXD512*E4****
E	200 ms	400 ms	IXD512*E5****
H	200 ms	800 ms	IXD512*E7****
F	200 ms	1.6 s	IXD512*E6****
K	400 ms	400 ms	IXD512*F5****
M	400 ms	800 ms	IXD512*F7****
L	400 ms	1.6 s	IXD512*F6****

MARKING (CONTINUED)

SOT-25

③Represents detect voltage

MARK	DETECT VOLTAGE (V)	PRODUCT SERIES
F	1.6	IXD5121xx16xx
H	1.7	IXD5121xx17xx
K	1.8	IXD5121xx18xx
L	1.9	IXD5121xx19xx
M	2.0	IXD5121xx20xx
N	2.1	IXD5121xx21xx
P	2.2	IXD5121xx22xx
R	2.3	IXD5121xx23xx
S	2.4	IXD5121xx24xx
T	2.5	IXD5121xx25xx
U	2.6	IXD5121xx26xx
V	2.7	IXD5121xx27xx
X	2.8	IXD5121xx28xx
Y	2.9	IXD5121xx29xx
Z	3.0	IXD5121xx30xx
0	3.1	IXD5121xx31xx
1	3.2	IXD5121xx32xx
2	3.3	IXD5121xx33xx
3	3.4	IXD5121xx34xx
4	3.5	IXD5121xx35xx
5	3.6	IXD5121xx36xx
6	3.7	IXD5121xx37xx
7	3.8	IXD5121xx38xx
8	3.9	IXD5121xx39xx
9	4.0	IXD5121xx40xx
A	41	IXD5121xx41xx
B	4.2	IXD5121xx42xx
C	4.3	IXD5121xx43xx
D	4.4	IXD5121xx44xx
E	4.5	IXD5121xx45xx
F	4.6	IXD5121xx46xx
H	4.7	IXD5121xx47xx
K	4.8	IXD5121xx48xx
L	4.9	IXD5121xx49xx
M	5.0	IXD5121xx50xx

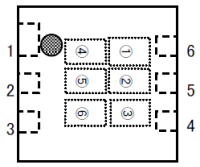
MARK	DETECT VOLTAGE (V)	PRODUCT SERIES
H	1.6	IXD512xxx16xx
K	1.7	IXD512xxx17xx
L	1.8	IXD512xxx18xx
M	1.9	IXD512xxx19xx
N	2.0	IXD512xxx20xx
P	2.1	IXD512xxx21xx
R	2.2	IXD512xxx22xx
S	2.3	IXD512xxx23xx
T	2.4	IXD512xxx24xx
U	2.5	IXD512xxx25xx
V	2.6	IXD512xxx26xx
X	2.7	IXD512xxx27xx
Y	2.8	IXD512xxx28xx
Z	2.9	IXD512xxx29xx
0	3.0	IXD512xxx30xx
1	3.1	IXD512xxx31xx
2	3.2	IXD512xxx32xx
3	3.3	IXD512xxx33xx
4	3.4	IXD512xxx34xx
5	3.5	IXD512xxx35xx
6	3.6	IXD512xxx36xx
7	3.7	IXD512xxx37xx
8	3.8	IXD512xxx38xx
9	3.9	IXD512xxx39xx
A	4.0	IXD512xxx40xx
B	41	IXD512xxx41xx
C	4.2	IXD512xxx42xx
D	4.3	IXD512xxx43xx
E	4.4	IXD512xxx44xx
F	4.5	IXD512xxx45xx
H	4.6	IXD512xxx46xx
K	4.7	IXD512xxx47xx
L	4.8	IXD512xxx48xx
M	4.9	IXD512xxx49xx
N	5.0	IXD512xxx50xx

④ Represents production lot number

0 to 9 and A to Z and inverted 0 to 9 and A to Z repeated. (G, I, J, O, Q, W excluded.)

MARKING (CONTINUED)

USP-6C



① Represents product series

MARK	PRODUCT SERIES
P	IXD5121xxxxxx
K	IXD5122xxxxxx
R	IXD5123xxxxxx
U	IXD5124xxxxxx

② Represents release delay time

MARK	RELEASE DELAY TIME	PRODUCT SERIES
A	3.13 ms	IXD512xAxxxx
C	50 ms	IXD512xCxxxx
D	100 ms	IXD512xDxxxx
E	200 ms	IXD512xExxxx
F	400 ms	IXD512xFxxxx

③Represents watchdog timeout

MARK	WATCHDOG TIMEOUT	PRODUCT SERIES
2	50 ms	IXD512xx2xxx
3	100 ms	IXD512xx3xxx
4	200 ms	IXD512xx4xxx
5	400 ms	IXD512xx5xxx
7	800 ms	IXD512xx7xxx
6	1.6 s	IXD512xx6xxx

④⑤ Represents detect voltage

MARK		DETECT VOLTAGE, V	PRODUCT SERIES
④	⑤		
3	3	3.3	IXD512xxx33x
5	0	5.0	IXD512xxx50x

④ Represents production lot number

0 to 9 and A to Z repeated. (G, I, J, O, Q, W excluded.)

Customer Support

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