

MOSFET

OptiMOS™ Power-Transistor, -150 V

Features

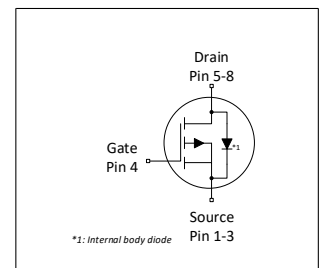
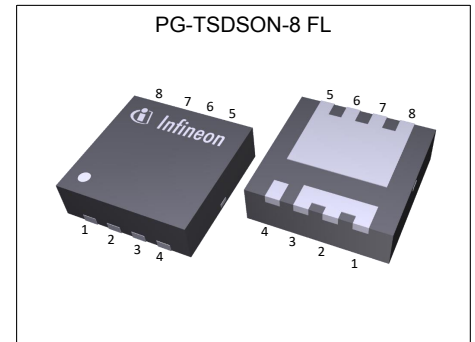
- P-channel, logic level
- Optimized for high and low switching frequency
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-150	V
$R_{DS(on),max}$	560	$m\Omega$
I_D	-6.7	A
Q_{oss}	-8.7	nC
$Q_G (0V...4.5V)$	-15.2	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
ISZ56DP15LM	PG-TSDSON-8 FL	56DP15L	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	-6.7 -4.8 -4.8 -1.35	A	$V_{GS}=-10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=-10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	-27	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	210	mJ	$I_D=-5.5\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	62.5 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=60\text{ °C/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.24	2.4	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area	R_{thJA}	-	-	60	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-150	-	-	V	$V_{GS}=0\text{ V}$, $I_D=-250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	-1	-1.5	-2	V	$V_{DS}=V_{GS}$, $I_D=-724\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	-1 -100	μA	$V_{DS}=-150\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=-150\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	460 453	560 550	m Ω	$V_{GS}=-10\text{ V}$, $I_D=-5\text{ A}$ $V_{GS}=-4.5\text{ V}$, $I_D=-4\text{ A}$
Gate resistance	R_G	-	5	-	Ω	-
Transconductance	g_{fs}	6	12	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=-5\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	1100	1400	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-75\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	48	62	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-75\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	12	21	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-75\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	12.4	-	ns	$V_{DD}=-75\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	14.8	-	ns	$V_{DD}=-75\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	49.6	-	ns	$V_{DD}=-75\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	24.8	-	ns	$V_{DD}=-75\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-5\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-3.2	-	nC	$V_{DD}=-75\text{ V}$, $I_D=-5\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	-1.65	-	nC	$V_{DD}=-75\text{ V}$, $I_D=-5\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	-7.6	-11.4	nC	$V_{DD}=-75\text{ V}$, $I_D=-5\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Switching charge	Q_{sw}	-	-9.1	-	nC	$V_{DD}=-75\text{ V}$, $I_D=-5\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	-15.2	-19	nC	$V_{DD}=-75\text{ V}$, $I_D=-5\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	-2.9	-	V	$V_{DD}=-75\text{ V}$, $I_D=-5\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	-30	-40	nC	$V_{DD}=-75\text{ V}$, $I_D=-5\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	-8.7	-11.6	nC	$V_{DS}=-75\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-6.5	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	-26	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	-0.82	-1.2	V	$V_{GS}=0\text{ V}, I_F=-5\text{ A}, T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	72.3	144.6	ns	$V_R=-75\text{ V}, I_F=-5\text{ A}, di_F/dt=-100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	222.2	444.4	nC	$V_R=-75\text{ V}, I_F=-5\text{ A}, di_F/dt=-100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

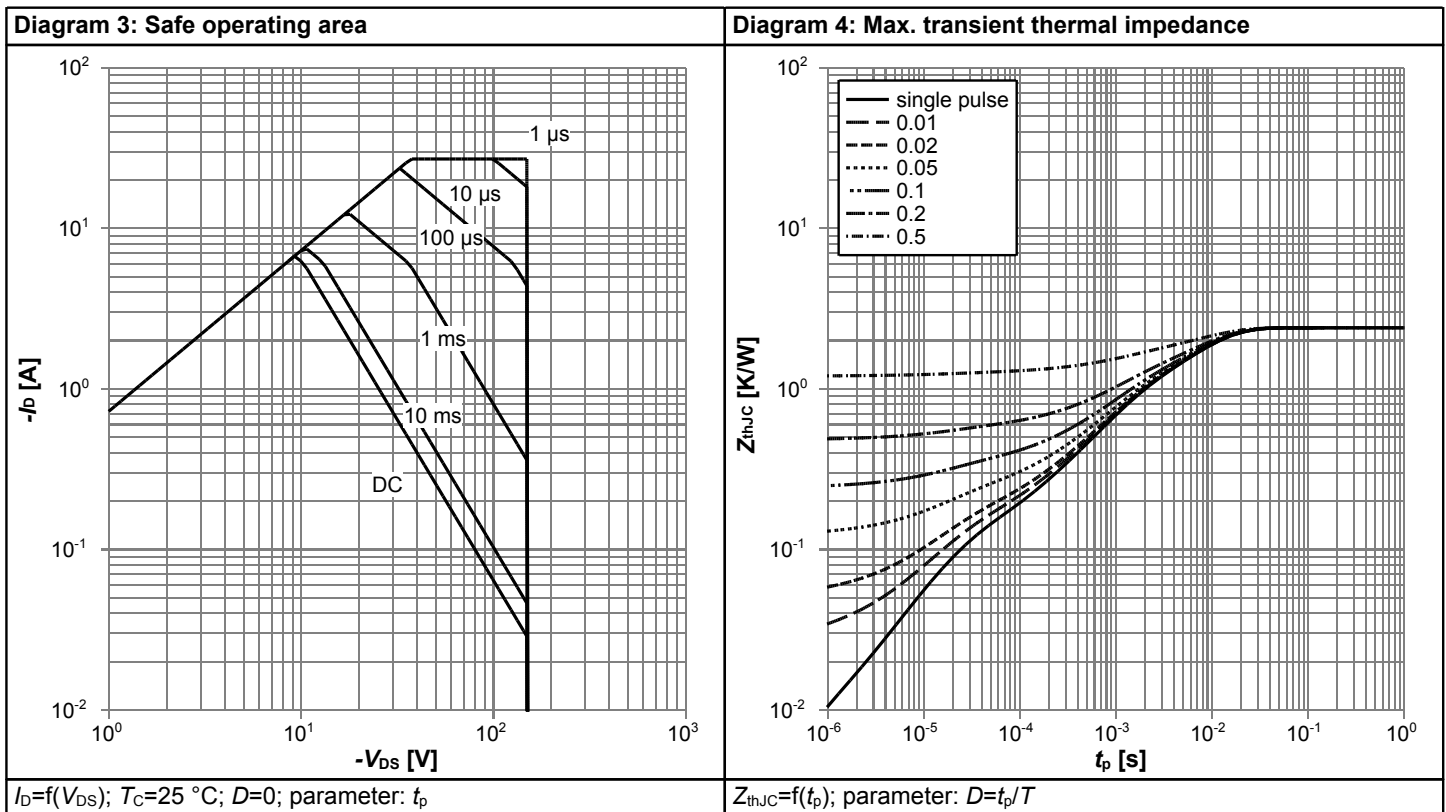
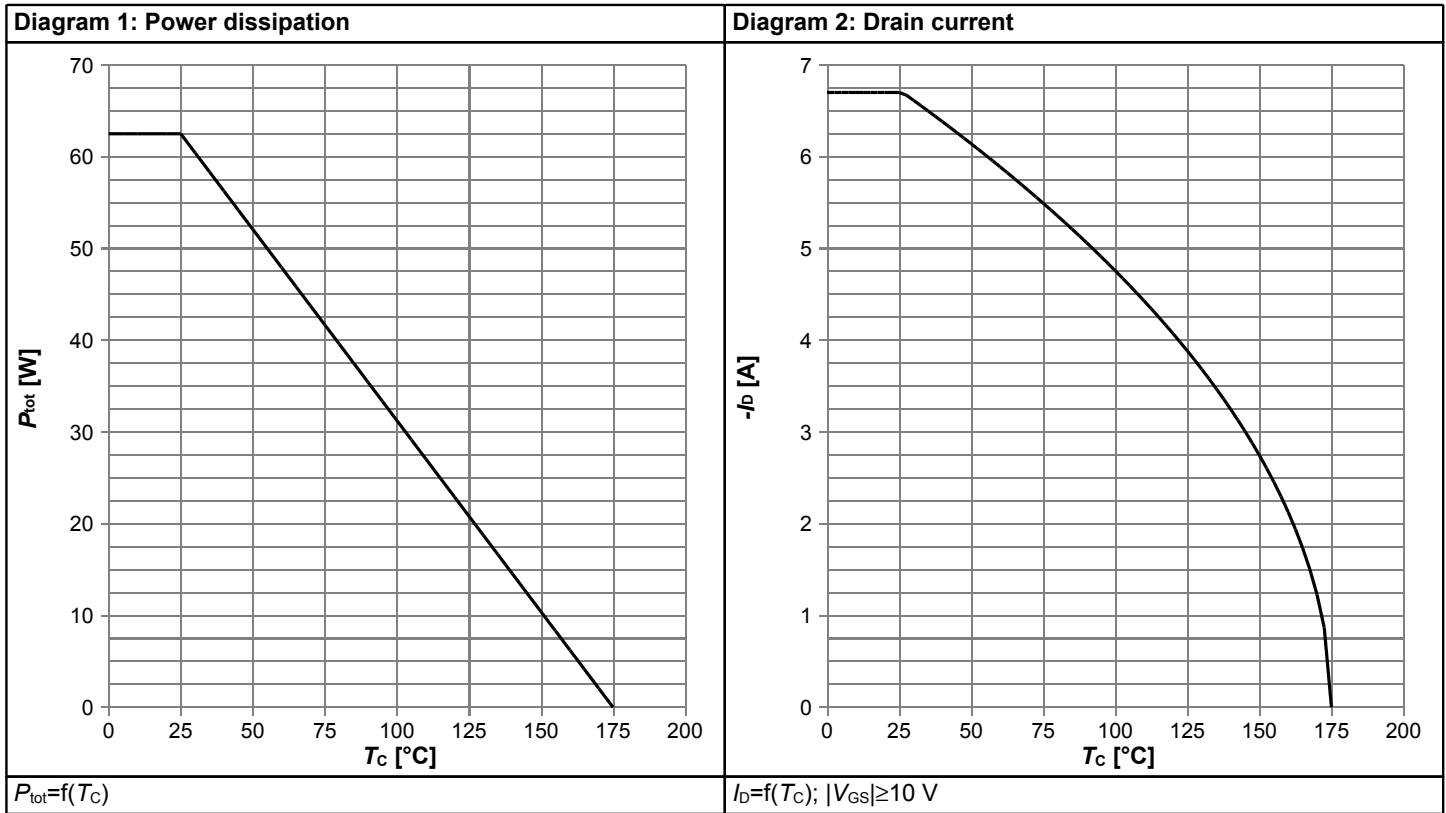
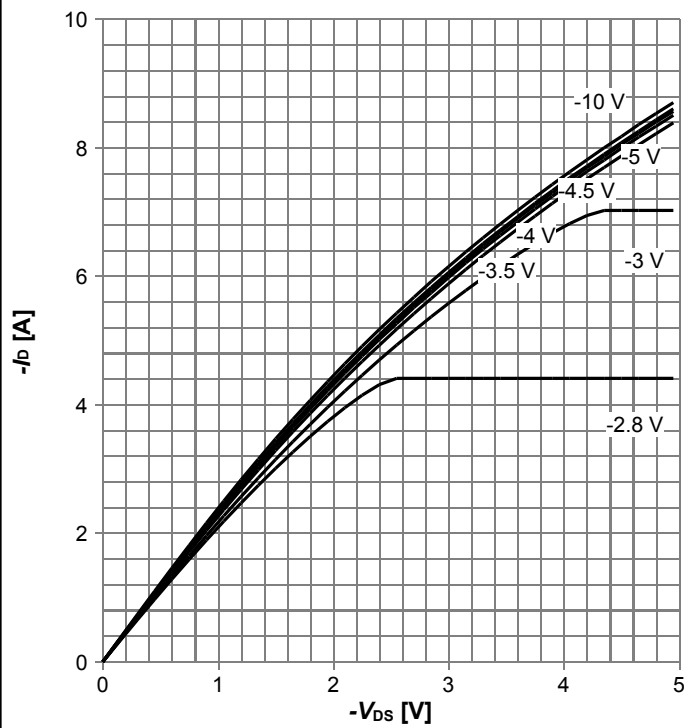
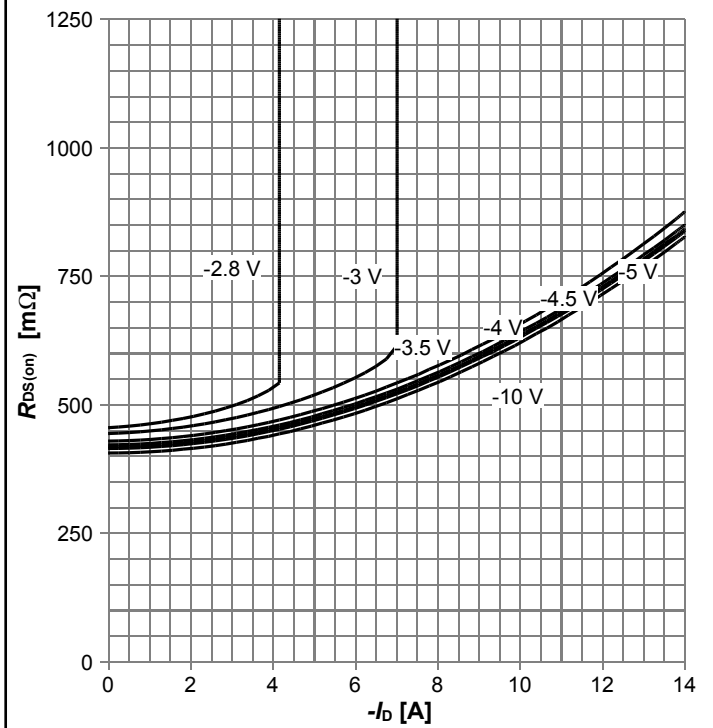


Diagram 5: Typ. output characteristics



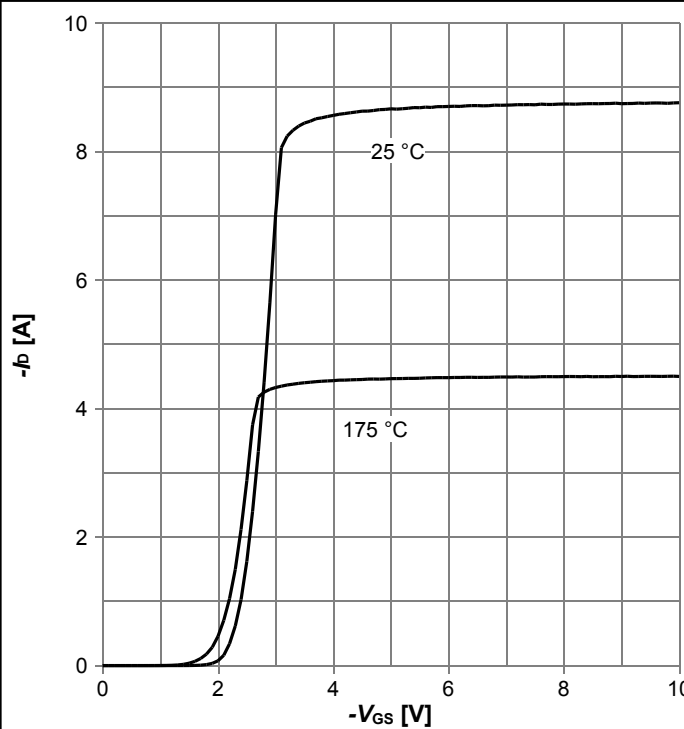
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



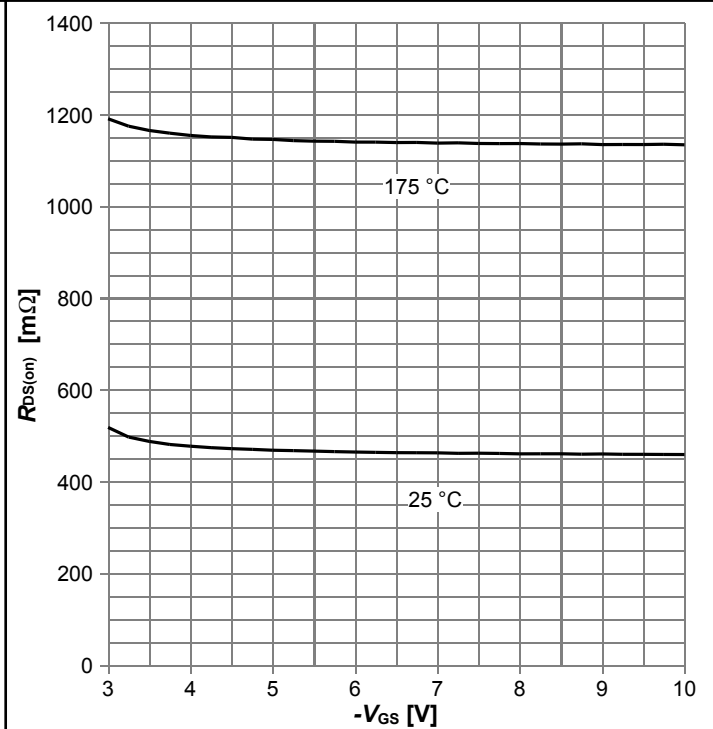
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



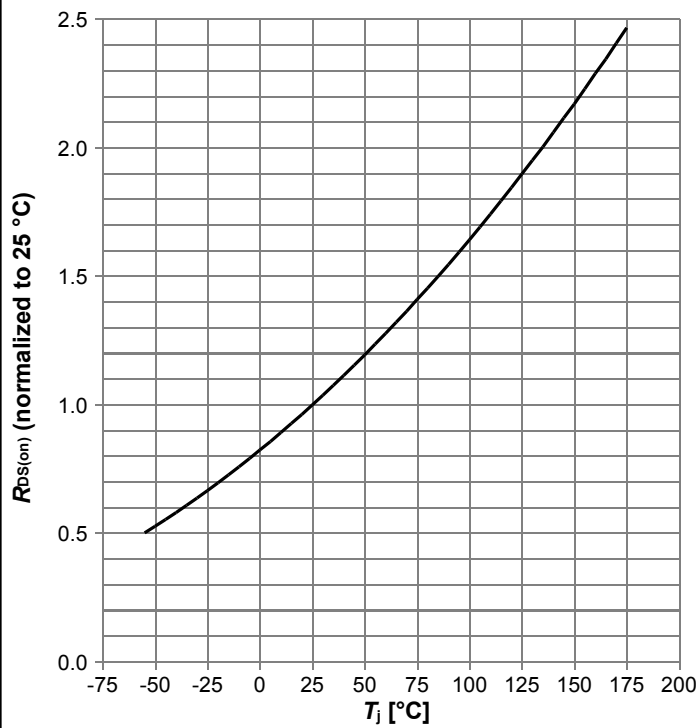
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



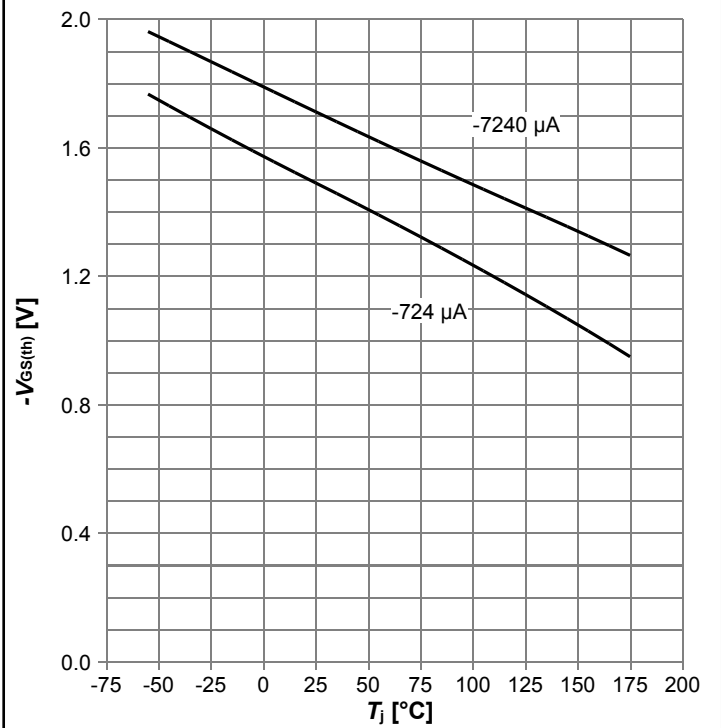
$R_{DS(on)} = f(V_{GS})$, $I_D = -5\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



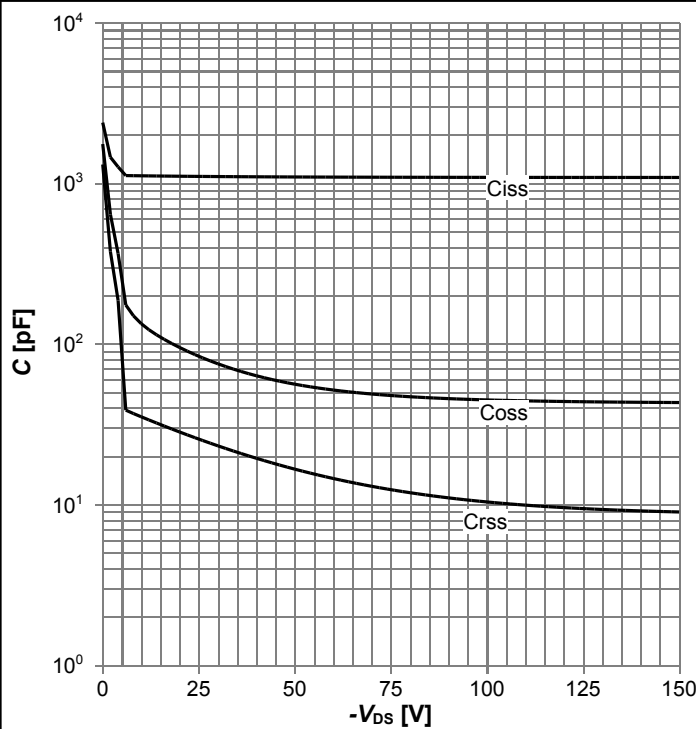
$R_{DS(on)}=f(T_j)$, $I_D=5$ A, $V_{GS}=-10$ V

Diagram 10: Typ. gate threshold voltage



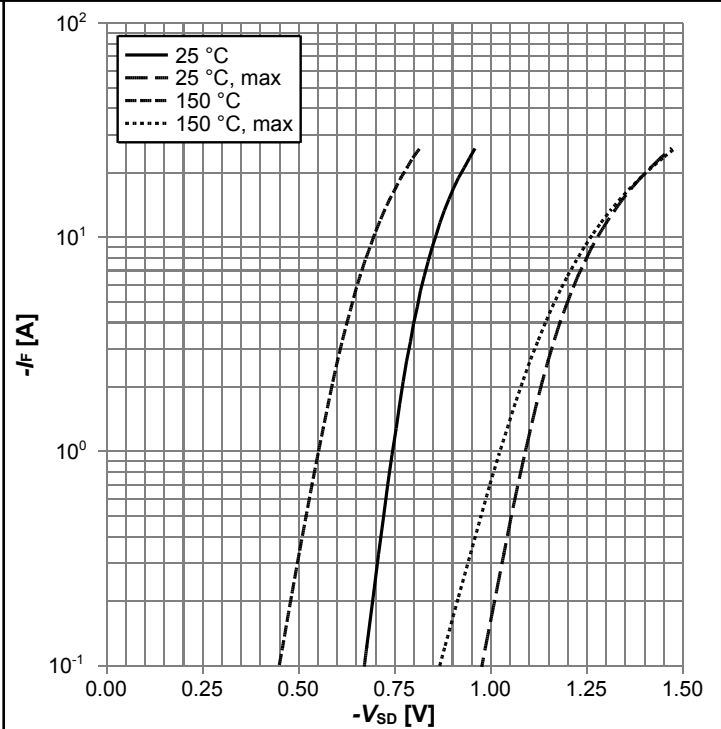
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



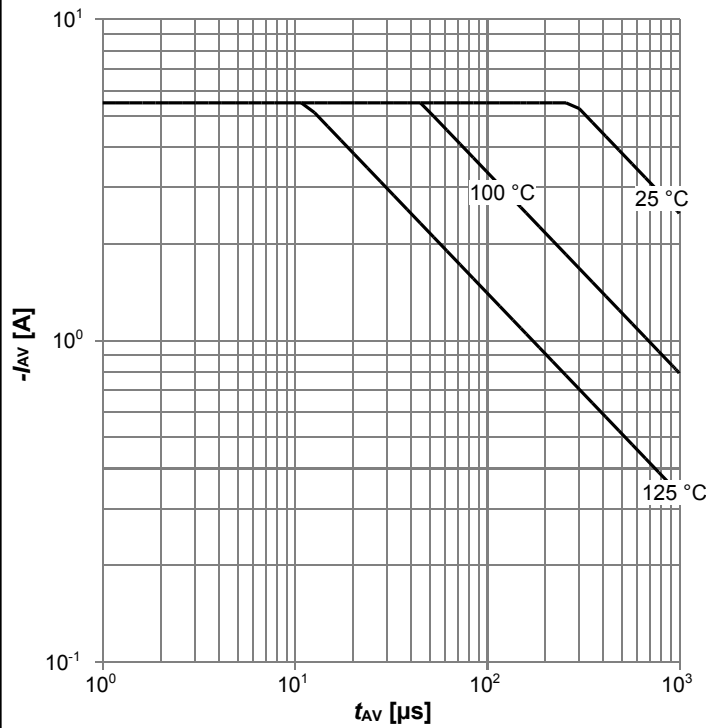
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



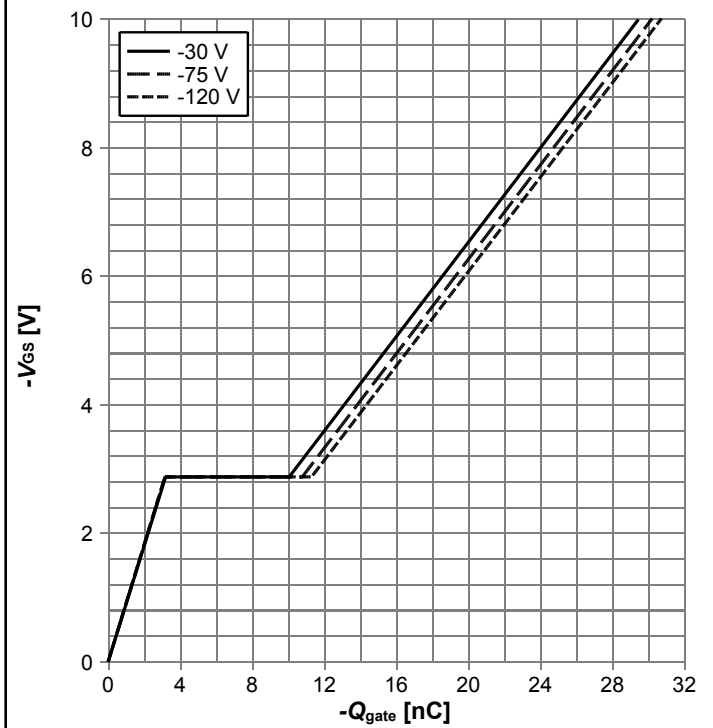
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



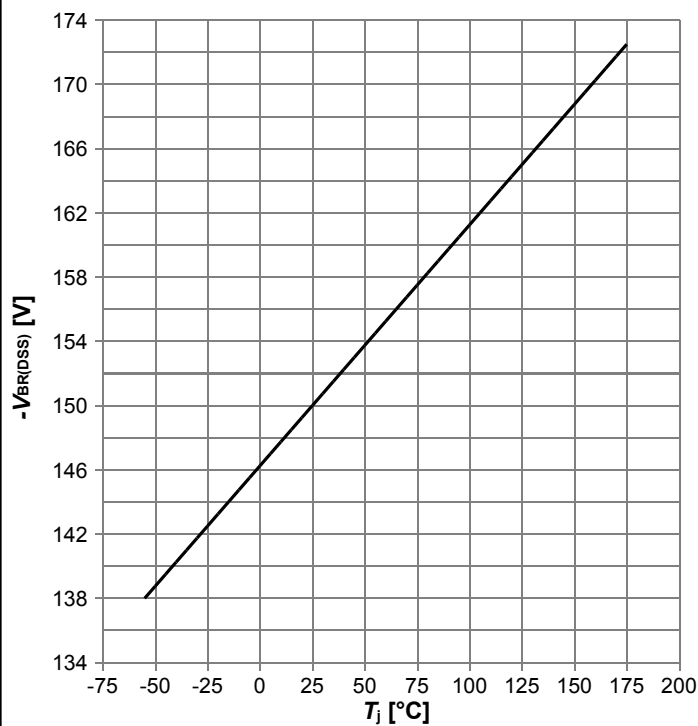
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



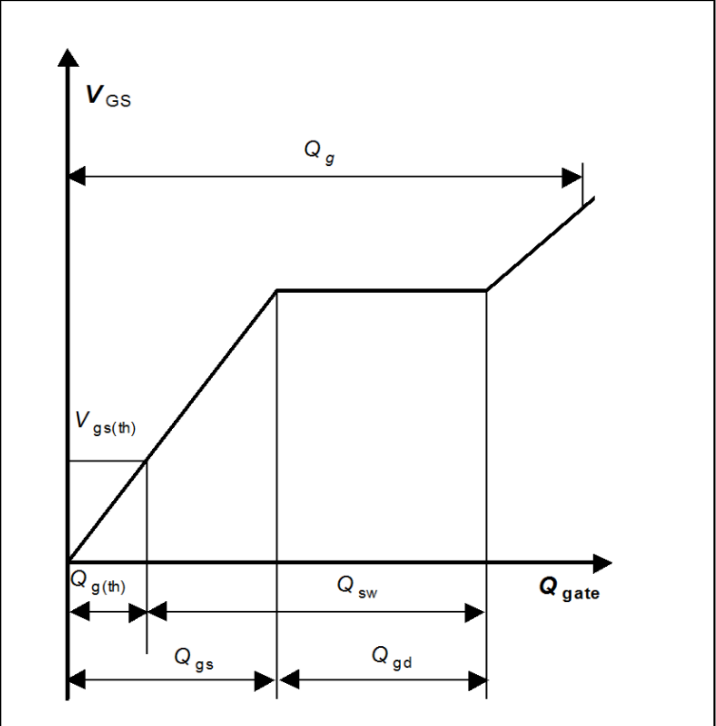
$V_{GS}=f(Q_{gate}), I_D=-5 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

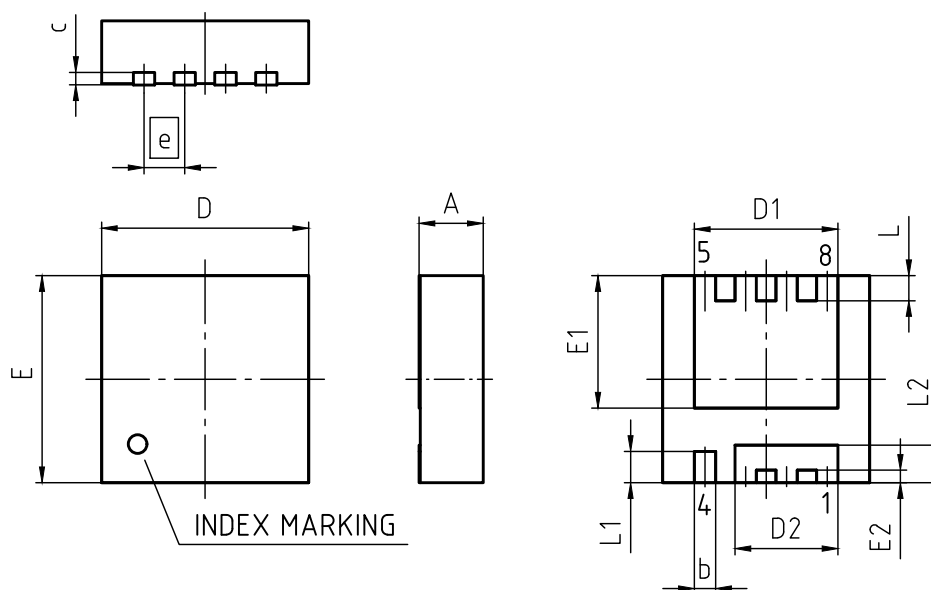


$V_{BR(DSS)}=f(T_j); I_D=-250 \mu\text{A}$

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER: PG-TSDSON-8-U03		
REVISION: 03		DATE: 20.10.2020
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
b	0.24	0.44
c	(0.20)	
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.10	0.30
e	0.65	
L	0.30	0.50
L1	0.40	0.60
L2	0.50	0.70
aaa	0.06	

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm

Revision History

ISZ56DP15LM

Revision: 2022-10-13, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-10-13	Release of final version

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